HIGH VOLTAGE, HIGH POWER

APEX

DC/DC CONVERTERS

HYBRID & IC

MONOLITHIC POWER

HANDBOOK

EVALUATION KITS

APEX µtech
DEDICATED TO EXCELLENCE

APEX MICROTECHNOLOGY CORPORATION
VOLUME V

PRODUCT REPLACEMENT POLICY

The APEX product warranty as stated on page F2, applies only to the original customer and is in lieu of all other warranties—expressed or implied. Under no condition will Apex Microtechnology Corp. be liable for any anticipated profits, consequential damages, loss of time or other losses incurred by the customer in connection with the purchase and/or use of Apex products.

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Apex has made every effort to insure the accuracy of this handbook to factory specifications as of August 1, 1991; however, no responsibility is assumed for possible omission or inaccuracies.

Apex Microtechnology Corp. reserves the right to make changes without further notice to any specifications or products herein to improve reliability, function or design. Changes and additions made after the publication of this handbook will be reflected in updated product data sheets or other literature as soon as possible. If more detailed information on any product is desired, contact Apex directly or any Apex authorized representative.

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The following is a trademark of APEX MICROTECHNOLOGY CORP.

Certain Apex products are manufactured under the following U.S. patents:
4833423, 07108745, 4871965.

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FREE TECHNICAL SUPPORT TO SERVE YOU

Applications Hotline and Technical Seminars

The APEX Applications hotline is the quickest way to get answers about your specific circuit needs. It puts you in touch with a wealth of experience. We can assist you with product selection, design suggestions, schematic review and circuit debugging.

APEX also conducts technical seminars across the U.S. and around the free world. These seminars are designed to provide you with extensive information on power amplifiers and DC/DC converter applications, in addition to the hows and whys of internal circuits and construction. Pros and cons of various approaches are presented along with potential dangers. Question and answer periods emphasize areas of special interest. These seminars are available free to groups of 10 or more engineers interested in APEX products. Contact your local APEX sales representative, or one of us directly about seminar scheduling in your area.

Application notes are developed with the help of your questions, suggestions and feedback. Please call us if you have identified and implemented a new useful application are ready to share the information with others.

We are always open to suggestions on products you'd like to see from us.

Tim Green
Applications Engineer
(602) 742-8662

Jerry Steele
Applications Engineer
(602) 742-8663

1-800-421-1865

OUTPUT SATURATION VOLTAGE VS OUTPUT CURRENT (TYP)

RANKED BY OUTPUT CURRENT

I_O	.1	.4	1	2	4	5	10	15	20	30
PA03	2.5	2.5	2.5	2.5	3.0	3.0	3.5	4.0	5.0	6.0
PA04*	2.0	2.0	2.0	2.2	2.8	3.0	3.5	4.5	5.0	—
PA04	5.0	5.0	5.0	5.5	6.0	6.2	7.5	8.5	10.0	—
PA12A	3.7	3.7	3.7	3.8	4.0	4.1	4.6	6.0	—	—
PA61	3.2	3.3	3.4	3.4	3.8	4.0	4.5	—	—	—
PA51	3.6	3.6	3.7	3.8	4.0	4.2	5.0	—	—	—
PA07	3.0	3.0	3.2	3.5	4.2	4.6	—	—	—	—
PA10	3.5	3.7	3.8	4.1	5.0	5.5	—	—	—	—
PA73	3.5	3.6	3.7	3.9	6.3	7.6	—	—	—	—
PA01	3.5	3.9	4.1	4.4	5.9	6.7	—	—	—	—
PA02	0.6	0.7	0.9	1.2	2.0	3.0	—	—	—	—
PA19	0.5	0.5	1.0	2.0	4.0	—	—	—	—	—
PA21	0.8	0.9	1.2	1.8	2.7	—	—	—	—	—
PA09	6.0	6.2	6.5	7.0	8.0	—	—	—	—	—
PB50	5.5	6.5	7.0	9.0	—	—	—	—	—	—
PB58	5.5	6.5	7.0	—	—	—	—	—	—	—
WA01	2.0	3.5	—	—	—	—	—	—	—	—

*with boost

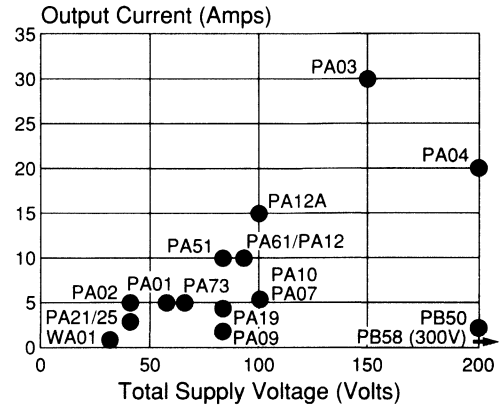
FREQUENCY (kHz) VS PEAK-TO-PEAK OUTPUT VOLTAGE (TYP)

RANKED BY SUPPLY VOLTAGE RANGE

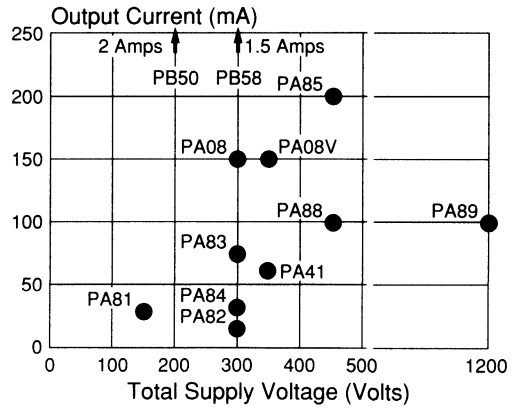
V_O(p-p)	20	25	30	45	60	90	120	180	280	430
PA85	3000	3000	3000	3000	2500	1600	1250	830	530	350
PA88	70	60	55	40	28	21	15	11	7	4
PA41	350	300	250	150	110	70	55	35	25	—
PA84	500	500	500	500	500	380	330	220	130	—
PB58	300	300	300	300	300	300	260	160	102	—
PA08	630	500	420	280	210	140	105	70	45	—
PA83	700	560	460	310	230	150	110	80	50	—
PA82	500	400	330	220	160	110	80	55	36	—
PB50	300	300	300	300	300	300	260	160	—	—
PA04	900	720	600	400	300	200	150	100	—	—
PA81	500	400	330	220	160	110	80	55	—	—
PA03	135	108	90	60	45	30	22	—	—	—
PA07	60	48	40	27	20	13	—	—	—	—
PA12	60	48	40	27	20	13	—	—	—	—
PA10	88	70	60	40	30	20	—	—	—	—
PA61	40	33	30	24	18	13	—	—	—	—
PA19†	5000	5000	5000	5000	5000	—	—	—	—	—
PA09	2600	2600	2200	1500	1100	—	—	—	—	—
PA51	55	45	37	25	18	—	—	—	—	—
PA73	50	42	35	23	—	—	—	—	—	—
PA01	50	42	35	23	—	—	—	—	—	—
PA02	300	240	200	—	—	—	—	—	—	—
PA21/25	33	20	17	—	—	—	—	—	—	—
WA01	40,000	—	—	—	—	—	—	—	—	—
WB05	75,000	—	—	—	—	—	—	—	—	—

†Av = 10V/V

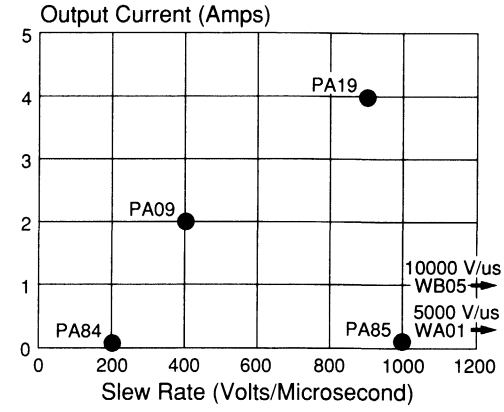
HIGH POWER MATRIX



HIGH VOLTAGE MATRIX



HIGH SPEED MATRIX



HIGH VOLTAGE

Model	±Supply Range Volts Min/Max	Output Current (Cont.) mA, Min	Saturation @I_OMax (V_S-V_O) Volts, Max	Internal Power Watts Max	Slew Rate V/µs Typ	V_{OS} Initial mV Max	V_{OS} vs Temp µV/°C Max	Bias Current nA Max	I_q mA Max	Gain BW Product MHz Typ	Current Limit (Amps)	Thermal Shutdown	Temp Range °C Min/Max
PA89	50/600	100	36	40	1.2	2	30	.05	4	2	Ext Adj	No	–25/85
PA89A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA85	15/225	200	10	35	1000	2	30	.05	25	110	Ext Adj	Yes	–25/85
PA85A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA85M	*	*	*	*	*	2	30	.05	*	*	*	*	–55/125
PA88	15/225	100	10	15	30	2	30	.05	2	10	Ext Adj	No	–25/85
PA88A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA41	50/175	60	12	12	40	30	65	.05	2	1.6	Ext Adj	No	–25/85
PA08V	15/175	150	15	17.5	30	2	30	.05	8.5	5	Ext Adj	Yes	–25/85
PA08	15/150	*	*	*	*	*	*	*	*	*	*	*	*
PA08A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA08M	*	*	*	*	*	2	30	.05	*	*	*	*	–55/125
PB58	15/150	1500	11	80	100	1500	7000	—	12	2.5	Ext Adj	No	–25/85
PB58A	*	2000	*	*	*	1000	*	—	*	*	*	*	*
PA83	15/150	75	10	17.5	30	3	25	.05	8.5	5	(.1)	Yes	–25/85
PA83A	*	*	*	*	*	1	10	.01	*	*	*	*	*
PA83M	*	*	*	*	*	3	25	.05	*	*	*	*	–55/125
PA84	15/150	40	7	17.5	200	3	25	.05	7.5	76	(.05)	Yes	–25/85
PA84A	*	*	*	*	*	1	10	.01	*	*	*	*	*
PA84M	*	*	*	*	*	3	25	.05	*	*	*	*	–55/125
PA84S	*	*	*	*	*	*	*	*	*	*	*	*	–25/85
PA82J	70/150	15	5	11.5	20	3	25	.05	8.5	5	(.025)	Yes	0/70
PB50	30/100	2000	11	35	100	1750	7000	—	18	2.5	Ext Adj	No	–25/85
PA81J	32/75	30	5	11.5	20	3	25	.05	8.5	5	(.05)	Yes	0/70

†Specifications apply for T_C = 25°C, unless otherwise stated. *Specification is same as above.

HIGH SPEED

Model	Slew Rate V/µs Typ	Output Current (Cont.) Amps., Min	±Supply Range Volts Min/Max	Saturation @I_OMax (V_S-V_O) Volts, Max	Internal Power Watts Max	V_{OS} Initial mV Max	V_{OS} vs Temp µV/°C Max	Bias Current nA Max	I_q mA Max	Gain BW Product MHz Typ	Current Limit (Amps)	Thermal Shutdown	Temp Range °C Min/Max
WA01	5000	.4	12/16	4	10.5	10	5.	20000	30	—	(.6)	No	–25/85
WA01A	*	*	*	*	*	5	25	10000	*	*	*	*	*
WB05	10000	1	5/15	6.5	15	100	500	30000	30	250	(1.5)	No	–25/85
PA85	1000	.2	15/225	10	35	2	30	.05	25	110	Ext Adj	Yes	–25/85
PA85A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA85M	*	*	*	*	4	2	30	.05	*	*	*	*	–55/125
PA19	900	4	15/40	5	78	3	30	.2	120	100	Ext Adj	Yes	–25/85
PA19A	*	*	*	*	*	.5	10	.05	*	*	*	*	*
PA09	400	2	12/40	8	78	3	30	.1	85	150	(4.5)	Yes	–25/85
PA09A	*	*	*	*	*	.5	10	.02	*	*	*	*	*
PA09M	*	*	*	*	*	3	30	.1	*	*	*	*	–55/125

†Specifications apply for T_C = 25°C, unless otherwise stated. *Specification is same as above.

HIGH POWER

Model	Internal Power Watts Max	Output Current (Cont.) Amps., Min	±Supply Range Volts Min/Max	Saturation @I_OMax (V_S-V_O) Volts, Max	Slew Rate V/µs Typ	V_{OS} Initial mV Max	V_{OS} vs Temp µV/°C Max	Bias Current nA Max	I_q mA Max	Gain BW Product MHz Typ	Current Limit (Amps)	Thermal Shutdown	Temp Range °C Min/Max
PA03	500	30	15/75	7	8	2	30	.05	300	1	Thermal	Yes	–25/85
PA03A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA04	200	20	15/100	5.3/8.8(1)	50	10	50	.05	90	2	Ext Adj	No	–25/85
PA04A	*	*	*	*	*	5	30	.02	*	*	*	*	*
PA12	125	10	10/45	6	4	6	65	30	50	4	Ext Adj	No	–25/85
PA12A	*	15	10/50	7	*	3	40	20	*	*	*	*	–55/125
PA12M	*	*	10/45	6	*	6	65	30	*	*	*	*	*
PA12H		1	*	4		6		30	100		*	*	–25/200
PA61(2)	97	10	10/45	7	2.8	6	65	30	10	1	Ext Adj	No	–25/85
PA61A(2)	*	*	*	6	*	3	40	20	*	*	*	*	*
PA61M(2)	*	*	*	7	*	6	65	30	*	*	*	*	–55/125
PA51(2)	97	10	10/36	8	2.6	10	65	40	10	1	Ext Adj	No	–25/85
PA51A(2)	*	*	10/40	*	*	5	40	20	*	*	*	*	*
PA51M(2)	*	*	10/36	*	*	10	65	40	*	*	*	*	*
PA07	67	5	12/50	5	5	2	30	.05	30	1.3	Ext Adj	Yes	–25/85
PA07A	*	*	*	*	*	.5	10	.01	*	*	*	*	*
PA07M	*	*	*	*	*	2	30	.05	*	*	*	*	–55/125
PA10	67	5	10/45	8	5	6	65	30	30	6	Ext Adj	No	–25/85
PA10A	*	*	10/50	6	*	3	40	20	*	*	*	*	–55/125
PA10M	*	*	10/45	8	*	6	65	30	*	*	*	*	*
PA73(2)	67	5	10/30	8	2.6	10	65	40	5	1	Ext Adj	No	–25/85
PA73M(2)	*	*	*	*	*	*	*	*	*	*	*	*	–55/125
PA01	67	5	10/28	10	2.6	12	65	50	50	1	Ext Adj	No	–25/85
PA02	48	5	7/19	4	20	10	50	.2	37	4.5	Ext Adj	No	–25/85
PA02A	*	*	*	*	*	3	25	.1	*	*	*	*	–55/125
PA02M	*	*	*	*	*	10	50	.2	*	*	*	*	*
PA21	36	2.5	2.5/20	3.0	1.2	10	15 typ	1000	90	.6	(3)	Yes	–25/85
PA21A	*	3.0	*	3.5	*	4	10 typ	250	*	*	(4)	*	*
PA21M	*	2.5	*	3.0	*	10	15typ	1000	*	*	(3)	*	–55/125
PA25	36	2.5	2.5/25	3.0	1.2	10	15 typ	1000	90	.6	(3)	Yes	–25/85
PA25A	*	3.0	*	3.5	*	4	10typ	25	*	*	(4)	*	*
PB50	35	2	30/100	11	100	1750	7000	—	18	2.5	Ext Adj	No	–25/85
PB58	80	1.5	15/150	11	100	1500	7000	—	12	2.5	Ext Adj	No	–25/85
PB58A	*	2.0	*	*	*	1000	*	—	*	*	*	*	*

†Specifications apply for T_C = 25°C, unless otherwise stated. *Specification is same as above.

(1) 5.3 with Boost Voltage = V_S + 5V; 8.8 without Boost Voltage (2) Class "C" output—optimized for low cost—not recommended above 1KHz

DC-DC CONVERTERS

Model	Output Voltage Nom	Output Current Max	Output Power Max	Input Voltage I_O = Max	Output Ripple I_O = Max	Temp Range Min/Max	η Efficiency I_O = Max	Isolation 500Vdc
DB2805SA	5	4.00	20	16-50	50mV	–55/125	74	Yes
DB2812SA	12	1.88	22.5	14-50	40mV	–55/125	76	Yes
DB2815SA	15	1.508	22.5	15-50	40mV	–55/125	77	Yes

SECOND SOURCES FOR APEX PRODUCTS

PA01	OPA511AM	(P/D)	Burr-Brown	Higher cost; slightly improved Vos and Vsat.
PA73	3573	(P/F)	Burr-Brown	
	MIOP42105	(P/F)	Micropac	
PA02	LH0101	(F/E)	National	PC layout can be designed to accept either; output=case; may require external swing enhancement network; some loss of speed and linearity.
PA03	None known			
PA04	None known			
PA07	None known			
PA08	None known			
PA09	TCPA09	(P/F)	Teledyne	
PA10	OPA511AM	(P/D)	Burr-Brown	No foldover current limit; supplies to ±30V only.
	OPA512	(P/D)	Burr-Brown	10A output; higher cost.
PA12	OPA512	(P/F)	Burr-Brown	
	1468	(P/D)	Teledyne	No foldover current limit feature.
	MIOP42109	(P/F)	Micropac	
PA19	None known			
PA21	None known			
PA25	OPA2541	(P/D)	Burr-Brown	Higher Vsat, higher cost, more distortion, higher supply voltages, wider bandwidth.
PA41	None known			
PA51	OPA501	(P/F)	Burr-Brown	
	MIOP42106	(P/F)	Micropac	
PA61	None known			
PA77	None known			
PA81J	3581J	(P/F)	Burr-Brown	
PA82J	3582J	(P/F)	Burr-Brown	
PA83	3583	(P/D)	Burr-Brown	Supplies down to +/-50V only.
PA84	3584	(P/D)	Burr-Brown	Slightly slower; supplies down to ±70V only.
PA85	None known			
PA88	None known			
PA89	None known			
PB50	None known			
PB58	None known			
WA01	None known			
WB05	None known			

APEX ALTERNATIVES FOR EXISTING DESIGNS

BURR-BROWN

OPA501	PA51	(P/F)	Slightly improved thermal performance for all grades.
	PA61	(P/D)	Supplies to ±45V; lower Vsat, Lower Vos.
OPA511AM	PA01	(P/D)	Lower cost; slightly higher Vos and Vsat
	PA10	(P/D)	Supplies to ±45V; lower Vos; faster; slightly higher cost.
OPA512BM	PA12	(P/F)	
OPA512SM	PA12A	(P/F)	
OPA541			Apex alternatives provide: independent setting of ± current limits; lower distortion, except on class C units; PC layout could accommodate alternates easily except for PA02. Two grades of OPA541 are FET input amplifiers with 1 and 10 mV of input offset. Both have max DC thermal resistance of 1.9 C/W.
	PA02	(F/E)	Lower Vsat; higher speed; Vos = 3 and 10mV; thermal resistance is 2.6 C/W.
	PA10	(P/D)	Bipolar Vos = 3 and 6 mV, thermal resistance is 2.6 C/W.
	PA61	(P/D)	Bipolar Vos = 3 and 6 mV; thermal resistance is 1.8 C/W; class C output stage.
	PA51	(P/D)	Bipolar Vos = 5 and 10 mV; thermal resistance is 1.8 C/W; class C output stage.
	PA12	(P/D)	Bipolar Vos = 3 and 6 mV; thermal resistance is 1.4 C/W; fully tested to 10A or 15A.
	PA07	(P/D)	FET Vos = 0.5 and 2 mV; thermal resistance is 2.6 C/W; supplies to ±50V; includes thermal shutdown.

EQUIVALENT/SECOND SOURCES

BURR-BROWN (continued)

OPA2541	PA25	(P/D)	Supplies to ±20V only; lower Vsat; lower cost; lower distortion.
3554	WA01	(P/D)	External comp not used on WA01; higher performance; higher output current capability; 4x slew rate; higher cost.
3571, 72			PC layout could accommodate Apex alternates easily.
	PA07	(P/D)	Higher voltage, power dissipation, frequency response.
	PA01	(P/D)	Supplies to ±28V; bipolar input; very low cost.
	PA10	(P/D)	High performance bipolar input; supplies to ±50V; much lower cost than 3572.
	PA12	(P/D)	Output currents to 15A; supplies to ±50V; high performance bipolar input.
	PA61	(P/D)	Output currents up to 10A; bipolar input; class C output; lower cost than 3572.
3573	PA73	(P/F)	
3580-83	PA83	(P/F)	Extends the best specs of each model through the entire voltage range.
3581J	PA81J	(P/F)	Recommend PA41 for any new design of 3580-3583 series.
3582J	PA82J	(P/F)	
3583AM	PA83	(P/F)	
3583AMQ	PA83Q	(P/F)	
3583J	PA83	(P/F)	
3584JM	PA84	(P/D)	Slightly faster, improved phase margin, higher current; APEX temperature range is -25 to +85°C.

INTERSIL

8510, 15	PA01	(F/E)	All Apex current models offer more power and several offer
8520, 30	PA07	(F/E)	accuracy improvements. The models listed here are 5A, 67W devices. All are 8 pin TO-3 packages.

MICROPAC

42105	PA73	(P/F)	
42106	PA51	(P/F)	
42109	PA12	(P/F)	

NATIONAL

LH0063	WB05	(P/D)	PC layout could accommodate either part; sleep mode feature; no offset adjust; 3x slew rate under load; 4x output current capability.
LH0101	PA02	(P/D)	PA02 swing enhancement network is internal; PC layout can often accept either part; isolated case; better speed and linearity; ±19V supplies max.
LM12	PA02	(F/E)	Often has efficiency advantages on applications up tp ±19V due to low Vsat at 5A or less.
	PA07	(F/E)	Lower Vos; adjustable Vos balance; supplies to ±50V; output currents to 5A.
	PA10	(F/E)	Lower Vos; supplies to ±45V and ±50V; 5A output current.
	PA61	(F/E)	Lower Vos; supplies to ±45V; 10A output current; low Iq; class C operation.
	PA12	(F/E)	Lower thermal resistance; lower Vos; supplies to ±45V or ±50V; 10A or 15A output currents.

TELEDYNE

1460	PA09	(P/D)	Faster and considerably more powerful.
1461	PA09	(F/E)	Slower but more powerful.
1468	PA12	(P/D)	PC layout could accommodate both parts; PA12 offers foldover current limit.
1480	PA83	(P/F)	
	PA84	(P/D)	Faster; external compensation; lower output current; PC layout could accommodate either part.

NOTES: (P/F) = Pin for pin compatible—form, fit and functional replacement
(P/D) = Pin for pin compatible—major performance differences noted
(F/E) = Functional equivalent—not pin for pin compatible—major differences noted

GENERAL OPERATING CONSIDERATIONS

GENERAL OPERATING CONSIDERATIONS

SAVE HOURS OF VALUABLE TIME

This applications information is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. We highly recommend that you take the small amount of time required to read this section so that you can avoid the common pitfalls in designing and testing power operational amplifier circuits. As a minimum, you should read all *oblique print* and the first paragraph in each numbered subsection. The majority of these problem areas have been identified from APEX Applications Hotline discussions of actual circuits. They range from higher than expected errors to total destruction of the amplifier.

1.0 ELECTROSTATIC DISCHARGE (ESD) PRECAUTIONS

All APEX amplifiers should be handled using proper ESD precautions! MOSFET amplifiers are especially susceptible to ESD damage and many of our amplifiers are MOSFET designs. Most of our bipolar designs use small geometry transistor input stages, which are vulnerable to ESD.

ESD damage causes a wide range of effects, from increased voltage offset or bias currents to total destruction. APEX manufactures its products in a tightly controlled, anti-static environment and ships its products in anti-static packaging. Strict ESD precautions from receiving inspection through final assembly at your facility must be adhered to. Some areas which will require ESD prevention measures include personnel, tabletops, stocking containers, floors, soldering irons, and test equipment.

2.0 BEFORE YOU APPLY POWER

In the design/prototype phase of an application, many dangers exist which will be eliminated by the time the circuit is ready for production. Pins may be wired in reverse order, connections may be missing, or test probes may cause momentary shorts. Any of these can destroy power amplifiers or other components in short order.

Five procedures can be employed to substantially reduce these dangers:

1) *Set power supplies to the minimum operating levels allowed by the data sheet.*
2) *Set current limit to very low levels* (i.e. use a current limit resistor of approximately 2.2 ohms for high current models and 47 ohms for high voltage models). Consult Section 5, **"Current Limit,"** as well as the individual data sheet to determine the proper values for the current limit resistor(s). *Do not depend on the variable current limit feature of your lab power supply for protecting the amplifier.*

   It is much safer to install current limit resistors. Setting the current limit to a low value on a commercial lab supply will not protect the amplifier against the surge current available from the output filter capacitors. Even when average power dissipation is low, SOA violations can occur due to secondary breakdown of bipolar output stages. This mode of output stage destruction results from simultaneous application of high current and voltage to the conducting transistor. See Section 6 on SOA and the individual data sheets to better understand SOA limits.
3) *Check for oscillations.* With low voltage applied and reduced current limits in place, set the input signal to zero and connect a wide bandwidth (100 MHz or greater) oscilloscope to the output of the op amp. With the time base set to the microsecond region, check for oscillations present at any amplitude settings. Next, inject a signal into the circuit and monitor the output for oscillations. Excessive ringing on small signal square wave response indicates marginal stability.

   If an oscillation is found, measure the frequency and amplitude of oscillation. Also note whether the oscillation only shows up on the positive or negative half of the output. Refer to Section 10, **"Stability,"** for diagnosing and fixing the cause of instability.

   With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions, i.e. motor reversal, square wave drive of reactive loads, or driving the output to $V_S/2$ for resistive loads. Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific voltages and power levels.
4) *Use the largest possible heatsink for your prototype work.* This precaution provides the best environment to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations, you may decide to use a smaller heatsink for your final circuit. Consult Section 7, **"Internal Power Dissipation And Heatsinking,"** for information on calculating heatsink requirements for your application.
5) *Avoid switching while the circuit is under power.* This includes plugging/unplugging banana jacks, switching relays in high current lines, switching within a feedback loop, etc. See Sections 9.1 and 9.3 for a further discussion of the dangers of switching.

3.0 ABSOLUTE MAXIMUM SPECIFICATIONS

Amplifiers should always operate below their Absolute Maximum Ratings to prevent permanent damage. If operation results in one of these maximums being reached, no permanent damage will result. *Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier.* Note that proper operation is only guaranteed over the ranges listed in the Specifications table.

Example: Most amplifiers have an Absolute Maximum case temperature rating of +125°C. If the Specifications table gives an operating temperature range of up to +85°C, then the parameter limits in the Specifications table are not valid between +85°C and +125°C. In addition, the amplifier may not even be operational in this range, (for example, the amplifier may latch to one of its supply rails when above +85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area.

The absolute maximum power dissipation rating used by APEX is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, it is not a reasonable operating point because it requires an ideal (infinite) heatsink. Furthermore, even with the best heatsink, *sustained operation at the maximum rated junction temperature will result in reduced product life.* Refer to Section 7, **"Internal Power Dissipation And Heatsinking,"** for information regarding operating junction temperatures and relative product life. APEX generally recommends operating at a case temperature that keeps maximum junction temperatures at 150°C or below.

Absolute Maximum Common Mode Voltage is another rating that illustrates the difference between the rated absolute maximum and the specified operating range. On many amplifiers, the rated absolute maximum voltage applied to both inputs simultaneously is equal to the power supply voltage. However, the linear operating range is 5V to 10V less than each power supply rail. This means that inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, may start to distort the signal, or could even latch the output to one of the supply rails.

For more information on specifications and limits, see Section 9, **"Amplifier Protection And Performance Limitations,"** Section 6, **"SOA,"** Section 4, **"Power Supplies,"** and the **"Parameter Definitions"** section of the handbook on pages B9-B10.

4.0 POWER SUPPLIES

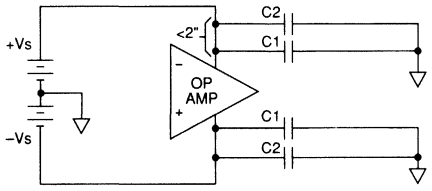
4.1 VOLTAGE SPECIFICATION

The specified voltage (±Vs) applies for a dual supply having equal voltages (±30V). An asymmetrical (+50V/–10V) or a single supply (60V) may be used as long as the total voltage between +Vs and –Vs does not exceed the maximum rating.

4.2 POWER SUPPLY BYPASSING

Inadequate power supply can lead to power amplifier circuit oscillations. Each supply pin should be bypassed to common with a "low frequency bypass" capacitance of 10µF per Ampere of peak output current. Tantalum capacitors should be used, although computer grade aluminum electrolytics can be substituted for operating temperatures above 0°C.

In addition, a "high frequency bypass," .1µF to .22µF ceramic capacitor, should be added in parallel with the low frequency bypass capacitors from each supply rail to common. Refer to Figure 1. In cases where supply line inductance is high, it may be necessary to add 1 to 10 ohms of resistance in series with the "high frequency bypass" to dampen the Q of the resulting LC tank circuit. Refer to Figure 1.



C1 = .1 to .22 µF, Ceramic Disk, High Frequency Bypass
C2 = 10µF/Amp out (peak), Electrolytic/Tantalum, Low Frequency Bypass

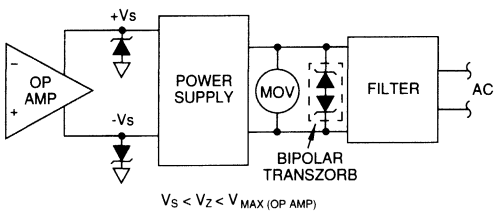
FIGURE 1. POWER SUPPLY BYPASSING

4.3 OVERVOLTAGE PROTECTION

The amplifier should not be stressed beyond its Absolute Maximum supply voltage rating. The amplifier should be protected against any condition that may lead to this voltage stress level. Two common sources of overvoltage are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply and AC main transients passing through a power supply to appear at the op amp supply pins.

Transient suppressors with a voltage rating greater than the maximum power supply voltage expected but less than the breakdown voltage of the amplifier will prevent the amplifier from damage. For low energy, slow rise-time transients, ordinary zener diodes may be used. For faster, higher energy, or higher duty cycle transients, TranZorbs (General Semiconductor Industries) may be used. TranZorbs function like a fast turn-on zener diode.

Transients from the AC mains can be clamped through the use of MOVs (Metal Oxide Varistors) such as those made by General Electric, or bipolar TransZorbs. Connect either of these devices across the inputs to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors used in power supply filters will pass all high frequency energy and capacitors used in the filter are usually electrolytics which have high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will pass on through the capacitor with little reduction. Refer to Figure 2.



$V_S < V_Z < V_{MAX\ (OP\ AMP)}$

FIGURE 2. OVERVOLTAGE PROTECTION

5.0 CURRENT LIMIT

The primary function of current limit is to keep an amplifier within its SOA. See Section 6, **"Safe Operating Area."** Some models of Apex Power Op Amps have an internal current limit, while most of our models have an adjustable limit that is set with one or two external resistors.

5.1 CURRENT LIMIT PRECISION

Standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow ±20% variation at room temperature. Furthermore, the current limit varies over temperature. This temperature dependence is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the current limit equation given in Section 5.3 with –2.2mV per degree (Centigrade) of case temperature rise above 25°C. For example, at a case temperature of 125°C, this term becomes 0.43V rather than 0.65V; (650mV–(125°C–25°C)(–2.2mV)). When working with high currents, the impedance of PCB traces, lead lengths and solder joints must be included in the current limit calculations.

5.2 EXTERNALLY ADJUSTABLE CURRENT LIMIT

Models with provisions to adjust current limit externally must have the current limit resistors connected as shown in the external connection diagram.

Current limit should never be set at a value greater than the rated maximum output current of the power op amp. This maximum is due to the current density limitations of conductors in the package and exceeding it can destroy the amplifier. Also, using a very low resistance (such as a jumper wire) will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to secondary breakdown, thereby destroying reliability.

Operation without current limit resistors installed (current limit pins left open) can also cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for the high voltage, low current series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors.

5.3 CALCULATING CURRENT LIMIT

Power op amps with provisions to adjust current limit externally require one or two current limit resistors (R_{CL}) which must be connected as shown in the applicable external connection diagram below. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Each resistor and its power dissipation is calculated as follows:

$$R_{CL}\ (\text{ohms}) = \frac{0.65}{I_{LIM}\ (A)} - 0.01\ ^*$$

$$PR_{CL}(\text{watts}) = 0.65 \cdot I_{LIM}$$

* .01 ohms = wire bond and pin resistance

I_{LIM} is the value of current limit desired and should be chosen to provide the amount of protection required for the specific application. For details on choosing "safe" levels of current limit and the protection/performance trade offs involved, see Section 6.3, **"Fault Protection Using Current Limit."**

For two resistor current limit schemes, asymmetrical current limiting ($R_{CL+} \neq R_{CL-}$) is permissible. For testing without a heatsink, the resistors should be selected to limit power dissipation in the amplifier to less than 3W under short circuit conditions.

Foldover current limit, discussed in detail in AN #9, Foldover Current Limiting, provides a lower current limit for short circuit conditions while increasing current limit for load drive. Two APEX power amplifiers, the PA10 and PA12, have this feature. Foldover reduces the protection/performance trade-off inherent in setting current limit.

6.0 SAFE OPERATING AREA (SOA)

6.1 READING THE SOA GRAPH

The horizontal axis on the SOA curve, $V_S–V_O$, defines the voltage stress across the output device that is conducting. It does *not* define a supply voltage or total supply voltage or the output voltage. $V_S–V_O$ is the

magnitude of the differential voltage from the supply to the output across the transistor that is conducting current to the load. Put another way: if the amplifier is sourcing current, use $(+V_S)-V_O$. If the amplifier is sinking current, use $(-V_S)-V_O$. Refer to Figures 3a & 3b.

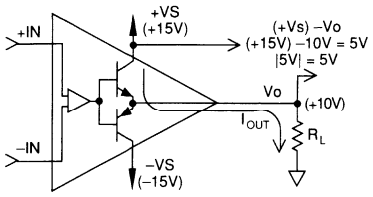


FIGURE 3A. *SOURCING* CURRENT

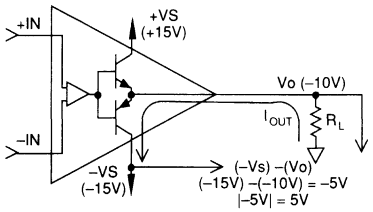


FIGURE 3B. *SINKING* CURRENT

The vertical axis represents the current that the amplifier is sourcing or sinking through the Output pin.

The Safe Operating Area curves show the limitations on the power handling capability of the amplifier. Refer to Figure 4. There are three basic limitations:

1) *Current handling capability.* This horizontal line near the top of the SOA CURVE represents the limit on output current imposed by current density constraints in the wire bonds, die junction area and thick film conductors.
2) *Power dissipation capability.* This is the total power dissipation capability of the amplifier and includes power due to quiescent current as well as power dissipated in the output stage. Note that the product of output current on the vertical axis and $V_S–V_O$ on the horizontal axis is constant over this line. In other words, this portion of the SOA curve is a "constant power line." For $T_C = 25°C$, this line represents the maximum power dissipation capability of the amplifier at maximum junction temperature using an infinite heatsink. As case temperature increases, this constant power/thermal line moves toward the origin. The new constant power line can be determined from the Power Derating curves on the data sheet. The case temperature is primarily a function of the heatsink used. For more details, refer to Section 7, **"Internal Power Dissipation And Heatsinking."**
3) *Secondary Breakdown.* Secondary breakdown is a phenomenon exhibited by bipolar transistors when they are simultaneously stressed with high collector-emitter voltage and high collector current. Non-uniform current density in the emitter results in localized heating and "hot spots" at the junction. The temperature dependence of junction current results in increased current density at the hot spots. This concentration of current tends to further increase the temperature. The process is cumulative, leading to thermal runaway and transistor failure.

The transient secondary breakdown lines (t=0.5ms, t=1ms, and t = 5ms) are based on a 10% duty cycle. For instance, in Figure 4, the amplifier may deliver 1.5A at a $V_S–V_O$ of 60V for 5ms but then must wait for 50ms before repeating this stress level. It is highly recommended to avoid entering the region beyond the DC secondary breakdown limits. Operation outside steady state limits in transient SOA regions is difficult to analyze adequately enough to insure best possible reliability. Note that MOSFET power transistors do not have this secondary breakdown limitation.

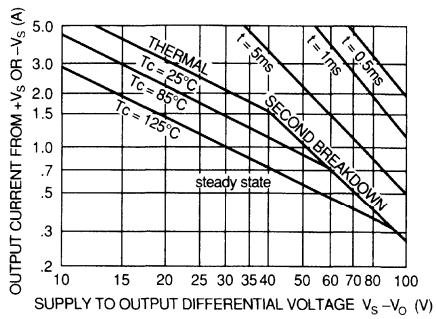


FIGURE 4. TYPICAL SOA CURVE

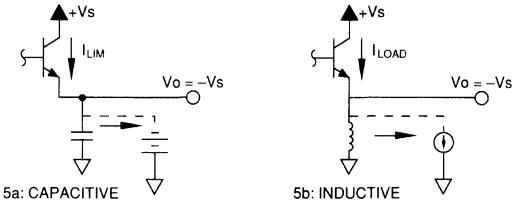
6.2 HIGH SOA STRESS CONDITIONS

For resistive loads tied to ground, calculating power dissipation in the amplifier is reasonably simple. Refer to Section 7.1, **"DC Power Dissipation,"** and Section 7.2, **"AC Power Dissipation."** However, with reactive loads, the voltage/current phase difference results in higher power being dissipated in the amplifier.

An example of an excessive transient stress condition created by a capacitive load is shown in Figure 5a. In this case the capacitive load has been charged to $–V_S$. Now the amplifier is given a "go positive" signal. Immediately the amplifier will deliver its maximum allowed output current (I_{LIM}) into the capacitor, which can be modeled at time t=0+ as a voltage source. This leads to a voltage stress across the conducting device equal to the rail-to-rail supply voltage. Simultaneously, the amplifier will be conducting its maximum (current-limited) value of current.

Figure 5b shows a similar transient stress condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the inductor has built up to some value I_{LOAD}. Now the amplifier is given a "go negative" signal which causes the output voltage to swing down to the negative supply. However, the inductor at time t=0+ can be modeled as a current source that requires the amplifier to continue to source I_{LOAD}. This leads to the same situation as before, that is, total supply voltage across a device conducting maximum rated current.

Note also that reactive loads cause higher thermal stress levels than resistive loads even under steady state sinusoidal conditions. *For purely reactive loads, all of the power is dissipated in the amplifier, none in the load.*



5a: CAPACITIVE 5b: INDUCTIVE

FIGURE 5. TRANSIENT STRESS WITH REACTIVE LOADS

6.3 FAULT PROTECTION USING CURRENT LIMIT

With a given supply voltage, current limit can be used to keep the amplifier within its Safe Operating Area. This allows amplifier protection during fault conditions such as shorts to ground or shorts to either supply. The cost of protection is lowered output current capability.

For short-to-ground fault protection, set current limit to the value given by the intersection of the supply voltage and the DC SOA curve for the appropriate case temperature. Simply find the supply voltage on the horizontal axis. When the output is shorted to ground, $V_O = 0$; therefore, $V_S–V_O = V_S$, follow up to the SOA curve intersection and then across to the output current. Referring to Figure 6, we see that in this example, a 2A current limit provides short circuit protection to ground at a case temperature of 25°C with ±30V supplies. Note that better heatsinking allows higher values of current limit.

For short-to-either supply protection, set current limit to the value given by the intersection of the rail-to-rail supply voltage (V_{SS}) and the

DC SOA curve. This requires a significant lowering of current limit. For this type of protection , add the magnitudes of the two supplies used, find that value on the V_S–V_O axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit. Referring to Figure 6, we see that in this example, a 0.7A current limit allows short protection to either supply.

It is often the case that requirements for fault protection and maximum output current may conflict. Under these conditions there are only four options. The first is to simply go to an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called "foldover" or "foldback." This is available on some amplifiers such as the PA10 and PA12. For a detailed discussion of foldover current limit and SOA fault protection refer to AN#9, **"Foldover Current Limiting."** For an explanation of how to choose current limit resistors to adjust current limit, see Section 5.3, **"Calculating Current Limit."**

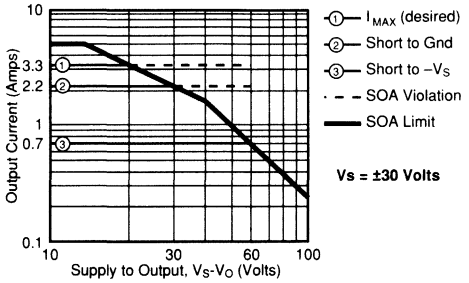


FIGURE 6. CURRENT LIMIT FAULT PROTECTION

7.0 INTERNAL POWER DISSIPATION AND HEATSINKING

It is important to not confuse Internal Power Dissipation with power delivered to the load. Internal dissipation is not equal to load dissipation except when the output voltage is 1/2 the supply voltage and the load is resistive. In this case the power dissipations are equal and internal power dissipation is at its maximum.

There are two main steps in the heatsink selection process. First, the maximum *internal* power dissipation must be calculated. Secondly, the maximum desired junction temperature must be chosen and the thermal model used to calculate the required thermal conductance of the heatsink.

7.1 DC POWER DISSIPATION

Calculating power dissipation in an amplifier under DC conditions with a resistive load is very simple. The first portion of power dissipation is the quiescent power, PD_Q, that the amplifier dissipates due to quiescent current and supply voltage. Multiplying total supply voltage by maximum quiescent current gives the value of this power dissipation:

$$PD_Q = I_Q (+V_S - (-V_S))$$

The second portion of internal power dissipation is developed in the output stage due to delivering load current. This output stage power, PD_{OUT}, is the output current times the voltage drop across the amplifier, V_S–V_O. For a resistive load, maximum power dissipation occurs at $V_O = 1/2V_S$ and has a value of:

$$PD_{OUT}(max) = \frac{V_S^2}{4R_L}$$

Refer to Figure 7 for the relationship between PD_{OUT} and V_O. The total internal power dissipation is simply the sum of these two components, or:

$$PD_{INT}(max) = PD_Q + PD_{OUT}(max)$$

7.2 AC POWER DISSIPATION

With an AC output and/or a reactive load, power dissipation calculations get quite a bit stickier. Several simplifying assumptions keep the problem reasonable for analysis. The actual internal dissipation can be determined analytically or through thermal or electrical bench measurements.

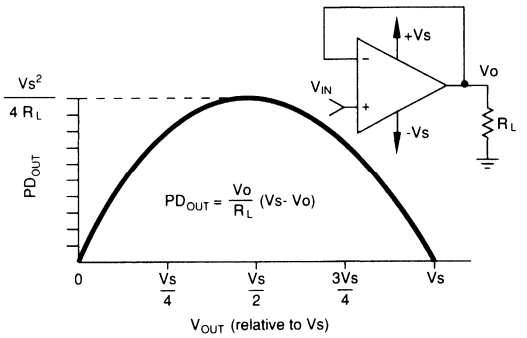


FIGURE 7. DC POWER DISSIPATION VS. OUTPUT VOLTAGE

ANALYTICAL APPROACH:

For analysis the following equations assume the use of symmetric power supplies and sinusoidal signals. In single supply applications, simplify by using equivalent symmetric split power supplies:

Purely resistive loads: $$PD_{OUT}max = \frac{2V_S^2}{\pi^2 R_L}$$

Primarily resistive loads: $PD_{OUT}max = \frac{2V_S^2}{\pi^2 Z_L \cos\theta}$ ($\theta < 40°$)

Primarily reactive loads: $PD_{OUT}max = \frac{V_S^2}{2Z_L}\left|\frac{4}{\pi} - \cos\theta\right|$ ($\theta > 40°$)

WHERE: $V_S = |V_S+|$ or $|V_S-|$ (symmetric supplies)
Z_L = Magnitude of load impedance
θ = Phase angle of load impedance

Refer to Figure 8 for the relationship between power dissipation and peak output voltage.

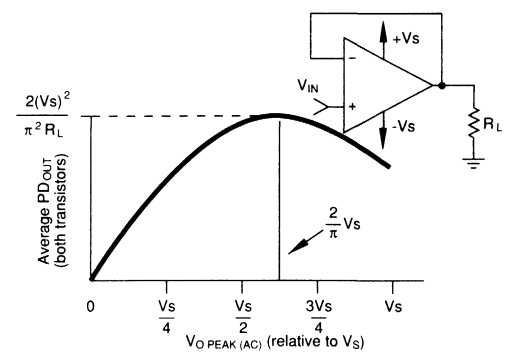


FIGURE 8. AC POWER DISSIPATION VS. PEAK OUTPUT VOLTAGE

THERMAL MEASUREMENT METHOD:

1) With no power applied, measure T_A, ambient temperature.
2) Using a resistive load, dissipate a known amount of power in the amplifier. For instance, set V_S–V_O to a DC value and calculate $P_{INT} = I_{LOAD}(V_S–V_O)$.
3) Measure $\Delta T = T_C–T_A$
4) Calculate $R_{\theta CA}$ from: $$R_{\theta CA} = \frac{\Delta T}{PD_{INT}}$$
5) Connect the load that you will use in your application and drive the amplifier with the typical signal for the application.
6) Measure the case temperature, T_C.
7) Calculate: $$PD_{INT} = \frac{T_C–T_A}{R_{\theta CA}}$$

ELECTRICAL MEASUREMENT METHOD #1:

1) Measure the power delivered TO the amplifier *from* the supply:

$$P_{IN} = \frac{2V_S I_{PEAK}}{\pi}$$

2) Measure the power delivered *from* the amplifier *to* the load:

$$P_{OUT} = (1/2)V_{PEAK}\, I_{PEAK}\cos\theta$$

3) Calculate power left in the amplifier:

$$PD_{INT} = P_{IN} - P_{OUT}$$

ELECTRICAL MEASUREMENT METHOD #2:

1) Use a small value current sense resistor between the load and ground to develop a voltage proportional to I_L. Use this signal to drive one channel of the X–Y display of an oscilloscope.
2) Use the output voltage of the amplifier, V_O, to drive the other channel of the X–Y display.
3) Calculate instantaneous power dissipation in the amplifier for several points on the ellipse using:

$$PD_{OUT} = (V_S - V_O)I_{LOAD}$$

4) Plot the points on the SOA curve and check for violations. Refer to Figure 9 for test set-up details.

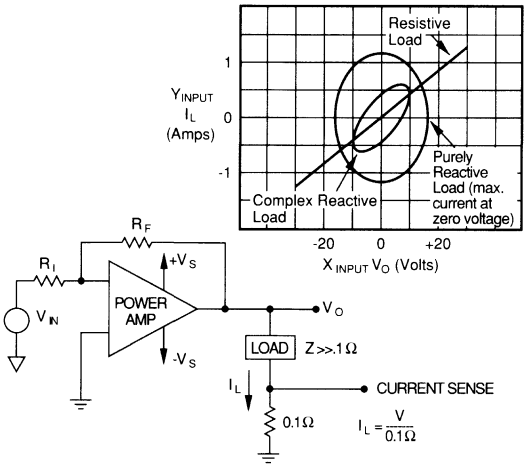


FIGURE 9. AC PD_{OUT} : ELECTRICAL MEASUREMENT METHOD #2

7.3 THERMO-ELECTRIC MODEL

The thermo-electric model, refer to Figure 10, translates power terms into their electrical equivalent. In this model, *power is modeled as current, temperature as voltage, and thermal resistance as electrical resistance.*

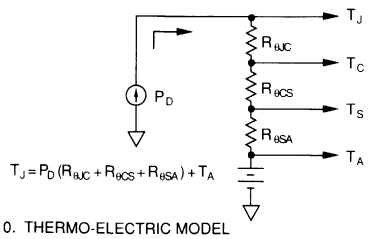
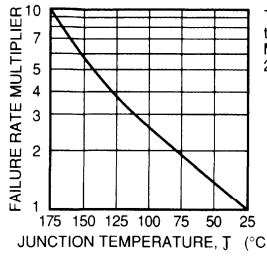


FIGURE 10. THERMO-ELECTRIC MODEL

Reliability is a strong function of junction temperature. Figure 11, from MIL-HDBK-217E, shows that a device with a junction temperature of 175°C will have a mean failure rate three times as high as a device with a junction temperature of 125°C.

There are two approaches to lowering junction temperature. The first is to reduce the internal power dissipation, and the second is to reduce the total thermal resistance.

Reducing power dissipation can be accomplished by reducing the supply voltage to no more than what is required to obtain the voltage swing desired. This reduces the $V_S - V_O$ quantity to as low a value as possible. Note from Figure 8 that as the output swing is raised above



This data was extracted from the base failure rate tables of MIL-HDBK-217E, revision of 27 October 1986

FIGURE 11. MTTF VS. TEMPERATURE

$2V_S/\pi$, power dissipation drops off significantly, approaching approximately 1/2 of maximum value as the output peak voltage approaches the supply voltage.

The thermal resistance problem should be attacked on all three fronts:

1) Buy an amplifier with the lowest possible $R_{\theta JC}$.
2) Use good mounting practices. See Section 8.0, **"Amplifier Mounting And Mechanical Considerations."**
3) Use the largest practical heatsink. See Section 7.4, **"Heatsink Selection."**

$R_{\theta JC}$, the thermal resistance from the semiconductor junction to the case of the amplifier, is characteristic of the amplifier itself. It is a function of the power die junction area, substrate material, attach method and package material. The way to obtain maximum reliability and cool junction temperatures is to buy an amplifier with as low a $R_{\theta JC}$ as affordable. This is usually a major portion of the total thermal resistance budget and reductions here result in significant reliability improvements. This parameter is also a function of frequency, with power sharing between the two output devices resulting in lower resistance at higher frequency.

$R_{\theta JC}$ is the thermal resistance from the case to a heatsink. This resistance can typically be kept down between 0.1 to 0.2°C/W if good mounting techniques are used. This includes using thermally conductive grease, properly torquing the package, and not using insulation washers. See Section 8.0, **"Amplifier Mounting And Mechanical Considerations,"** for details.

The final piece of the thermal budget is $R_{\theta SA}$, the thermal resistance from the heatsink to ambient air. This is a very crucial element and should not be skimped on. A quick glance at an SOA curve or a power derating curve will show the difference between power limitations of an amplifier with an 85°C case and a 125°C case. Clearly this shows the benefit of using the maximum heatsink allowable. One word of caution: published heatsink specifications can be used as a guideline, but actual performance depends significantly on a wide variety of variables. These include air flow, altitude, configuration, and mounting. It is best to verify thermal performance through measurement under operating conditions.

7.4 HEATSINK SELECTION

Power op amps can be operated without a heatsink only if the internal power dissipation is less than 5 watts at 25°C ambient. Five Watts times the typical $R_{\theta JA}$ of 30°C/W results in a junction temperature rise of 150°C. Adding in the 25°C ambient results in a junction temperature of 175°C.

The steps to selecting a heatsink are:

1) *Calculate the maximum internal power dissipation, PD_{INT}(max).* Sections 7.1 and 7.2 cover how to calculate PD_{INT}(max) for various applications.
2) *Determine the maximum junction temperature, T_J max, that will give the level of reliability required for your application.* See Section 7.3 for details of junction temperature versus MTTF.
3) *Use the appropriate thermal resistance of the amplifier* given on the product data sheet ($R_{\theta JC(DC)}$ or $R_{\theta JC(AC)}$) and the appropriate $R_{\theta CS}$ (typically 0.1 to 0.2°C/W for thermal grease). See Section 8.0, **"Amplifier Mounting And Mechanical Considerations."**
4) *Calculate the maximum allowable heatsink to ambient resistance,* $R_{\theta SA}$, from:

$$R_{\theta SA} \le \frac{T_J - T_A}{PD_{INT}(max)} - R_{\theta JC} - R_{\theta CS}$$

5) *Choose a heatsink with a $R_{\theta SA}$ lower than or equal to the calculated value.* Note that the calculation may give a value of $R_{\theta SA}$ that is too low to be attainable with commercially available heatsinks. It may even result in a negative number! If this happens, first make sure you aren't excessively "padding" your assumption values, then consider a higher allowable junction temperature or an amplifier with a lower $R_{\theta JC}$.

Example:

Given: PA02 Power Op Amp
$\pm V_S = \pm 18V$
$R_L = 4$ Ohms
$T_A = 25°C$
Application frequency: DC to 5 kHz
Find: APEX heatsink

1) From Section 7.1, DC power dissipation is:

$$PD_{INT}(max) = PD_Q + PD_{OUT}(max)$$

$$= I_Q(V_S+ - V_S-) + \frac{V_S^2}{4R_L}$$

$$= 37mA(36V) + \frac{(18V)^2}{4(4\ ohms)}$$

$$PD_{INT}(max) = 21.6\ Watts$$

2) For conservative design, keep $T_J \leq 125°C$.
3) PA02 data sheet gives $R_{\theta JC\ MAX}$, DC as 2.6°C/W. For conservative design, use 0.2°C/W as $R_{\theta CS}$.
4)

$$R_{\theta SA} \leq \frac{T_J - T_A}{PD_{INT}(max)} - R_{\theta JC} - R_{\theta CS}$$

$$\leq \frac{(125-25)°C}{21.6W} - 2.6°C/W - 0.2°C/W$$

$$R_{\theta SA} \leq 1.8°C/W$$

5) Select APEX HS03; $R_{\theta SA} = 1.7°C/W$.
Refer to **"Package and Accessories Information"** section of APEX Amplifier Handbook.

8.0 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

For Power Op Amp designs, high reliability consists of mechanical considerations as well as electrical considerations. Proper mounting is very important for power amplifiers. Once the proper heatsink has been selected as described in Section 7.4, the following mounting techniques should be used.

All APEX amplifiers have an electrically isolated case. This means that mica insulating washers are not necessary and ***should not be used.*** Mica washers are for electrical insulation and therefore are unnecessary. In addition, they raise thermal resistance by as much as 1°C/W, seriously degrading reliability.

In addition, APEX uses a thin beryllia substrate to get the lowest possible thermal resistance. While this leads to cool running, high reliability amplifiers, it is important not to run the risk of cracking this substrate. In order to prevent this, two major precautions must be observed:

1) *Do not use compressible thermal washers.* These are silicon rubber based pads such as Silpad. The amount of compressibility in a washer over 2 mil thick can lead to header flexing, which can crack the substrate. Also, thermal grease has superior thermal properties.
2) *Do not over torque the case. Recommended mounting torque for the TO-3 8-Pin package is 4-7 in-lbs (.45-.79 N-m) and for the Power Dip™ packages (PD10 AND PD12) is 8-10 in-lbs (.90-1.13 N-m).* Refer to Figure 12. Apply a thin, uniform film of thermal grease between the case and heatsink. Apply small increments of torque alternately between each screw when mounting the amplifier.

Due to dimensional tolerances between heatsink thru-holes and power op amp packages, extreme care must be taken not to let the pins touch the heatsink inside the thru-holes. *Do not count on the anodization for insulation* as it can nick easily, exposing bare aluminum, an excellent electrical conductor. *Use teflon tubing to sleeve at least two opposite pins* if you are using a mating socket or printed circuit board. If you are wiring directly to the pins, it is best to sleeve all pins. *Refer to the Package and Accessories Information section of the Hybrid & IC Handbook for further details on sleeving sizes, mating sockets and cage jacks for PC board mounting of power amplifiers.*

Never drill out the entire area inside the pin circle, drill individual holes for each pin. Often, heatsinking is accomplished with a custom heatsink or by directly mounting to a bulkhead. These approaches require the use of heatsink thru-holes for the amplifiers pins. For the 8-Pin TO-3 package, the main path for heat flow occurs inside the circumference of 8 pins. Refer to Figure 13. Therefore, a single, large hole, to allow the 8 pins to pass through, will remove the critical heatsinking from where it is most needed. Instead, 8 separate #46 drill size holes must be drilled.

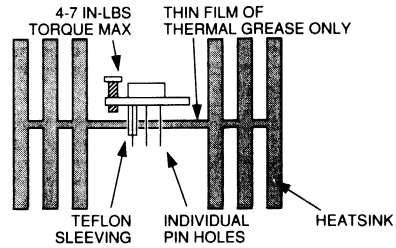


FIGURE 12. MOUNTING CONSIDERATIONS

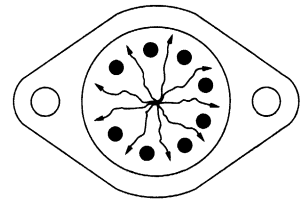


FIGURE 13. MAIN HEAT FLOW PATH: 8-PIN TO-3 PACKAGE

9.0 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

9.1 OUTPUT PROTECTION

Attempting to make sudden changes in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. Brush type DC motors can produce continuous trains of high voltage, high frequency kickback spikes. In addition, mechanical shocks to a piezo-electric transducer will cause it to generate a voltage. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes should not be counted on to protect the amplifier against sustained high frequency, high energy kickback pulses. Many of these diodes are intrinsic "epi" diodes that occur as a result of the manufacture of the power darlington output transistor. Epi diodes generally have slow reverse recovery times and may have large forward voltage drops. *Under sustained high energy flyback conditions, high speed, fast reverse recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes.* See Figure 14. These fast recovery diodes should have reverse recovery times of less than 100 nanoseconds and for very high frequency energy should be under 20 nanoseconds.

One other point to note is that the power supply must look like a true low impedance source when current flows in the opposite direction from normal. Otherwise, the flyback energy, coupled back into the supply pin, will merely result in a voltage spike at the supply pin of the op amp. This would lead to an overvoltage condition and possible destruction. Refer to Section 4.3 for information on overvoltage protection.

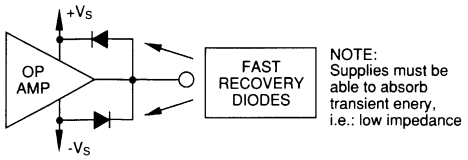


FIGURE 14. OUTPUT PROTECTION

9.2 COMMON MODE VOLTAGE LIMITATIONS

One of the most widely misunderstood parameters on an op amp data sheet is the *Common Mode Voltage Range*, which specifies how close an input voltage *common to both inputs* may approach either supply rail. *When these limits are exceeded, the amplifier is not guaranteed to perform linearly. The Absolute Maximum Common Mode Voltage* specification on most data sheets refers to the voltage above which *the inputs may not exceed or damage will result to the amplifier.*

There are two cases which clearly illustrate the constraints of common mode voltage specifications: single supply operation and asymmetrical supply operation.

Example:

The APEX PA82J has a Common Mode Voltage Range of ±Vs – 10. This implies that if the PA82J is to be operated from a single supply, both inputs must be biased at least 10 volts above ground. Figure 15 illustrates an implementation of this which keeps both inputs above 10 volts for the given range of input voltages. Note that for single supply operation, the output of the amplifier is never capable of swinging all the way down to ground. This is due to the output saturation voltage of the amplifier.

Figure 16 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage source allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar supply. As long as the amplifier remains in the linear region of operation, the common mode voltage will be zero. With the 12V supply the allowed positive common mode voltage range is from 0 to 2V. Note the output of the PA81J can swing all the way to zero now also. The 12V supply in this case need only supply the quiescent current of the power op amp. If the load is reactive or EMF generating, the low voltage supply must also be able to absorb the reverse currents generated by the load.

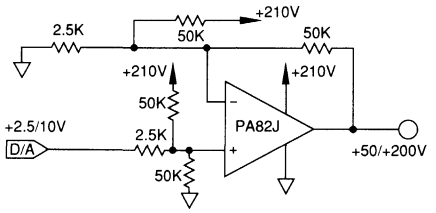


FIGURE 15. SINGLE SUPPLY OPERATION: V_{CM} CONSIDERATIONS

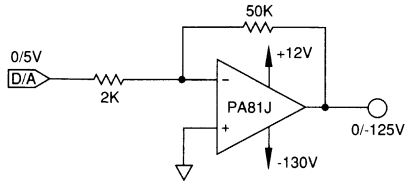


FIGURE 16. NON-SYMMETRICAL SUPPLY OPERATION

9.3 DIFFERENTIAL INPUT VOLTAGE LIMITATIONS AND PROTECTION

Exceeding the Absolute Maximum Differential Input Voltage specified on the data sheet can cause permanent damage to the differential input stage. Failure modes range from increased V_{OS} and V_{OS} drift, I_B and I_B drift, and input offset current, up to input stage destruction. Although the differential input voltage (V_{ID}) under normal closed loop conditions is microvolts, several conditions can cause it to be in the Volt range. Causes of V_{ID}:

1) Fast rise-time inputs.
2) Signal input while not under power.
3) High impedance output states (current limit, thermal shutdown, sleep mode).
4) Switching within the feedback loop.

An example of condition 4 is shown in Figure 17a. This configuration is often used in ATE systems for changing the gain of an op amp. The amplifier's full scale transition time (microseconds) is faster than the typical relay switching time (milliseconds); therefore when the relay opens the feedback loop, the Aol of the amplifier will drive the output to one of the supply rails. In the example shown, the output will approach 150V while the relay is still switching. Because the 100K feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the input. Since the Absolute Maximum V_{ID} for the PA08 is ±50V, the input stage that will be destroyed.

Effective input protection networks provide two functions:

1) Limit differential voltage to less than the reverse breakdown voltage of the input transistors base-emitter junction, typically ~6V.
2) Limit input transient current flow to less than 150mA.

Figure 17b shows an example of an input V_{ID} protection network. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

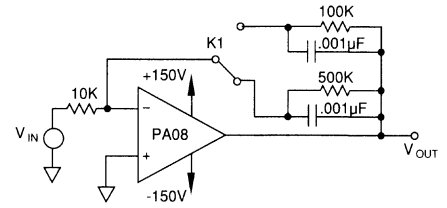


FIGURE 17a. GAIN SWITCHING AND V_{ID} *VIOLATION*

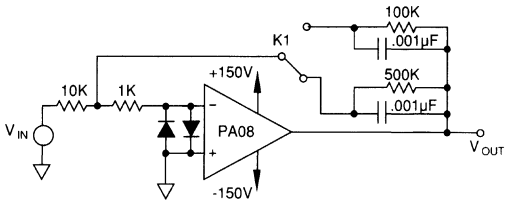


FIGURE 17b. GAIN SWITCHING AND V_{ID} *PROTECTION*

10.0 STABILITY

The most common application problem when working with power op amps is stability. Although most power op amps are compensated for unity gain stability, they are frequently required to drive reactive loads, deliver high currents, or use high impedances due to high voltage. These conditions make stability more difficult to achieve. However, EVERY circuit can be stabilized if the guidelines given here are followed. Table 1 provides a troubleshooting guide for stability problems. The **"Probable Cause / Possible Solution Key"** gives insight into the origin of the problem and provides guidance as to the appropriate fix.

CONDITION AND PROBABLE CAUSE TABLE fosc Oscillation Frequency	Oscillates unloaded?	Oscillates with V_{IN} = 0?	Loop Check† fixes oscillation?	Probable Cause(s) (in order of probability)
CLBW ≤ f_{osc} ≤ UGBW	N	Y	N	A, C, D, B
CLBW ≤ f_{osc} ≤ UGBW	Y	Y	Y	K, E, F, J
CLBW ≤ f_{osc} ≤ UGBW	–	N	Y	G
f_{osc} ≤ CLBW	N	Y	Y	D
f_{osc} ≈ UGBW	Y	Y	N*	J, C
f_{osc} << UGBW	Y	Y	N	L, C
f_{osc} > UGBW	N	Y	N	B, A
f_{osc} > UGBW	N	N**	N	A, B, I, H

CLBW = Closed Loop Bandwidth
UGBW = Unity Gain Bandwidth
† See Figure 18 for loop check circuit.
— Indeterminate; may or may not make a difference.
*Loop check (Figure 18) will stop oscillation if Rn << |Zcf| at UGBW.
**Only oscillates over a portion of the output cycle.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 4.2.
B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 4.2.
C. Cause: Ground loops.
Solution: Use **"Star"** grounding. See Figure 19.
D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use input R–C compensation network. See Section 10.2.1 .
E. Cause: Inductor within the feedback loop (noise gain zero).
Solution: Use alternate feedback path. See AN#5, **"Precision Magnetic Deflection,"** or AN#13, **"V–I Conversion."**
F. Cause: Input capacitance reacting with high R_F (noise gain zero).
Solution: Use Cf in parallel with Rf. (Cf =~Cin). Do not use too much Cf, or you may get problem J.
G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate R_B (the bias current compensation resistor from –IN to ground)
H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output **"snubber"** network. See Section 10.2.3 .
I. Cause: **"Composite PNP"** output stage with reactive load.
Solution: Use output **"snubber network."** See Section 10.2.3 .
J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce Cf and/or increase Cc for unity gain stability.
K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase Cc or increase gain and/or use input R–C compensation network. See Section 10.2.1.
L. Cause: Servo loop stability problem.
Solution: Compensate the **"front end"** or **"servo amplifier."**

10.1 BASICS OF STABILITY

Some basic practices must be followed to ensure stability. Proper ground practices are mandatory and are illustrated in Figure 19. Improper grounding can lead to oscillations near the unity gain bandwidth frequency of the amplifier. Proper bypassing of power supplies is also illustrated in Figure 19. The local bypassing close to the amplifier with a small electrolytic and ceramic capacitor insure good high frequency grounding of the supply lines. The internal phase compensation on op amps will be referred to one of the supply lines and this is the reason for the importance of good local bypassing.

10.2 METHODS OF CONTROLLING OSCILLATIONS

10.2.1 INPUT R-C NETWORK COMPENSATION

The first method for stabilizing an oscillating amplifier is shown in Figure 20.

The basic theory of an oscillator states that there must be sufficient gain and sufficient feedback to sustain oscillation. This connection is intended to attenuate feedback more than the open loop gain at the frequency of oscillation.

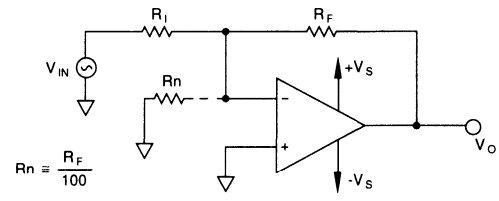


FIGURE 18. LOOP CHECK CIRCUIT

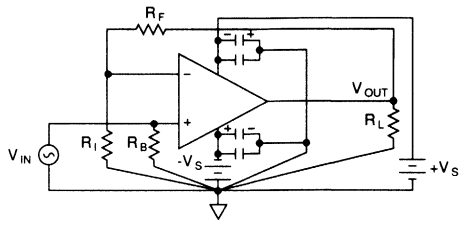


FIGURE 19. BASIC REQUIREMENTS FOR STABILITY

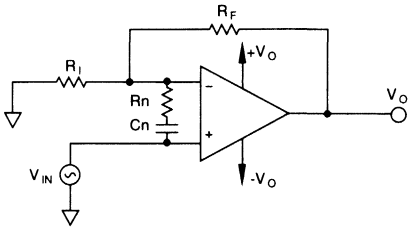


FIGURE 20. INPUT R-C NETWORK COMPENSATION

The question is often asked about why a capacitor from output to inverting input is used. This is often a result of trying that technique and noting that oscillation stopped. Oscillation with the complementary output power op amp is most often the result of capacitive effects in the load and the accompanying phase lag. Certain values of feedback capacitance will create a phase lead in the feedback that will compensate the load caused lag. The problem is that this is a matching condition that will not always correctly match over a wide range of devices and operating conditions. This also creates an increase in high frequency feedback. This is not the most reliable method to achieve stability. This technique is most useful in high speed amplifiers to compensate for input capacitance effects and achieve best settling time.

The R-C across the inputs can compensate for just about any type of condition causing loop instability, either inductive or capacitive. The R-C network is intended to provide simple resistive attenuation of the feedback. If the wrong values are used, the R-C network could be reactive at high frequencies and introduce additional phase lag into the feedback. This will aggravate oscillation problems. Two methods will be shown for selecting the component values:

GRAPHICAL METHOD (Refer to Figure 21)

1) Measure or predict f_{OSC}.
2) Determine Aol, f_{OSC}, Aol at f_{OSC} (from amplifier **"small signal response"** curve)
3) Set ratio of R_F/Rn = 10 x Aol_{fosc}
4) From **"small signal response"** curve, find f_{INT} at gain of R_F/Rn.
5) Select Cn such that: $f_{3dB} = f_{INT}/4$

$$Cn = \frac{4}{2\pi Rn\, f_{int}}$$

Example. (Refer to Figure 21)
Given: PA07 power op amp; R_{OUT} = 2.25 ohms
Capacitive load C_L = 700nF; R_F = 10KΩ, R_I = 10KΩ; noninverting gain of 2 (Refer to Fugure 21)

Find: Input R-C compensation network for stability.

Graphical Method:

R_{OUT} and C_L form an additional pole in the PA07 Aol.

1) Plot Acl on modified Aol. f_{OSC} will occur at approximately 200kHz, using rate of closure stability criteria.
2) Aol_{FOSC} = 18dB = gain of 7.9
3) $R_F/Rn = 10\ Aol_{FOSC}$
   $10K/Rn = 10 \times 7.9 = 79 = 38dB \longrightarrow Rn = 127\Omega$
4) f_{INT} at 38dB = 11kHz
5) $Cn = \frac{4}{2\pi Rnf_{int}} = \frac{4}{2\pi\ (127\Omega)\ (11kHz)} = 456nF$

$f_{3dB} = f_{int}/4 = 11kHz/4 = 2.75kHz$

Before input R-C compensation was added bandwidth was about 200kHz, but system oscillated. After input R-C compensation was added, bandwidth was about 11kHz and system was stable. Using the rate of closure criteria for stability, one can reiterate and trade off R_F/Rn with f_{3dB} for improved bandwidth.

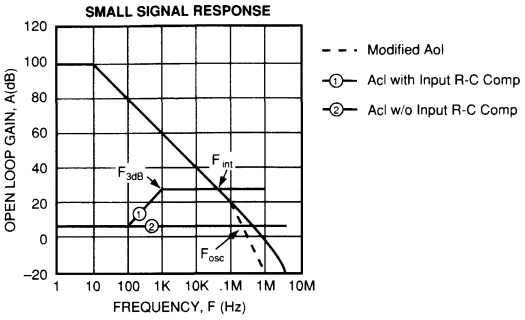


FIGURE 21. INPUT R-C COMPENSATION: GRAPHICAL METHOD

EMPIRICAL OR BENCH METHOD:

1) Use large resistance between ± inputs; reduce until oscillation stops.
2) Introduce a capacitor in series with resistor. If oscillation resumes, increase capacitor until it ceases. If oscillation doesn't occur, decrease capacitor until it does; then increase capacitor just enough to stop oscillation.

Note: Input R-C Compensation network will only solve local loop stability problems and not power supply bypassing or other sources of instability!

10.2.2 CAPACITIVE LOAD ISOLATION

The inductor in series with the output serves to isolate the amplifier circuit from capacitor loading. The feedback should be taken prior to the inductor. Refer to Figure 22. The inductor is a small value, generally from 5 to 10 microhenry, wound from heavy gauge wire. The inductor may be paralleled with a resistor, from 5 to 100 ohms, to kill any resonance effects.

This technique is similar to using a resistor in small-signal op amp designs to accomplish the same function. The inductor is used to reduce power losses to a minimum over the useful frequency band.

10.2.3 OUTPUT SNUBBER NETWORK

Hybrid complementary output amplifiers won't usually oscillate as a result of inductive loading. This is one of the advantages of a full complementary output stage. Asymmetrical output stages, such as those required in monolithic power amplifiers, do not have this luxury. Usually oscillations due to this will occur at frequencies beyond the unity gain bandwidth of the amplifier. Compensation for this is a simple R-C from output to ground which insures a low impedance resistive load for the amplifier at high frequencies. Refer to Figure 23. Resistance will run from 10 to 100 ohms, and capacitance will generally be between .1 to 1 microfarad.

The only observed case of an APEX complementary hybrid amplifier showing instability into inductive loading is the PA02 in high speed inductive load applications. The instability is a result of heavy local feedback in the output stage.

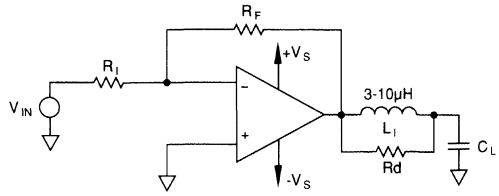


FIGURE 22. CAPACITIVE LOAD ISOLATION

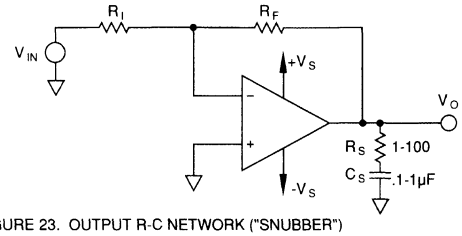


FIGURE 23. OUTPUT R-C NETWORK ("SNUBBER")

10.3 COMMON SOURCES OF INSTABILITY

The following is a list of the most common instability situations reported:

1) Ungrounded cases can cause oscillations, especially with faster amplifiers. The cases of all APEX amplifiers are electrically isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross-coupling or positive feedback leading to oscillations.
2) A standard inverting circuit includes an impedance matching resistor in series with the non-inverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna, receiving positive feedback, causing oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least .01uF.
3) Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended, but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
4) A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test okay. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the board oscillates. Cross coupling through the supplies is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case and include an input R-C compensation network as described in Section 10.2.1 if possible.

10.4 A FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an **"acceptably low"** level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply these techniques and ideas under your worst case load conditions and you can conquer your oscillation problems.

The APEX Applications Hotline

The APEX Applications Hotline provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to APEX for a free failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.

QUALITY

NOTES:

GRADE COMPARISON

Apex offers two different levels of quality screening: INDUSTRIAL AND MILITARY GRADE. Both grades are produced on the same production line and assembled in the same Class 100,000 clean room. This approach ensures a high quality level for our INDUSTRIAL products, as well as our MILITARY products.

Our INDUSTRIAL products are 100% static and dynamic tested, performed at 25°C. Our MILITARY products are 100% tested over their respective full temperature range for both static and dynamic parameters.

OPERATION	INDUSTRIAL GRADE	MILITARY GRADE
Clean room processing	YES	YES
Clean room testing	YES	YES
Solder Integrity tested	YES	YES
Wire bond integrity tested	YES	YES
All processing under document control	YES	YES
High power die inspection	NO	YES
Processed on military line	YES	YES
Certified operators	NO	YES
Assembled by a single team	NO	YES
Maximum Number Of Rework Cycles Specified:		
Solder	YES	YES
Epoxy	NO	YES
Wirebond	NO	YES
Pre-cap visual	SAMPLE	100%
Pre-seal vacuum bake	1 hr.	2 hrs.
Welded in controlled ATM.	YES	YES
Each unit checked for hermeticity	NO	YES
Stabilization bake: 24 hrs. @ 150°C	NO	YES
Temp. cycle: -65 to +150°C @ 10 cycles	NO	YES
Constant acceleration 10000G Y1	NO	YES
Burn-in: 160 hrs. @ 125°C	NO	YES
Dynamic testing	25°C	–55, +25, +125°C
External visual	NO	YES
Pin finish	Ni	Au

AUGUST 1, 1991
SMD GRADE AVAILABILITY

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BASE MODEL	INDUSTRIAL	"M" NON-COMPLIANT MILITARY	"M/883"	STOCKED SMD #
DB2805	S	N	N	N
DB2812	S	N	N	N
DB2815	S	N	N	N
PA01	S	N	N	N
PA02	S	N	C	5962-9067901HXC
PA03	S	N	N	N
PA04	S	N	N	N
PA05	S	N	N	N
PA07	S	N	C	5962-9063801HXC
PA08	S	N	C	5962-9072301HXC
PA09	S	N	S[3]	5962-9170001HXC[2]
PA10	S	N	C	5962-9082801HXC
PA12	S	N	C	5962-9065901HXC
PA19	S	N	N	N
PA21	S	N	N[1]	N
PA25	S	N	N	N
PA41	S	N	N	N
PA51	S	N	S[3]	5962-8762002YC[2]
PA61	S	N	S	N
PA73	S	N	S	N
PA81	S	N	N	N
PA82	S	N	N	N
PA83	S	N	C	5962-9162101HXC
PA84	S	N	C	5962-9073601HXC
PA85	S	S	N	N
PA88	S	S	N	N
PA89	S	N	N	N
PB50	S	N	N	N
PB58	S	N	N	N
WA01	S	N	N	N
WB05	S	N	N	N

S = stocked,
C = custom order basis
N = not available

[1] Under development with expected availability 2nd quarter '92
[2] Not released as of August 1, 1991.
[3] These models will switch to custom order basis upon SMD release.

NOTE: For a complete, up-to-date listing of all "M/883" products and Standardized Military Drawing (SMD) numbers, refer to the most current Apex Order Information and Price List data sheet.

M and /883 SCREENING PROGRAM

DESCRIPTION

These Apex Microtechnology power hybrids have been screened to MIL-STD-883C, Method 5008, Class B and manufactured in a DESC Certified MIL-STD-1772 Facility using the baseline documents listed herein. They provide a high reliability product option and satisfy the requirements for components used in airborne and ground-based military applications. Compliance with these requirements is signified by the "/883" suffix in the model number. "Non-compliant" version is identified using "M" only in the model number.

Complete description of an APEX "M" or "/883" product consists of the following:

1. **Industrial Grade Data Sheet** (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. **"M" Data Sheet** (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of –55°C to +125°C.
3. **APEX "/883" Screening Program Data Sheet** (i.e. this document).
   This defines the manufacturing processes and screening steps for an "M" or "M/883" product. (Refer to Figure 1 for order of flow.)
4. **Package and Accessories Information Data Sheet**
   This contains the package outline dimensions (i.e. 8-pin TO-3).

All applications data and performance optimization suggestions given for the Industrial model apply to Military versions of a given product family as well. Package outlines are identical except that Military grade pins are gold plated to meet the solderability requirements of MIL-STD-883, Method 2003.

1772 FACILITY APPROVAL STATUS

As of November 8, 1989, APEX is a DESC certified MIL-STD-1772 facility. DESC approved the APEX MIL-STD-1772, Section B, test plan in November of 1989. Qualification was granted to APEX as of May 31, 1990. APEX received a QML listing on May 31, 1990.

CONSTRUCTION

These power hybrids have been built and assembled using the chip and wire process. A metallized ceramic (beryllia) substrate is used with thick film resistors and gold conductors. Power transistors are attached to silver conductors at the same time that the substrate is attached to the header, using high temperature solder and reflow techniques. Small signal die are attached using MIL-STD-883 method 5011 conductive epoxy. Chip capacitors are attached with conductive epoxy. Die to substrate and pin to substrate wire bonds use 1, 5 or 10 mil diameter aluminum wire. The package is hermetically sealed using high-speed, one-shot resistance welding in a dry nitrogen atmosphere.

1.0 APPLICABLE DOCUMENTS

1.1 SPECIFICATIONS

MIL-M-55565	Microcircuits, Packaging of
MIL-H-38534	General Specification for Hybrid Microcircuits

1.2 STANDARDS

MIL-STD-883	Test Methods and Procedures for Microelectronics

1.3 BASELINE DOCUMENTS

APEX maintains on file the procedures, process specifications and process qualification reports that are in general the documents which have established the baseline for APEX in satisfying the requirements of certification in accordance with Section A of MIL-STD-1772.

1.4 PERFORMANCE SPECIFICATIONS

The performance specifications for a particular "M" or "/883" hybrid circuit are contained in the following documents:

1. Industrial Grade Data Sheet (i.e. PA02/PA02A).
   This contains Typical Characteristics and Performance Graphs.
2. "M" Data Sheet (i.e. PA02M).
   This is the Table 4 – Group A Inspection which defines the parameters and limits that the product must meet when tested over the full military case temperature range of -55°C to +125°C.

In the event of conflicting requirements, the order of precedence will be: purchase order, customer's SCD, the APEX "M" data sheet, and other reference documents.

2.0 GENERAL REQUIREMENTS

The individual requirements are specified herein and in accordance with the applicable APEX "M" data sheet. The static and dynamic electrical performance requirements for the hybrid circuit and test conditions are as specified in the applicable APEX "M" data sheet.

2.1 PROCESS CONDITIONING, TESTING, RELIABILITY, and QUALITY ASSURANCE SCREENING

Process conditioning, screening and testing are as specified in Section 4.0. Figure 1 illustrates the process flow for "M" or "M/883" products processed to MIL-STD-883, Class B.

2.1.1 PRODUCT or PROCESS CHANGE

APEX will not implement any major change, as listed in MIL-H-38534, to the design, materials, construction, configuration, or manufacturing process which may affect the performance, quality, reliability, or interchangeability of the circuit without full or partial re-qualification. "M" product is a HI-REL non-compliant product.

2.2 QUALITY CONFORMANCE

The "M" or "/883" hybrid circuits furnished under this specification are products which have been produced and tested in conformance with all the provisions of this specification.

2.3 MARKING

2.3.1 MARKING EACH DEVICE

The following marking is placed on each hybrid circuit:

a) Index point (see 2.3.4)
b) Part number (see 2.3.5)
c) CAGE code number (see 2.3.6)
d) Lot identification code (see 2.3.7)
e) Manufacturer's identification (see 2.3.8)
f) Country of origin (see 2.3.9)
g) BeO warning (if applicable, see 2.3.10)
h) ESD identifier Δ

These units are Class 1 as defined in MIL-H-38534; therefore, the ESD identifier Δ is incorporated in the mark.

2.3.2 MARKING ON INITIAL CONTAINER

Marking on initial anti-static packaging for delivery includes:

a) Manufacturer's identification
b) Customer name
c) Customer's P.O. number
d) Quantity packaged
e) Lot code
f) Customer's SCD number
g) Date packaged
h) Packaging operator's initials

2.3.3 MARKING PERMANENCE
Marking is permanent in nature to MIL-STD-883, Method 2015.

2.3.4 INDEX POINT
The index point, denoting location of Pin 1, is indicated as shown on the appropriate Package Outline.

2.3.5 PART NUMBER
The part number is the APEX generic part number.

2.3.6 CAGE CODE NUMBER
The CAGE code number for APEX is 60024 as designated by the Federal government.

2.3.7 LOT IDENTIFICATION CODE
The lot identification code is a 9-digit alphanumeric code. The first two letters indicate the assembly team leader responsible for manufacture of the lot. These initials are followed by a three digit lot code, a two digit year-of-seal code, and a two digit week-of-seal code.

2.3.8 MANUFACTURER'S IDENTIFICATION
The manufacturer's identification is signified by the name, logo, or trademark of APEX MICROTECHNOLOGY incorporated in the mark.

2.3.9 COUNTRY OF ORIGIN
The country of origin is signified by USA incorporated in the mark.

2.3.10 BeO WARNING
Since these hybrid circuits contain beryllium oxide substrates, the "BeO" identifier is marked on the package as an alert to the user, that if the package seal is broken, not to crush, machine, or subject the substrate to temperatures in excess of 850°C to avoid generating toxic fumes.

3.0 CONDITIONS AND METHODS OF TEST
Conditions and methods of test are to MIL-STD-883, Method 5008, MIL-H-38534 and as specified herein. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application. All tests are performed on a 100% basis except where indicated.

3.1 HIGH POWER DIE INSPECTION
High power die inspection is performed to MIL-STD-750 Method 2072 and 2073, and MIL-STD-883 Method 2010.

3.2 INTERNAL VISUAL INSPECTION (PRECAP)
Internal visual inspection is performed to MIL-STD-883, Method 2017 and 2032.

3.3 STABILIZATION BAKE
Stabilization bake is performed to MIL-STD-883, Method 1008, Condition C. The devices are stored for 24 hours at 150°C. No end point measurements are performed.

3.4 TEMPERATURE CYCLING
Temperature cycling is performed to MIL-STD-883, Method 1010, Condition C, using 10 cycles from –65°C to +150°C.

3.5 BURN-IN
Burn-in is performed to MIL-STD-883, Method 1015, Condition D for 160 hours at a case temperature of 125°C.

3.6 CONSTANT ACCELERATION
Constant acceleration is performed to MIL-STD-883, Method 2001, Condition B, at 10,000 G's, in the Y1 axis only.

3.7 FINAL ELECTRICAL TEST
Final electrical tests are performed to MIL-STD-883. Both static and dynamic parameters from Group A, Subgroups 1-6, are 100% tested to the "M" data sheet limits at –55°C, 25°C and +125°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to static (DC) measurements at 25°C.

3.8 HERMITICITY
Hermiticity tests are performed per the following:

3.8.1 FINE LEAK TESTING
Fine leak testing is performed to MIL-STD-883, Method 1014, Condition A, at $1X10^{-6}$ cc/sec standard leak rate.

3.8.2 GROSS LEAK TESTING
Gross leak testing is performed to MIL-STD-883, Method 1014, Condition C, at 60 PSIG pre-pressurization.

3.9 EXTERNAL VISUAL INSPECTION
All "M" and "/883" hybrid circuits receive external visual to MIL-STD-883, Method 2009.

4.0 QUALITY ASSURANCE PROVISION*

4.1 QUALITY CONFORMANCE INSPECTION
Quality Conformance Inspection (QCI) is to MIL-H-38534, Option 1, in-line qualification method. Lots failing to meet quality conformance inspection for a given product assurance level are rejected.

4.1.1 GROUP A ELECTRICAL TESTING
Group A electrical testing is performed using in-line verification in accordance with Option 1 of MIL-H-38534. Electrical parameters and test limits are as shown in the "M" data sheet.

4.1.2 GROUP B INSPECTION
Group B inspection is satisfied by performing in-line inspection sampling, to MIL-H-38534, Option 1, for the following subgroups:

i) Physical dimensions
ii) Resistance to solvents
iii) Internal visual and mechanical
iv) Bond strength
v) Die Shear
vi) Solderability
vii) Seal

4.1.3 GROUP C INSPECTION
Group C inspection is performed on the first lot submitted for inspection and as required to evaluate or qualify changes in manufacturing processes per MIL-H-38534, Option 1.

4.1.4 GROUP D INSPECTION
Group D testing in accordance with MIL-H-38534, Option 1, is accomplished during package evaluation at incoming inspection to MIL-STD-883, Method 5008, and is not repeated.

5.0 DATA AND REPORTS*

5.1 CERTIFICATE of COMPLIANCE
All "M/883" hybrid circuits are accompanied by a Certificate of Compliance.

5.2 QUALITY CONFORMANCE REPORTS
Per MIL-H-38534, Option 1, Group A lot data is kept on file with the production records. In-line Groups B, C and D (reference 4.1.4) generic data is also on file.

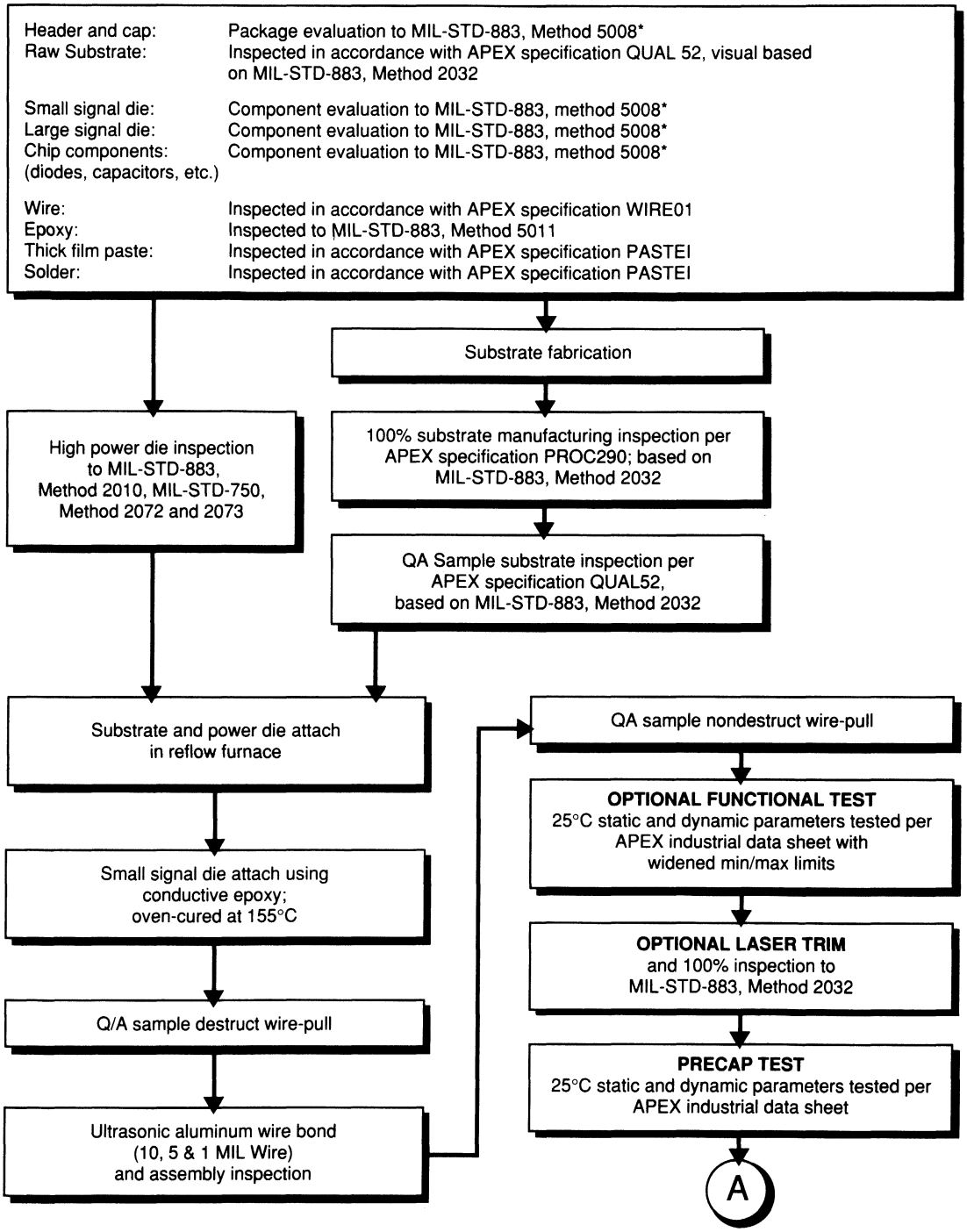
5.3 TRACEABILITY
Traceability is to MIL-H-38534. Each hybrid circuit is traceable to the production lot. Re-worked or repaired circuits maintain traceability.

6.0 PACKAGING
Packing and packaging are to MIL-M-55565.

7.0 CUSTOM MARKING
Production quantities of "M" and "M/883" devices may be dual or solely marked with an applicable SCD number.

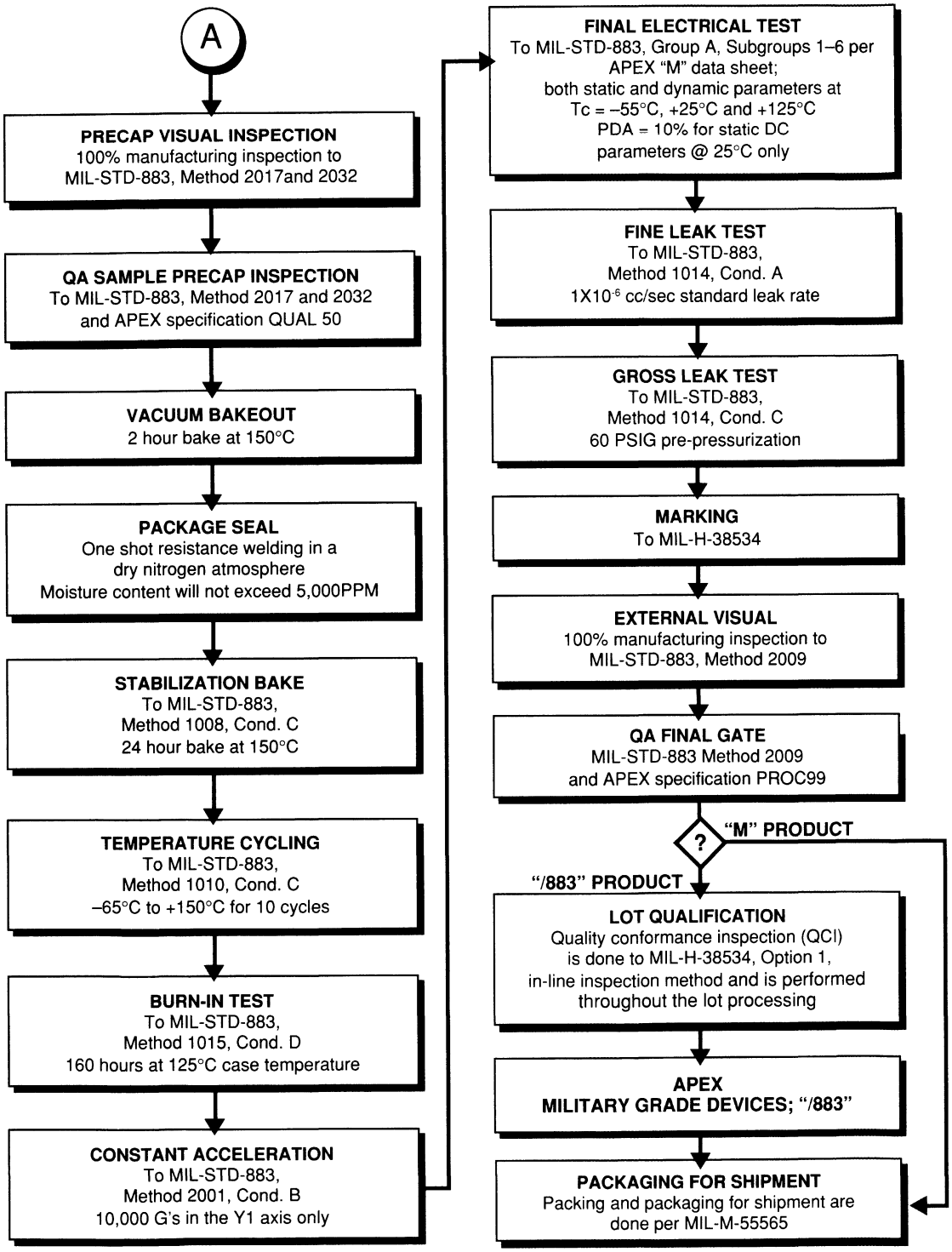
* Applies to compliant (/883) product only.

FIGURE 1: APEX COMPLIANT /883 & NON-COMPLIANT "M" GRADE PRODUCT SCREENING FLOW



* Applies to compliant (/883) product only.

FIGURE 1: APEX COMPLIANT /883 & NON-COMPLIANT "M" GRADE PRODUCT SCREENING FLOW



ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are stress levels which may be applied to the amplifier one at a time. The amplifier will not suffer permanent damage. However, proper operation is not implied. Simultaneous application of two or more of these maximum stress levels may induce permanent damage to the amplifier.

DIFFERENTIAL INPUT VOLTAGE

Differential input voltage is the voltage difference between the two input pins. It will be near zero in any linear (nonsaturated) operating mode. Non-zero voltages arise with very fast rising input waveform, shorted outputs, overdriven inputs, and other abnormal conditions.

RTI (REFERRED TO THE INPUT)

All input errors will be seen at the output of the amplifier at an amplitude equal to the input error term times the noninverting gain of the circuit. Errors are seen from the noninverting input pin, i.e., voltage offset will appear at a gain of two at the output in an inverting gain of one circuit.

LOOP GAIN

Loop gain is the difference between open loop gain and the gain of the external circuit. This excess gain over the required signal amplification is the key feature of all operational amplifiers that provide a proportional increase in accuracy.

TYPICAL SUPPLY VOLTAGE

Typical supply voltage is a value which APEX has determined to be the optimum voltage to specify. This value is influenced by both customer input and competitor specifications.

COMMON MODE IMPEDANCE: Z_{IN}

Z_{IN} is the effective impedance from either input to common (ground). Because most op amps do not have ground pins, the specification is often referred to the midpoint of the two power pin voltages as in the case of single supplies. Measuring the effect of a known source impedance driving a buffer configuration will yield common mode input impedance. Low frequency inputs are used to characterize resistive elements and higher frequencies enable measuring capacitive elements of the input impedance. This value is generally very high and can be neglected; therefore, it is usually part of the design characterization data rather than a 100% tested parameter.

COMMON MODE VOLTAGE: CMV

CMV is the average (common component) of two input voltages with respect to the midpoint of the two power supply voltages (ground in the case of dual symmetric supplies). Because most op amps do not have ground pins, the parameter is often specified as a minimum voltage difference between the CMV and either supply rail. When operating on a single supply, the CMV specifications of APEX amplifiers do not allow input pin voltages to reach zero or the supply voltage. In any nonsaturated operating mode, both input voltages will be essentially equal.

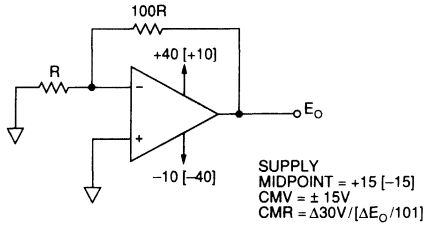


FIGURE 1. SUPPLY MIDPOINT, COMMON MODE VOLTAGE, COMMON MODE REJECTION

COMMON MODE REJECTION: CMR

Common mode rejection is the ability of the amplifier to reject two equal input signals as they vary from the midpoint of the two supply voltages (ground in the case of dual symmetric supplies).

INPUT BIAS CURRENT: I_B

I_B is the net current flowing into or out of the amplifier input pins at a zero signal condition. This current results from base currents of bipolar input transistors (sometimes reduced by cancellation networks) or gates leakage of FET input transistors. Measurement techniques require insertion of very large impedances in series with the inputs and converting the resulting output voltage change to a bias current in accordance with Ohm's Law.

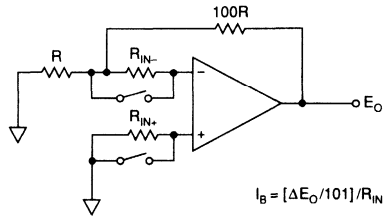


FIGURE 2. INPUT BIAS CURRENT

INPUT OFFSET CURRENT: IOS

I_{OS} is the difference between the two bias currents. The offset current rating is generally smaller than the bias current rating which implies that matching impedances for the two amplifier inputs will result in smaller error than either bias current alone would produce.

INPUT OFFSET VOLTAGE: V_{OS}

V_{OS} is the voltage required at the input of an amplifier to produce zero output. Most often, this parameter is measured in the opposite manner, namely, the output voltage resulting from a zero input. With a given gain configuration, the output voltage is divided by the noninverting gain of the circuit to determine the voltage at the input (referred to the input or RTI).

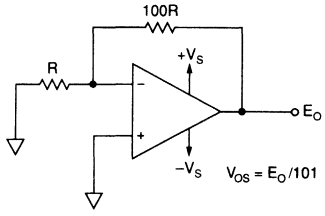


FIGURE 3. INPUT OFFSET VOLTAGE

INPUT VOLTAGE NOISE: V_N

V_N is the noise component of voltage offset. The noise is measured at the output with a true RMS meter and referred to the input. Low pass and bandpass filters may be used to limit meter response. At any given 3dB bandwidth, the RMS value is divided by the square root of that bandwidth to obtain the spectral noise density.

INPUT CURRENT NOISE: I_N

I_N is the noise component of bias current. It is an RTI specification similar to current offset. The use of the filters and the calculation of spectral noise density is similar to the procedures used for voltage noise.

POWER SUPPLY REJECTION: PSR

PSR is the ability of the amplifier to reject the effect of changes in total supply voltage on voltage offset. Dual, supplies are varied simultaneously to test this parameter. Supply values will include the minimum and maximum operating specifications. Changing from dual 15V supplies to dual 20V supplies is a 10V change of total supply voltage. A resulting 1mV offset change would indicate a PSR of 100µV/V or 80dB. When PSR is plotted versus frequency, one supply at a time has the AC waveform impressed upon it.

OUTPUT VOLTAGE SWING: V_O

V_O is the minimum voltage swing capability of the amplifier and is usually specified at multiple current ratings. The amplifier is driven in excess of the specified output and then checked for minimum output with the appropriate load.

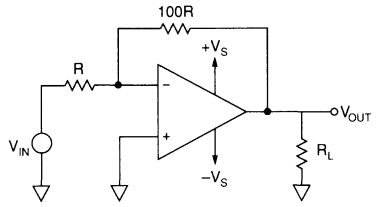
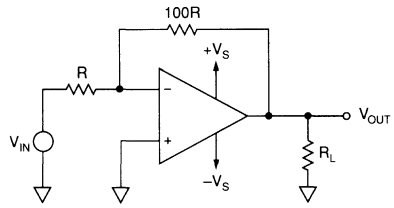


FIGURE 4. OUTPUT VOLTAGE SWING

CURRENT LIMIT: I_{CL}

With the amplifier overdriven, a small resistor is used to detect the point of current limiting. Resistance values and power supply voltages are selected to insure that a nonlimiting amplifier will be detected without excessive internal power dissipation.



$I_{CL} = V_{OUT}/R_L$

FIGURE 5. CURRENT LIMIT

SLEW RATE: SR

SR is the maximum rate of change of the output voltage. An inverting gain circuit is usually used with an input signal at least 10 times faster than the amplifier rating. Measurement points are between 10 and 90% of total output swing. Overdriving the amplifier is permissible though at times may result in overload recovery problems.

FULL POWER RESPONSE

Full power response is the highest frequency at which the amplifier can drive a sine wave without visible distortion (3-5%) on an oscilloscope. Supply voltage is set to the typical rating. Power response curves relate the reduced output as a function of frequency but independent of gain.

GAIN BANDWIDTH PRODUCT

Gain Bandwidth Product is the product of gain times frequency at a specified frequency. This is always measured at or below the unity gain frequency of the amplifier.

SETTLING TIME

Settling time is the time required for the amplifier to settle within a specified error of final value. Slewing time is included. This parameter is usually measured using the inverting gain of one circuit, a false summing junction, and a very fast rising input waveform triggering an oscilloscope.

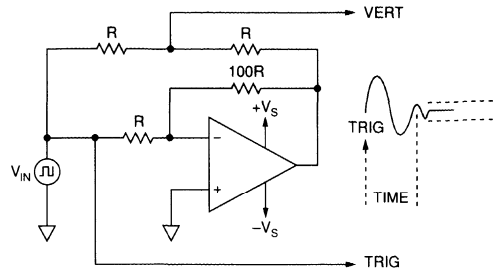
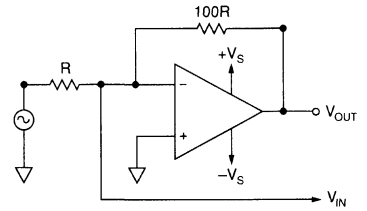


FIGURE 6. SETTLING TIME

OPEN LOOP GAIN: A_{OL}

A_{OL} is the actual gain from the inverting input pin to output, with the noninverting input grounded. If plotted versus frequency, it is call a bode plot.



$A_{OL} = V_{OUT}/V_{IN}$

A_{OL} [dB] = 20 Log [V_{OUT}/V_{IN}]

FIGURE 7. OPEN LOOP GAIN

OPEN LOOP PHASE RESPONSE

Open loop phase response is the actual phase from the noninverting input pin to output. While ideally between 0° and 90°, it may be higher. It is usually plotted versus frequency. Measurement techniques are similar to those used for open loop gain.

PHASE MARGIN

Phase margin is 180° less the open loop phase at frequency where the open loop gain of the amplifier is unity.

QUIESCENT CURRENT: I_Q

Quiescent current is the current drawn from each supply rail with zero output voltage and load current. Insignificant differences between the two supply rail currents may exist due to input bias currents.

REACTANCE CHART

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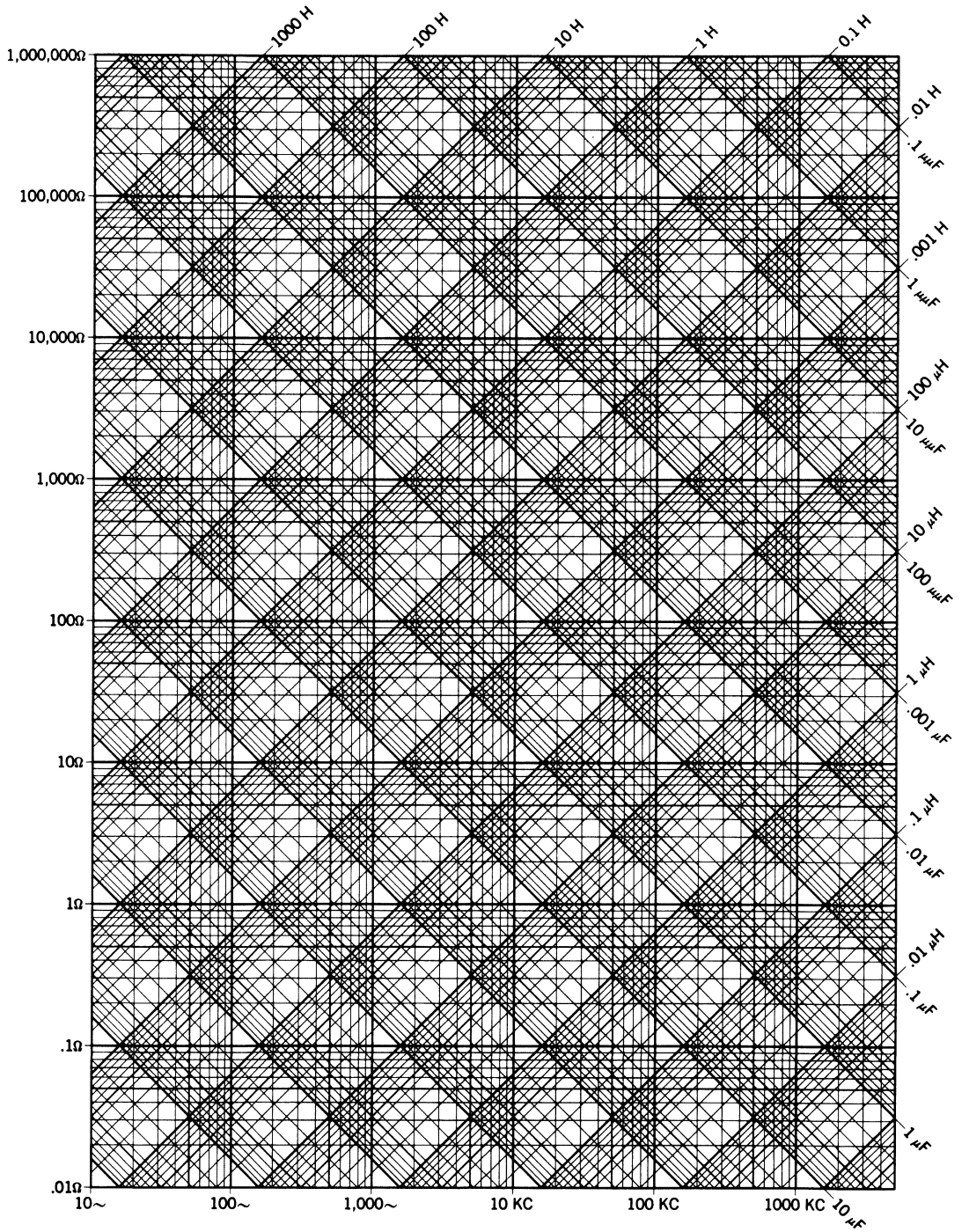
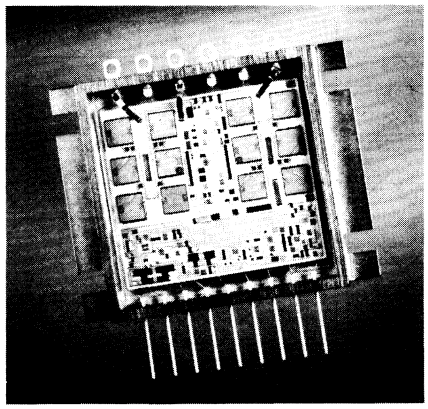


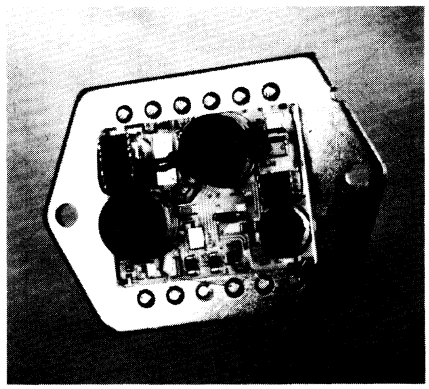
THINGS TO COME FROM APEX
PRODUCTS UNDER DEVELOPMENT

As this handbook went to print on August 1, 1991, these are a few of the areas where Apex is focusing its new product efforts.



2000W OP AMP

- 1000W internal dissipation
- 50A continuous output capability, 100A pulse
- Side lead package (see cover photo)
- ±15V to ±100V supply
- Foldover current limiting with Kelvin sensing
- Thermal protection and temperature reporting



DUAL DC/DC CONVERTERS

- 30W output power
- ±12V and ±15V models
- 9V to 50V input range
- 30W per cubic inch

Apex welcomes new product input from our customers. If you have a new product idea, please call the Apex Applications Hotline at (800) 421-1865, or return the reply card provided at the back of this handbook and an Apex Applications Engineer will call you. Thank you.

POWER AMPLIFIERS

NOTE: For a complete listing of all /883 products and Standardized Military Drawing numbers (SMD) refer to the most current APEX Order Information and Price List.

NOTES:

PA01 • PA73

FEATURES

- LOW COST, ECONOMY MODEL — PA01
- SECOND SOURCEABLE — PA73
- HIGH OUTPUT CURRENT — Up to ±5A PEAK
- EXCELLENT LINEARITY — PA01
- HIGH SUPPLY VOLTAGE — Up to ±34V
- ISOLATED CASE —300V

APPLICATIONS

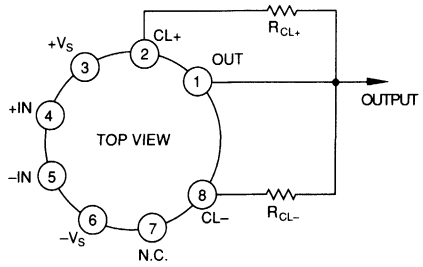
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 20kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 56V
- AUDIO AMPLIFIERS UP TO 50W RMS

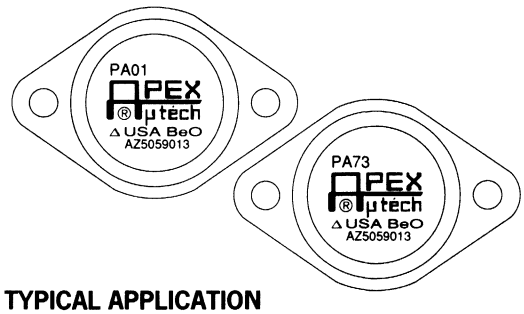
DESCRIPTION

The PA01 and PA73 are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. All three have a complementary darlington emitter follower output stage protected against transient inductive kickback or back EMF. For optimum linearity, the PA01 has a class A/B output stage. The PA73 has a simple class C output stage (see Note 1) to reduce cost for motor control and other applications where crossover distortion is not critical and to provide interchangeability with type 3573 amplifiers. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limit resistors. These amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

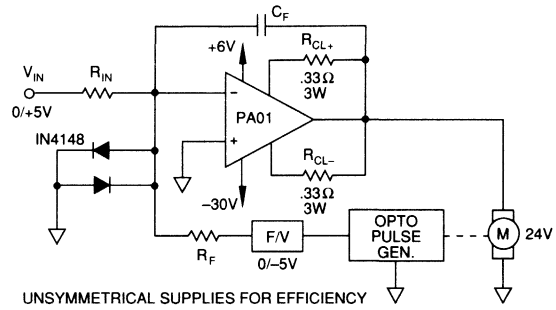
This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EXTERNAL CONNECTIONS





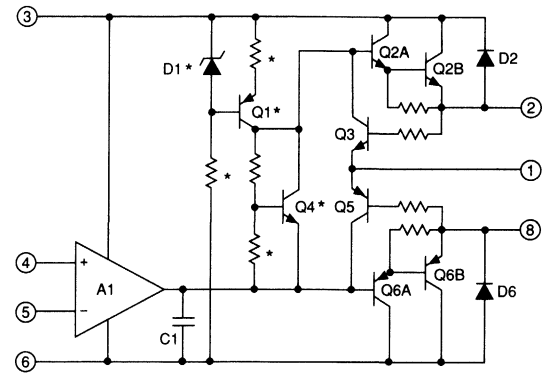
TYPICAL APPLICATION



Unidirectional Optical Speed Control

The pulse output of a non-contact optical sensor drives a voltage-to-frequency converter which generates feedback for the op amp. With the loop closed in this manner, the op amp corrects for any variations in the speed due to changing load. Because of operation in only one direction, an unsymmetrical supply is used to maximize efficiency of both power op amp and power supply. High speed diodes at the input protect the op amp from commutator noise which may be generated by the motor.

EQUIVALENT SCHEMATIC



NOTE 1: * Indicates not used in PA73. Open base of Q2A connected to output of A1.

ABSOLUTE MAXIMUM RATINGS

	PA01	PA73
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	60V	68V
OUTPUT CURRENT, within SOA	5A	5A
POWER DISSIPATION, internal[1]	67W	67W
INPUT VOLTAGE, differential	$\pm V_S$ –3V	$\pm V_S$ –3V
INPUT VOLTAGE, common-mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, junction[1]	200°C	200°C
TEMPERATURE, pin solder -10s	300°C	300°C
TEMPERATURE RANGE, storage	–65 to +150°C	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C	–25 to +85°C

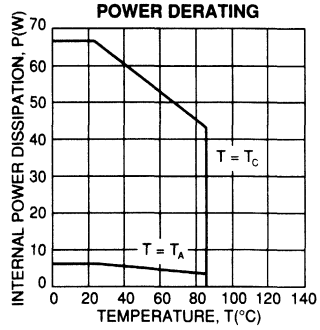
SPECIFICATIONS

		PA01			PA73			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±12		*	±.10	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±35			*	±200	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±15	±50		*	±40	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05	±.4		*	*	nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.02			*		nA/V
OFFSET CURRENT, initial	T_C = 25°C		±5	±15		*	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.01			*		nA/°C
INPUT IMPEDANCE, common-mode	T_C = 25°C		200			*		MΩ
INPUT IMPEDANCE, differential	T_C = 25°C		10			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–6	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	T_C = 25°C, $V_{CM} = V_S$ –6V	70	110		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	91	113		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 4A, $V_O = 40V_{PP}$	15	23		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–10	$\pm V_S$–5		$\pm V_S$–8	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6	$\pm V_S$–5		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 46mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	±5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 2.5Ω	±1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			3.3			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±28	*	*	±30	V
CURRENT, quiescent	T_C = 25°C		20	50		20/2.6	30/5	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

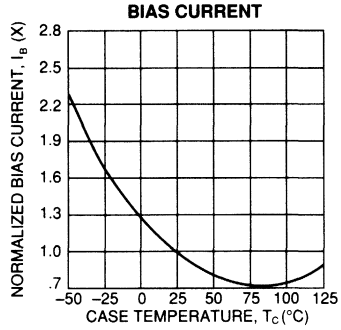
NOTES: * The specification of PA73 is identical to the specification for PA01 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

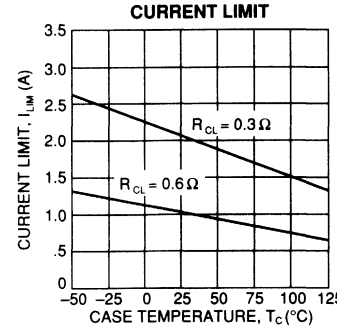
POWER DERATING



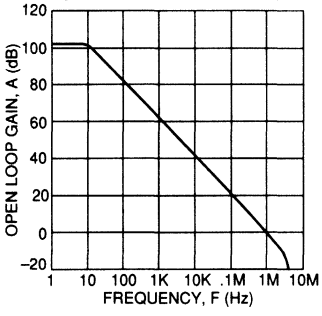
BIAS CURRENT



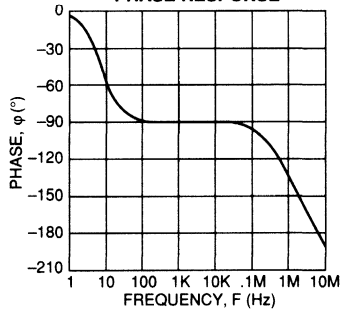
CURRENT LIMIT



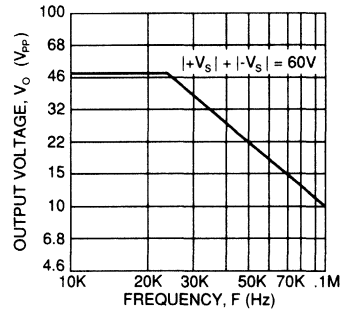
SMALL SIGNAL RESPONSE



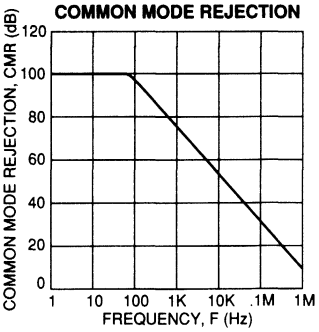
PHASE RESPONSE



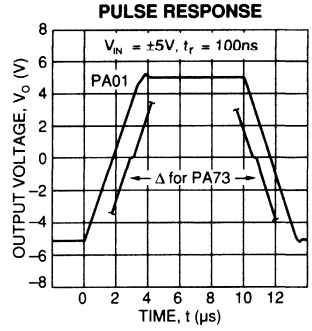
POWER RESPONSE



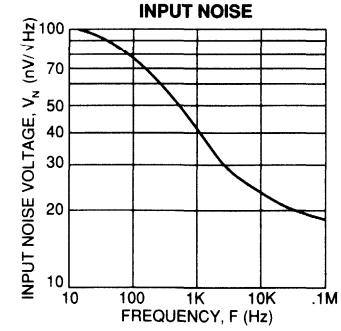
COMMON MODE REJECTION



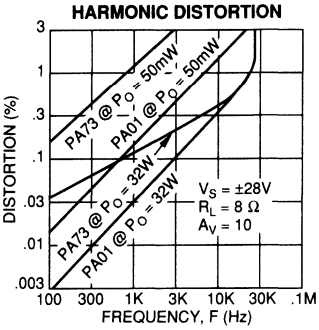
PULSE RESPONSE



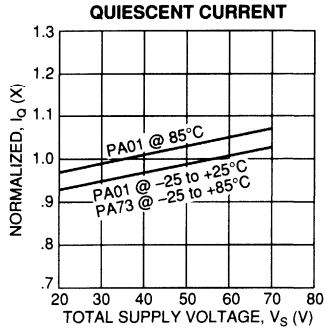
INPUT NOISE



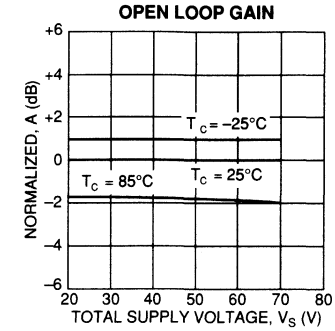
HARMONIC DISTORTION



QUIESCENT CURRENT



OPEN LOOP GAIN



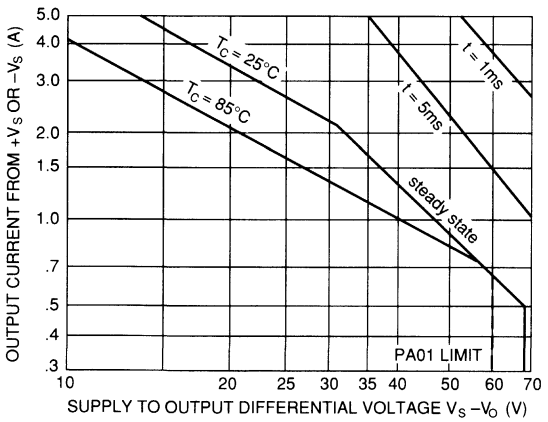
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. Capacitive and dynamic* inductive loads up to the following maximums are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
30V	1,200µF	500µF	250mH	24mH
25V	4,000µF	1,600µF	400mH	38mH
20V	20,000µF	5,000µF	1,500mH	75mH
15V	**	25,000µF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Secondary breakdown effect imposes no limitation but thermal limitations must still be observed.

2. EMF generating or reactive load and short circuits to the supply rails or shorts to common are safe if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
34V	.50A	1.2A
30V	.60A	1.3A
25V	.75A	1.6A
20V	1.0A	2.1A
15V	1.3A	2.8A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

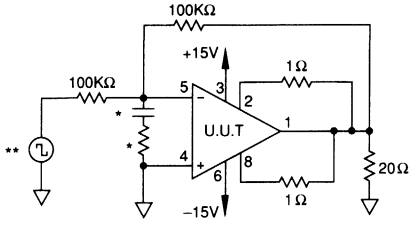
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown, in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±28V	V_{IN} = 0, A_V = 100		5	mA
1	Input Offset Voltage	V_{OS}	25°C	±28V	V_{IN} = 0, A_V = 100		±10	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
1	Input Offset Voltage	V_{OS}	25°C	±30V	V_{IN} = 0, A_V = 100		±10.8	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±28V	V_{IN} = 0		±40	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±28V	V_{IN} = 0		±40	nA
1	Input Offset Current	I_{OS}	25°C	±28V	V_{IN} = 0		±10	nA
3	Quiescent Current	I_Q	–55°C	±28V	V_{IN} = 0, A_V = 100		5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±28V	V_{IN} = 0, A_V = 100		±15.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±22.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±30V	V_{IN} = 0, A_V = 100		±16	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±28V	V_{IN} = 0		±72	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±28V	V_{IN} = 0		±72	nA
3	Input Offset Current	I_{OS}	–55°C	±28V	V_{IN} = 0		±26	nA
2	Quiescent Current	I_Q	125°C	±28V	V_{IN} = 0, A_V = 100		7	mA
2	Input Offset Voltage	V_{OS}	125°C	±28V	V_{IN} = 0, A_V = 100		±16.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±23.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±30V	V_{IN} = 0, A_V = 100		±17.3	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±28V	V_{IN} = 0		±80	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±28V	V_{IN} = 0		±80	nA
2	Input Offset Current	I_{OS}	125°C	±28V	V_{IN} = 0		±30	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±18.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 50mA	V_O	25°C	±30V	R_L = 500Ω	25		V
4	Output Voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±16V	R_L = 2.07Ω	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±28V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±28V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
6	Output Voltage, I_O = 5A	V_O	–55°C	±18.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 50mA	V_O	–55°C	±30V	R_L = 500Ω	25		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±30V	R_L = 12Ω	24		V
6	Stability/Noise	E_N	–55°C	±30V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±28V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
6	Common Mode Rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 50mA	V_O	125°C	±30V	R_L = 500Ω	25		V
5	Output Voltage, I_O = 2A	V_O	125°C	±30V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	125°C	±28V	R_L = 500Ω, A_V= 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±28V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±28V	R_L = 500Ω, F = 10Hz	91		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

FEATURES

- HIGH POWER BANDWIDTH — 350kHz
- HIGH SLEW RATE — 20V/μs
- FAST SETTLING TIME — 600ns
- LOW CROSSOVER DISTORTION — Class A/B
- LOW INTERNAL LOSSES — 1.2V at 2A
- HIGH OUTPUT CURRENT — ±5A PEAK
- LOW INPUT BIAS CURRENT — FET Input
- ISOLATED CASE — 300 VDC

APPLICATIONS

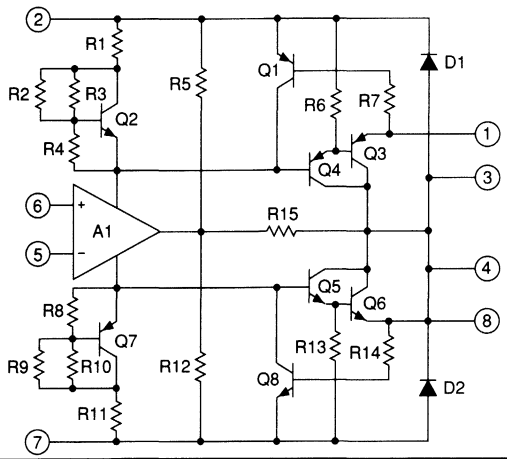
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 5A
- POWER TRANSDUCERS UP TO 350 kHz
- AUDIO AMPLIFIERS UP TO 30W RMS

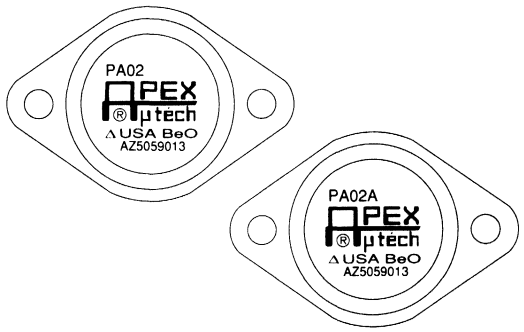
DESCRIPTION

The PA02 and PA02A are wideband, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting resistors (down to 10mA). Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

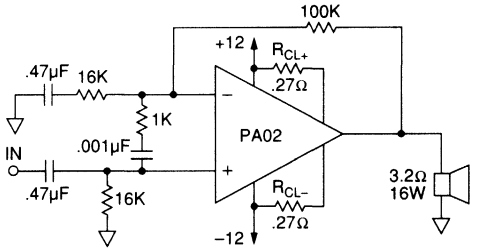
These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. Isolation washers are not recommended. The use of compressible isolation washers may void the warranty.

SCHEMATIC





TYPICAL APPLICATION

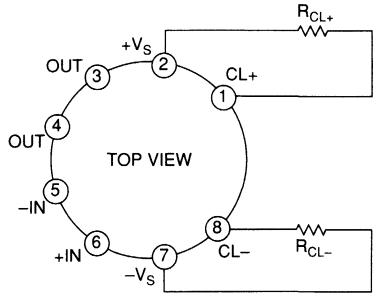


LOW INTERNAL LOSS MAXIMIZES EFFICIENCY

Vehicular Sound System Power Stage

When system voltages are low and power is at a premium, the PA02 is a natural choice. The circuit above utilizes not only the feature of low internal loss of the PA02, but also its very low distortion level to implement a crystal clear audio amplifier suitable even for airborne applications. This circuit uses AC coupling of both the input signal and the gain circuit to render DC voltage across the speaker insignificant. The resistor and capacitor across the inputs form a stability enhancement network (refer to Application Note 1). The 0.27 ohm current limit resistors provide protection in the event of an output short circuit.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	38V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	48W
INPUT VOLTAGE, differential	$\pm V_S$ –5V
INPUT VOLTAGE, common mode	$\pm V_S$ –2V
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

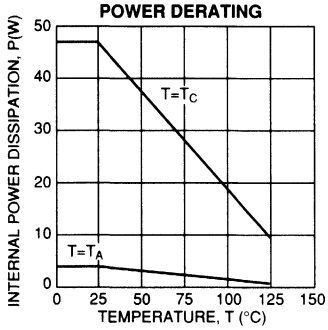
SPECIFICATIONS

		PA02			PA02A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±50		*	±25	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±6			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		50	200		25	100	pA
BIAS CURRENT, vs. temperature	T_C = 85°C			60			*	nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET VOLTAGE, initial	T_C = 25°C		25	100		15	50	pA
OFFSET VOLTAGE, vs. temperature	T_C = 85°C			15			*	nA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		1000			*		GΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLT. RANGE[5], Pos.	Full temperature range	$+V_S$ –6	$+V_S$ –3		*	*		V
COMMON MODE VOLT. RANGE[5], Neg.	Full temperature range	$-V_S$ +6	$-V_S$ +5		*	*		V
COMMON MODE REJECTION, DC	Full temperature range	70	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1kΩ load		103			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 10kΩ load	86	100		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, 10Ω load		4.5			*		MHz
POWER BANDWIDTH	T_C = 25°C, 10Ω load		350			*		kHz
PHASE MARGIN	Full temp. range, 10Ω load		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A, R_{CL} = .08Ω	$\pm V_S$ –4	$\pm V_S$ –3		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$ –2	$\pm V_S$ –1.2		*	*		V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.6			*		µs
SLEW RATE	T_C = 25°C	13	20		*	*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V > 10		SOA			*		
HARMONIC DISTORTION	P_O = .5W, F = 1kHz, R_L = 10Ω		.004			*		%
SMALL SIGNAL rise/fall time	R_L = 10Ω, A_V = 1		100			*		ns
SMALL SIGNAL overshoot	R_L = 10Ω, A_V = 1		10			*		%
POWER SUPPLY								
VOLTAGE	Full temperature range	±7	±15	±19	*	*	*	V
CURRENT, quiescent	T_C = 25°C		27	37		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC junction to case	F < 60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

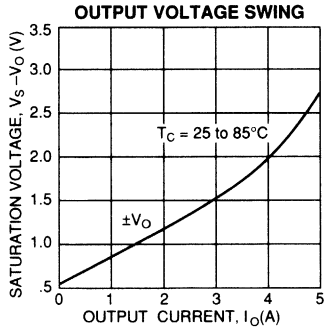
NOTES: * The specification of PA02A is identical to the specification for PA02 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. Exceeding CMV range can cause the output to latch.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

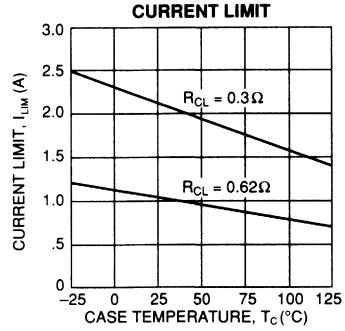
POWER DERATING



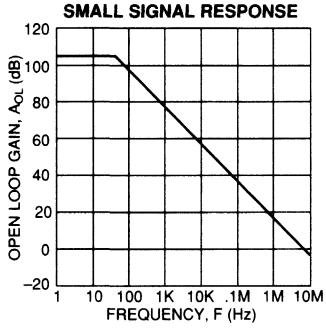
OUTPUT VOLTAGE SWING



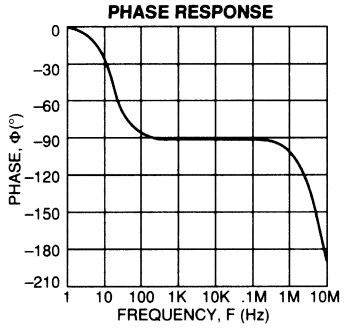
CURRENT LIMIT



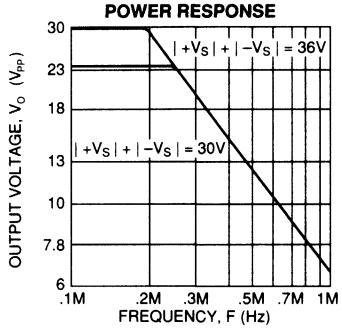
SMALL SIGNAL RESPONSE



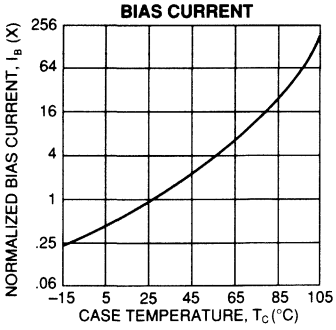
PHASE RESPONSE



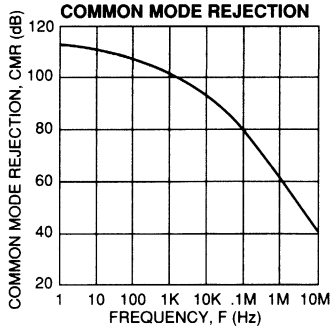
POWER RESPONSE



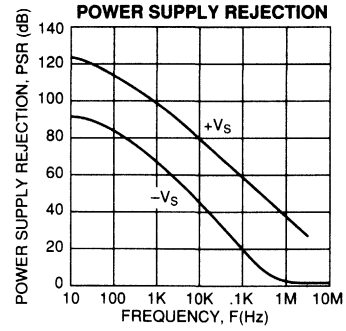
BIAS CURRENT



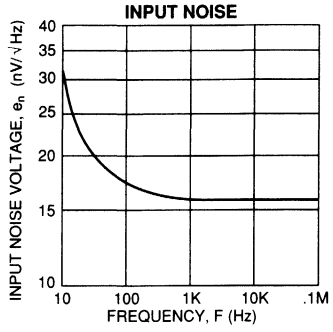
COMMON MODE REJECTION



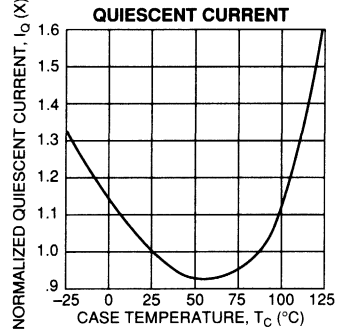
POWER SUPPLY REJECTION



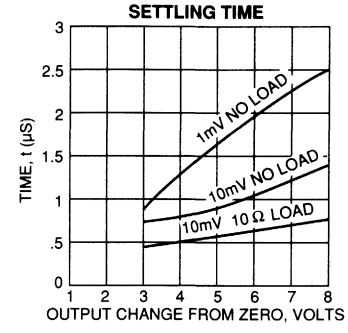
INPUT NOISE

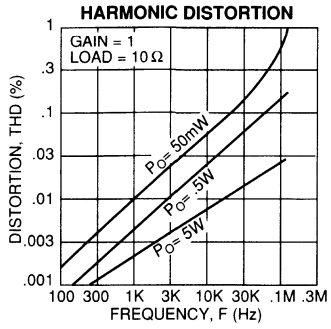


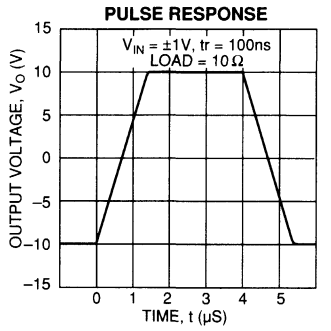
QUIESCENT CURRENT

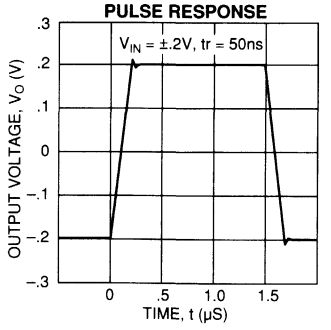


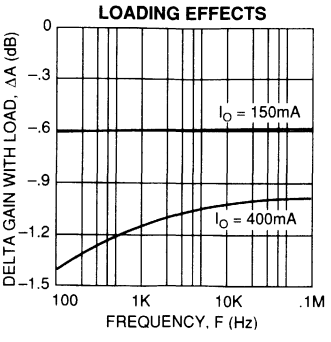
SETTLING TIME









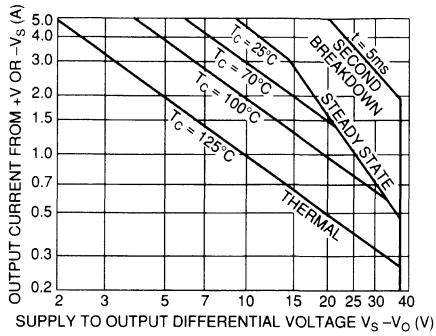


GENERAL

Please read the "General Operating Considerations" section which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:



1. Under transient conditions, capacitive and dynamic* loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
18V	2mF	0.7mF	.2H	10mH
15V	10mF	2.2mF	.7H	25mH
10V	25mF	10mF	5H	50mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A, or 17V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L OR EMF LOAD	SHORT TO COMMON
18V	.5A	1.7A
15V	.7A	2.8A
10V	1.6A	4.2A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 0.12 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

DEVICE MOUNTING

The case (mounting flange) is electrically isolated and should be mounted directly to a heatsink with thermal compound. Screws with Belville spring washers are recommended to maintain positive clamping pressure on heatsink mounting surfaces. Long periods of thermal cycling can loosen mounting screws and increase thermal resistance.

Since the case is electrically isolated (floating) with respect to the internal circuits it is recommended to connect it to common or other convenient AC ground potential.

PA02D

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421 1865

FEATURES

- **LOWER DISTORTION THAN PA02**
- **PROVIDES PA02 PERFORMANCE**
  - **HIGH SLEW RATE — 20V/μs**
  - **LOW V_{SAT} — 1.2V at 2A**
  - **HIGH OUTPUT CURRENT — ±5A**

APPLICATIONS

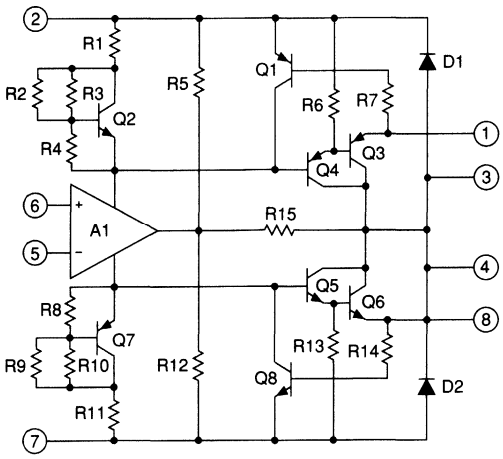
- **PRECISION ELECTROMAGNETIC DEFLECTION**
- **AUDIO AMPLIFIERS**

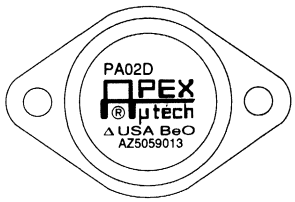
DESCRIPTION

The PA02D is a lower distortion PA02. Class A/B bias current has been increased in the output stage to improve THD. It is a wideband, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. Its complementary "collector output" stage can swing close to the supply rails and is protected against inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable, current limiting, resistors (down to 10mA). The amplifier is internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

These hybrid integrated circuits utilize thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. Isolation washers are not recommended. The use of compressible thermal interface washers and improper mounting will void the warranty.

EQUIVALENT SCHEMATIC

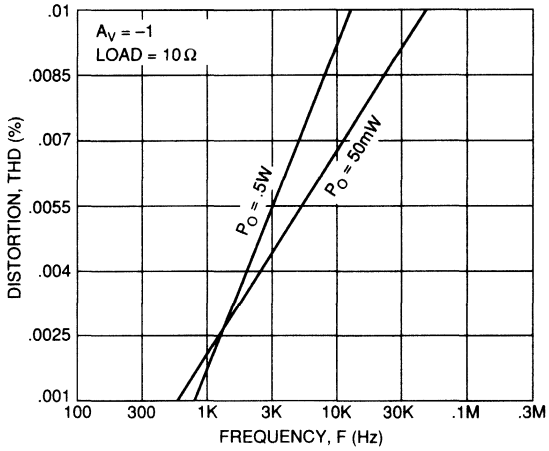




SPECIFICATIONS

Specifications of the standard PA02, except for quiescent current, apply with the benefit of lower distortion ratings. Design changes enabling lower distortion have no effect on the shape of the typical performance graphs, except for harmonic distortion.

HARMONIC DISTORTION



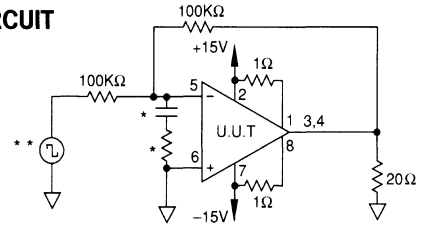
QUIESCENT CURRENT

		MIN	MAX
T_C = 25°C	$\pm V_S$ = ±15V		
	R_{CL} = .2Ω	90mA	110mA

NOTE: The increase in quiescent current for the PA02LD from a standard PA02 may require additional heatsinking.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω†		40	mA
1	Input offset voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		10	mV
1	Input offset voltage	V_{OS}	25°C	±7V	V_{IN} = 0, A_V = 100		11.6	mV
1	Input offset voltage	V_{OS}	25°C	±19V	V_{IN} = 0, A_V = 100		10.8	mV
1	Input bias current, +IN	$+I_B$	25°C	±15V	V_{IN} = 0		200	pA
1	Input bias current, –IN	$-I_B$	25°C	±15V	V_{IN} = 0		200	pA
1	Input offset current	I_{OS}	25°C	±15V	V_{IN} = 0		100	pA
3	Quiescent current	I_Q	–55°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω†		60	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		14	mV
3	Input offset voltage	V_{OS}	–55°C	±7V	V_{IN} = 0, A_V = 100		15.6	mV
3	Input offset voltage	V_{OS}	–55°C	±19V	V_{IN} = 0, A_V = 100		14.8	mV
3	Input bias current, +IN	$+I_B$	–55°C	±15V	V_{IN} = 0		200	pA
3	Input bias current, –IN	$-I_B$	–55°C	±15V	V_{IN} = 0		200	pA
3	Input offset current	I_{OS}	–55°C	±15V	V_{IN} = 0		100	pA
2	Quiescent current	I_Q	125°C	±15V	V_{IN} = 0, A_V = 100, R_{CL} = .2Ω†		60	mA
2	Input offset voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		15	mV
2	Input offset voltage	V_{OS}	125°C	±7V	V_{IN} = 0, A_V = 100		16.6	mV
2	Input offset voltage	V_{OS}	125°C	±19V	V_{IN} = 0, A_V = 100		15.8	mV
2	Input bias current, +IN	$+I_B$	125°C	±15V	V_{IN} = 0		30	nA
2	Input bias current, –IN	$-I_B$	125°C	±15V	V_{IN} = 0		30	nA
2	Input offset current	I_{OS}	125°C	±15V	V_{IN} = 0		30	nA
4	Output voltage, I_O = 5A	V_O	25°C	±9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
4	Output voltage, I_O = 36mA	V_O	25°C	±19V	R_L = 500Ω	18		V
4	Output voltage, I_O = 2A	V_O	25°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
4	Current limits	I_{CL}	25°C	±9V	R_L = 1Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/noise	E_N	25°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew rate	SR	25°C	±18V	R_L = 500Ω	13	100	V/µs
4	Open loop gain	A_{OL}	25°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
4	Common mode rejection	CMR	25°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB
6	Output voltage, I_O = 5A	V_O	–55°C	+9V	R_L = 1Ω, R_{CL} = 0Ω	5		V
6	Output voltage, I_O = 36mA	V_O	–55°C	±19V	R_L = 500Ω	18		V
6	Output voltage, I_O = 2A	V_O	–55°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
6	Stability/noise	E_N	–55°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew rate	SR	–55°C	±18V	R_L = 500Ω	13	100	V/µs
6	Open loop gain	A_{OL}	–55°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
6	Common mode rejection	CMR	–55°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB
5	Output voltage, I_O = 3A	V_O	125°C	±7V	R_L = 1Ω, R_{CL} = 0Ω	3		V
5	Output voltage, I_O = 36mA	V_O	125°C	±19V	R_L = 500Ω	18		V
5	Output voltage, I_O = 2A	V_O	125°C	±12V	R_L = 5Ω, R_{CL} = 0Ω	10		V
5	Stability/noise	E_N	125°C	±15V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew rate	SR	125°C	±18V	R_L = 500Ω	8.5	100	V/µs
5	Open loop gain	A_{OL}	125°C	±15V	R_L = 500Ω, F = 10Hz	86		dB
5	Common mode rejection	CMR	125°C	±8.25V	R_L = 500Ω, F = DC, V_{CM} = ±2.25V	70		dB

BURN IN CIRCUIT



† 30 seconds after power applied.

* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

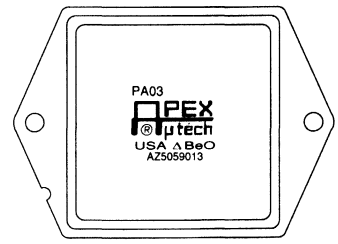
** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA03 • PA03A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- PD12/60C POWER DIP™ PACKAGE
- HIGH INTERNAL POWER DISSIPATION — 500 watts
- HIGH VOLTAGE OPERATION — ± 5V
- VERY HIGH CURRENT — ±30 amps
- INTERNAL SOA PROTECTION
- OUTPUT SWINGS CLOSE TO SUPPLY RAILS
- EXTERNAL SHUTDOWN CONTROL



APPLICATIONS

- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD DEFLECTION
- PROGRAMMABLE POWER SUPPLIES to ±72V
- TRANSDUCER/AUDIO TO 1000W

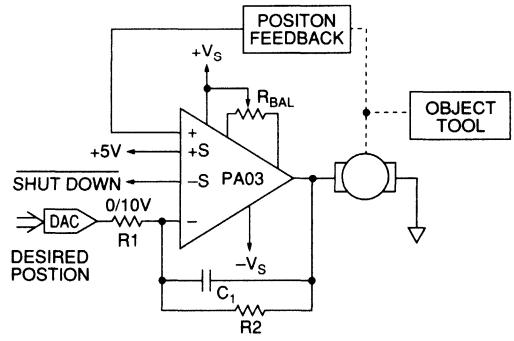
DESCRIPTION

The super power PA03 advances the state of the art in both brute force power and self protection against abnormal operating conditions. Its features start with a copper dip package developed by Apex to extend power capabilities well beyond those attainable with the familiar TO-3 package. The increased pin count of the new package provides additional control features, while the superior thermal conductivity of copper allows substantially higher power ratings.

The PA03 incorporates innovative current limiting circuits limiting internal power dissipation to a curve approximating the safe operating area of the power transistors. The internal current limit of 35A is supplemented with thermal sensing which reduces the current limit as the substrate temperature rises. Furthermore, a subcircuit monitors actual junction temperatures and with a response time of less than ten milliseconds reduces the current limit further to keep the junction temperature at 175°C.

The PA03 also features a laser trimmed high performance FET input stage providing superior DC accuracies both initially and over the full temperature range.

TYPICAL APPLICATION

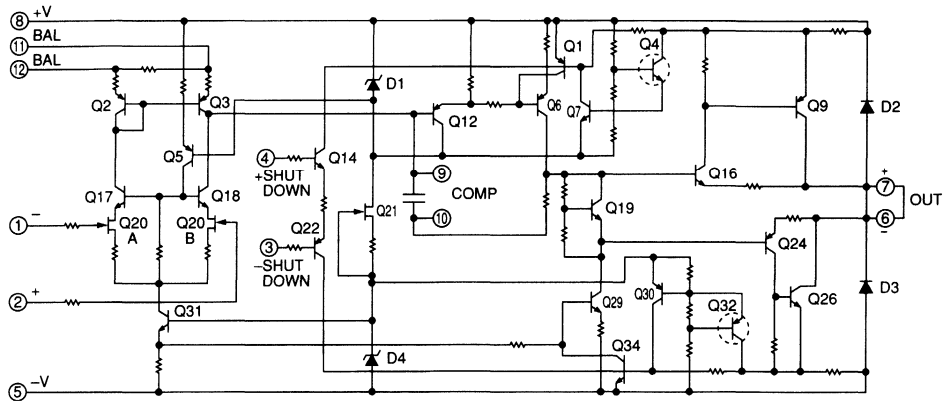


The PA03 output power stages contain fast reverse recovery diodes for sustained high energy flyback protection.

This hybrid integrated circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 Copper, 12-pin Power Dip™ package (see Package Outlines), is hermetically sealed and isolated from the internal circuits. Insulating washers are not recommended.

IMPORTANT: Observe mounting precautions.

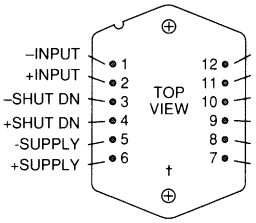
EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	150V
OUTPUT CURRENT, within SOA	Internally limited
POWER DISSIPATION, internal	500W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMP. RANGE, case	–55 to +125°C
SHUTDOWN VOLTAGE, differential	±5V
SHUTDOWN VOLTAGE, common mode	$\pm V_S$

EXTERNAL CONNECTIONS



Pins 6 & 7 must be connected together.

If unused, tie Pins 11 & 12 to +SUPPLY.

† **IMPORTANT: OBSERVE MOUNTING PRECAUTIONS. REVERSE INSERTION WILL DESTROY UNIT.**

SPECIFICATIONS

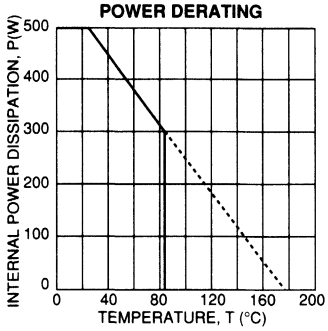
PARAMETER	TEST CONDITIONS[2]	PA03 MIN	PA03 TYP	PA03 MAX	PA03A MIN	PA03A TYP	PA03A MAX	UNITS
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		± .5	± 2		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	+ V_S –10V			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	108		*	*		dB
SHUTDOWN CURRENT[4]	Full temperature range		100			*		µA
SHUTDOWN VOLTAGE	Full temp. range, amp enabled			.85			*	V
SHUTDOWN VOLTAGE	Full temp. range, amp disabled	3.5			*			V
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	92	102		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 15A, V_O = 88V_{PP}		30			*		kHz
PHASE MARGIN	Full temp. range, C_C = 1.8nF		65			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 30mA	± V_S –7	6.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 12A	± V_S –5	4.2		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 146mA	± V_S –4	3.5		*	*		V
CURRENT, peak	T_C = 25°C		30		*			A
SETTLING TIME to .1%	T_C = 25°C, 10V step		8			*		µs
SLEW RATE	T_C = 25°C, C_C - open		8			*		V/µs
CAPACITIVE LOAD	Full temp. range, A_V = 1	2			*			nF
SHUTDOWN DELAY	T_C = –25°C, disable		10			*		µs
	T_C = –25°C, operate		20			*		µs
POWER SUPPLY								
VOLTAGE	Full temperature range	± 15	± 50	± 75	*	*	*	V
CURRENT, quiescent[6]	T_C = 25°C		125	300		*	*	mA
CURRENT, disable mode	Full temperature range		25	40		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, F>60Hz		.22	.28		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, F<60Hz		.25	.3		*	*	°C/W
RESISTANCE, junction to case	Full temperature range		14			*		°C/W
TEMPERATURE, junction	Sustained operation			150			*	°C
TEMPERATURE RANGE, case	Meets full range specification	– 25		85	*		*	°C

NOTES: * The specification of PA03A is identical to the specification for PA03 in applicable column to the left.

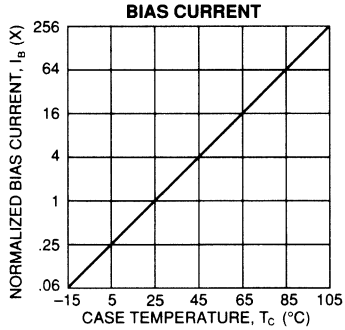
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if both shutdown inputs are least 1V inside supply rails. If one of the shutdown inputs is tied to a supply rail, the current in that pin may increase to 2.4mA.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. The PA03 must be used with a heatsink or the quiescent power may drive the unit into thermal shutdown.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

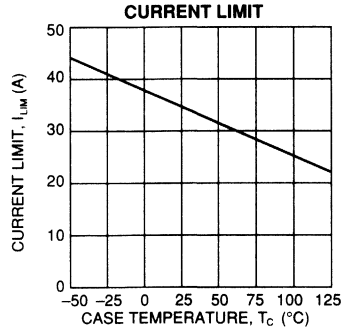
POWER DERATING



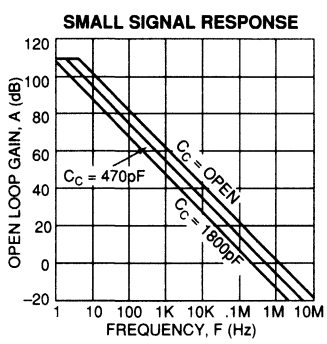
BIAS CURRENT



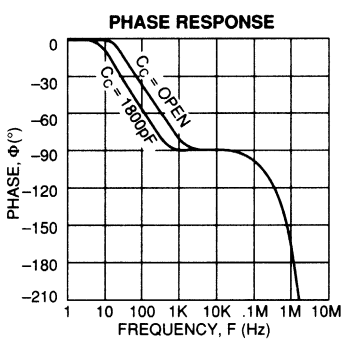
CURRENT LIMIT



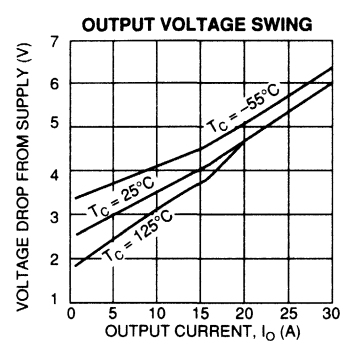
SMALL SIGNAL RESPONSE



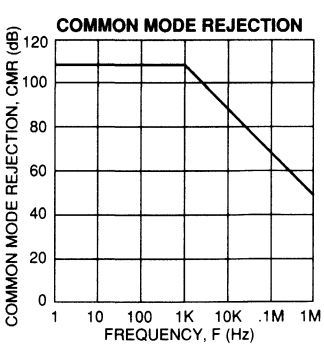
PHASE RESPONSE



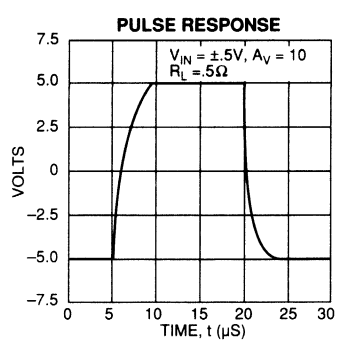
OUTPUT VOLTAGE SWING



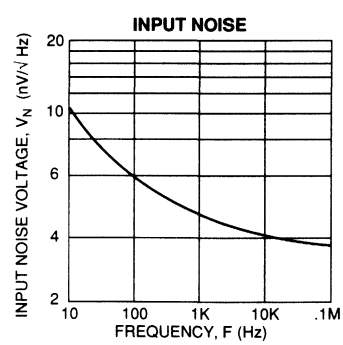
COMMON MODE REJECTION



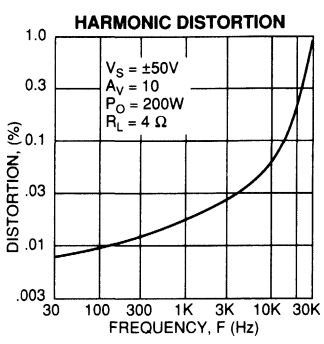
PULSE RESPONSE



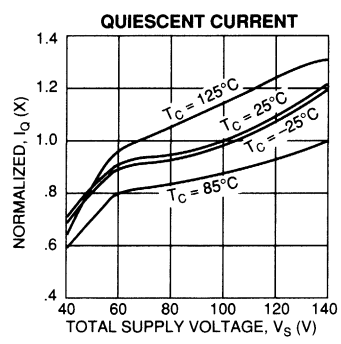
INPUT NOISE



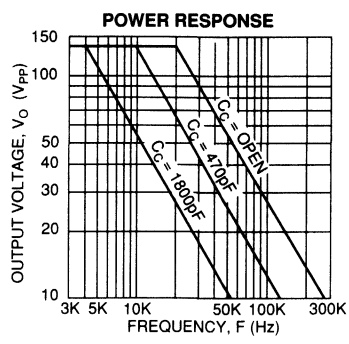
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

MOUNTING PRECAUTIONS

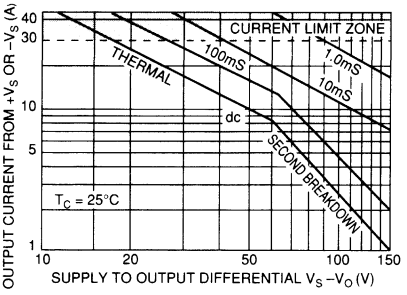
The PA03 copper base is very soft and easily bent. Do not put any stress on the mounting ears of this package. This calls for caution when pushing the amplifier into certain types of packaging foam and particularly when inserting the device into a socket. Insert the amplifier into the socket only by pushing on the perimeter of the package lid. Pushing the unit into the socket by applying pressure to the mounting tabs will bend the base due to the high insertion force required. The base will then not contact the heatsink evenly resulting in very poor heat transfer. To remove a unit from a socket, pry the socket away from the heatsink so that the heatsink will support the amplifier base evenly. Recommended mounting torque is 8–10 in.-lbs. (.9–1.13 N•m).

SAFE OPERATING AREA (SOA)

Due to the internal (non-adjustable) current limit of the PA03, worst case power dissipation calculations must assume current capability of 46 amps. Application specific circuits should be checked against the SOA curve when relying upon current limit for fault protection.

SAFE OPERATING AREA CURVES

Second breakdown limitations do apply to the PA03 but are less severe, since junction temperature limiting responds within 10ms. Stress levels shown as being safe for more than 10ms duration will merely cause thermal shutdown.



Under normal operating conditions, activation of the thermal shutdown is a sign that the internal junction temperatures have reached approximately 175°C. Thermal shutdown is a short term safety feature. If the conditions remain that cause thermal shutdown, the amplifier will oscillate in and out of shutdown, creating peak high power stresses, destroying useful signals, and reducing the reliability of the device.

BALANCE CONTROL

The voltage offset of the PA03 may be externally adjusted to zero. To implement this adjustment install a 100 to 200 ohm potentiometer between pins 11 and 12 and connect the wiper arm to the positive supply. Bypass pins 11 and 12 each with at least a .01µF ceramic capacitor.

If the optional adjust provision is not used, connect both pins 11 and 12 to the positive supply.

OUTPUT STAGE SHUTDOWN

The entire power stage of the PA03 may be disabled using one of the circuits shown in Figure 1. There are many applications for this function. One is a load protection based on power delivered to the load or thermal rise. Another one is conservation of power when using batteries. The control voltage requirements accommodate a wide variety logic drivers.

1. CMOS operating at +5V can drive the control pins directly.
2. CMOS operating at greater than 5V supplies need a voltage divider.
3. TTL logic needs a pull up resistor to +5V to provide a swing to the fully disabled voltage (3.5V). When not using the shutdown feature, connect both pins 3 and 4 to common.

PHASE COMPENSATION

At low gain settings an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered. A frequency of 1 MHz is most appropriate to calculate gain. Operation at gains below 10, without the external compensation capacitor opens the possibility of oscillations near output saturation regions when under load, the improper operation of the thermal shutdown circuit. This can result in amplifier destruction.

At gains of 10 or more:

1. No external components are required.
2. Typical slew rate will be 8V/µs.
3. Typical phase margin will be 70°.

At a gain of 3:

1. Connect a 470pF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 5V/µs.
3. Typical phase margin will be 45°.

At unity gain:

1. Connect a 1.8nF compensation capacitor between pins 9 and 10.
2. Typical slew rate will be 1.8V/µs.
3. Typical phase margin will be 65°.

FIGURE 1a. DIRECT DRIVE OF SHUTDOWN

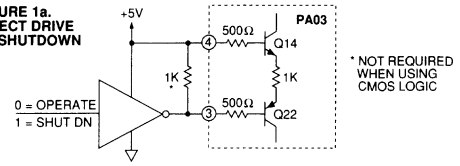


FIGURE 1b. HIGH VOLTAGE LOGIC INTERFACE

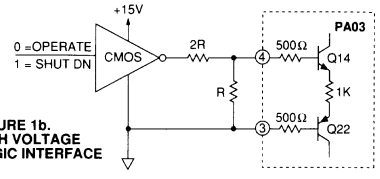
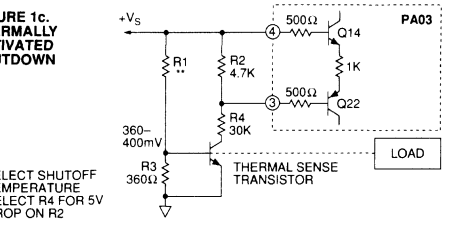


FIGURE 1c. THERMALLY ACTIVATED SHUTDOWN



PA04 • PA04A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- HIGH INTERNAL DISSIPATION — 200 WATTS
- HIGH VOLTAGE, HIGH CURRENT — 200V, 20A
- HIGH SLEW RATE — 50V/μS
- 4 WIRE CURRENT LIMIT SENSING
- LOW DISTORTION
- EXTERNAL SLEEP MODE CONTROL
- OPTIONAL BOOST VOLTAGE INPUTS
- EVALUATION KIT — SEE EK04

APPLICATIONS

- SONAR TRANSDUCER DRIVER
- LINEAR AND ROTARY MOTOR DRIVES
- YOKE/MAGNETIC FIELD EXCITATION
- PROGRAMMABLE POWER SUPPLIES TO ±95V
- AUDIO UP TO 400W

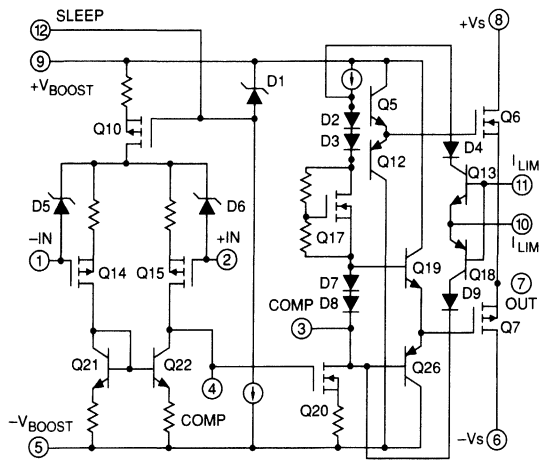
DESCRIPTION

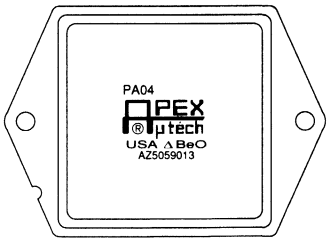
The PA04 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA04 is a highly flexible amplifier. The sleep mode feature allows ultra-low quiescent current for standby operation or load protection by disabling the entire amplifier. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line.

The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Do not use insulating washers.

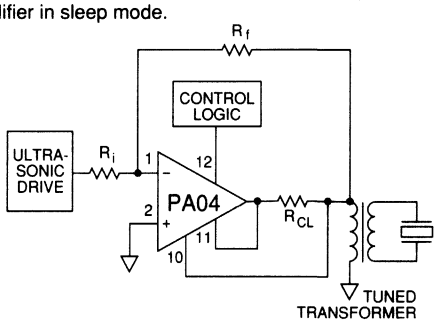
EQUIVALENT SCHEMATIC





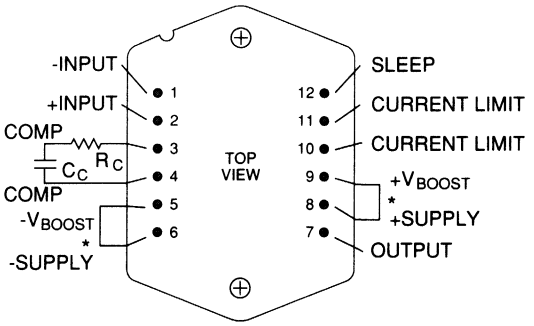
TYPICAL APPLICATION

The high power bandwidth and high voltage output of the PA04 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA04. Control logic turns off the amplifier in sleep mode.



Sonar Transducer Driver

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	100pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

*See "BOOST OPERATION" paragraph.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, within SOA	20A
POWER DISSIPATION, internal	200W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

		PA04			PA04A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			15			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_S$-8			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	98		*	*		dB
INPUT NOISE	100kHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 100pF	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	I_O = 10A		2			*		MHz
POWER BANDWIDTH	R_L = 4.5Ω, V_O = 180V p-p C_C = 100pF, R_C = 120Ω		90			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 15A	$\pm V_S$-8.8	$\pm V_S$-7.5		*	*		V
VOLTAGE SWING	V_{BOOST} = Vs + 5V, I_O = 20A	$\pm V_S$-5.8	$\pm V_S$-5.0		*	*		V
CURRENT, peak		20			*			A
SETTLING TIME to .1%	A_V = 1, 10V step, R_L = 4Ω		2.5			*		µs
SLEW RATE	A_V = 10, C_C = 100pF, R_C = 120Ω	40	50			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = +1	10			*			nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±75	±100	*	*	*	V
CURRENT, quiescent, boost supply			30	40		*	*	mA
CURRENT, quiescent, total			70	90		*	*	mA
CURRENT, quiescent, total, sleep mode	Full temperature range		3	5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.5	.6		*	*	°C/W
RESISTANCE[4], junction to air	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

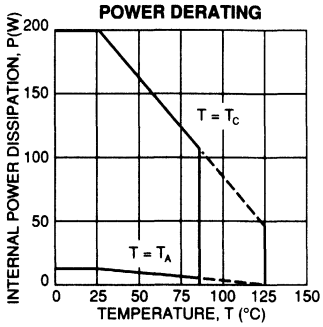
NOTES: * The specification of PA04A is identical to the specification for PA04 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA04 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

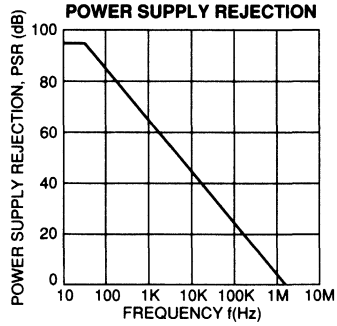
CAUTION The PA04 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

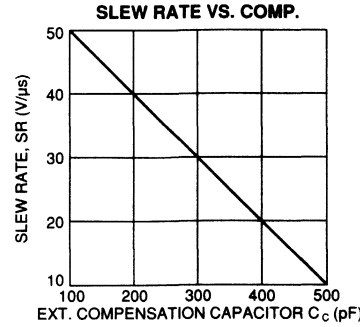
POWER DERATING



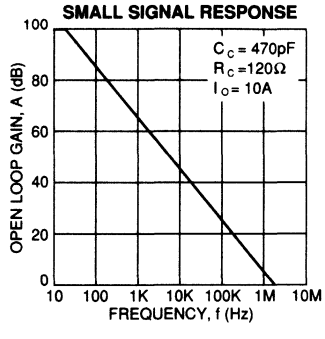
POWER SUPPLY REJECTION



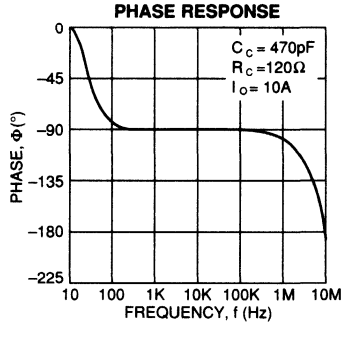
SLEW RATE VS. COMP.



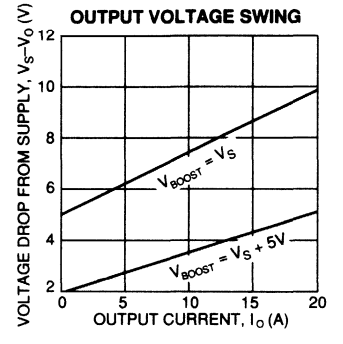
SMALL SIGNAL RESPONSE



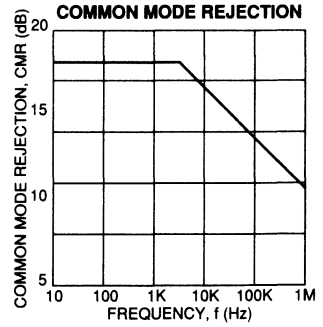
PHASE RESPONSE



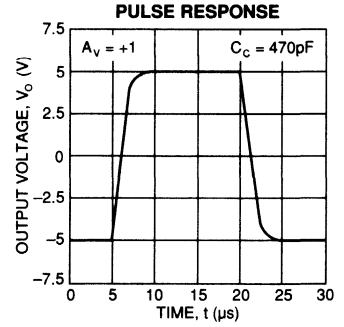
OUTPUT VOLTAGE SWING



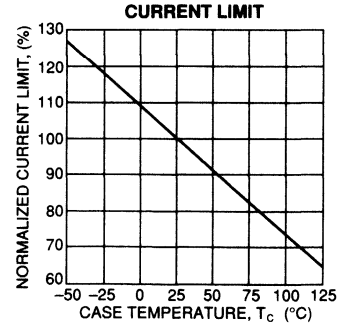
COMMON MODE REJECTION



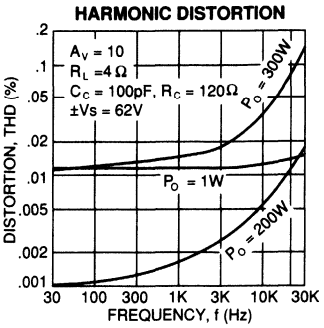
PULSE RESPONSE



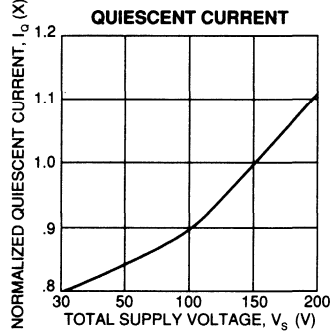
CURRENT LIMIT



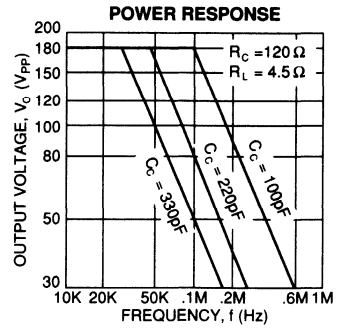
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook. The EK04 Evaluation Kit makes prototype circuits a snap by providing an EK04PC proto circuit board, MS05 mating socket, HS11 heatsink and hardware kit.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. **For the current limit to work correctly pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.** This connection will bypass any parasitic resistances, Rp, formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

$$R_{CL} = \frac{.76}{I_{LIMIT}}$$

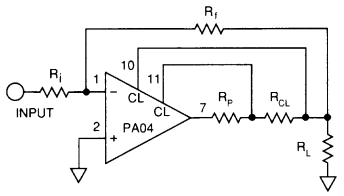


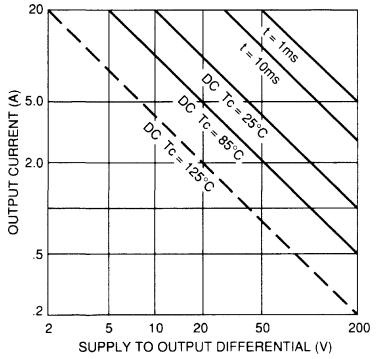
Figure 1.
Current Limit.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SLEEP MODE OPERATION

In the sleep mode, pin 12 (sleep) is tied to pin 9 ($+V_{BOOST}$). This disables the amplifier's internal reference and the amplifier shuts down except for a trickle current of 3 mA which flows into pin 12. Pin 12 should be left open if the sleep mode is not required.

Several possible circuits can be built to take advantage of this mode. In Figure 2A a small signal relay is driven by a logic gate. This removes the requirement to deal with the common mode voltage that exists on the shutoff circuitry since the sleep mode is referenced to the $+V_{BOOST}$ voltage.

In Figure 2B, circuitry is used to level translate the sleep mode input signal. The differential input activates sleep mode with a differential logic level signal and allows common mode voltages to $\pm V_{BOOST}$.

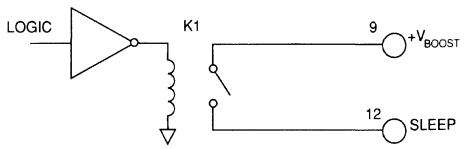


Figure 2A. Sleep mode circuit.

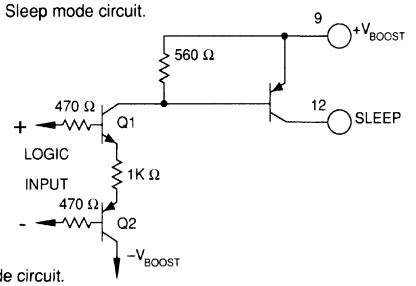


Figure 2B.
Sleep mode circuit.

BOOST OPERATION

With the V_{BOOST} feature the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9) and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

EVALUATION KIT FOR PA04 PIN-OUT

EK04

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of power op amps using the PA04 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations, and is flexible enough to do most standard amplifier test configurations.

The schematic of the PC board is shown in Figure 2. Note that all of the components shown on the schematic will probably not be used for any single circuit. The component locations on the PC board (See Figure 3) provide maximum flexibility for a variety of configurations. Also included are loops for current probes as well as connection pads on the edge of the PC board for easy interconnects.

The hardware required to mount the PC board and the device under evaluation to the heatsink are included in the kit. Because of the limitless combination of configurations and component values that can be used, no other parts are included in this kit. However, generic formulas and guidelines are included in the APEX HYBRID & IC HANDBOOK.

ASSEMBLY HINTS

The mating socket included with this kit has recessed nut sockets for mounting the device under evaluation. This allows assembly from one side of the heatsink, making it easy to swap devices under evaluation. The sizes of the stand-offs were selected to allow proper spacing of the board-to-heatsink and allow enough height for components when the assembly is inverted.

PARTS LIST

Part #	Description	Quantity
HS11	Heatsink	1
EK04PC	PC Board	1
MS05	Mating Socket	1
HWRE01	Hardware Kit	1

HWRE01 contains the following:

4	#8 Panhead Screws	4	#6 x 1.25" Panhead Screws
4	#8 .375" Hex Spacers	4	#6 x 5/16" Hex Nuts
4	#8 1.00" Hex Stand Offs	2	#6 x 1/4" Hex Nuts

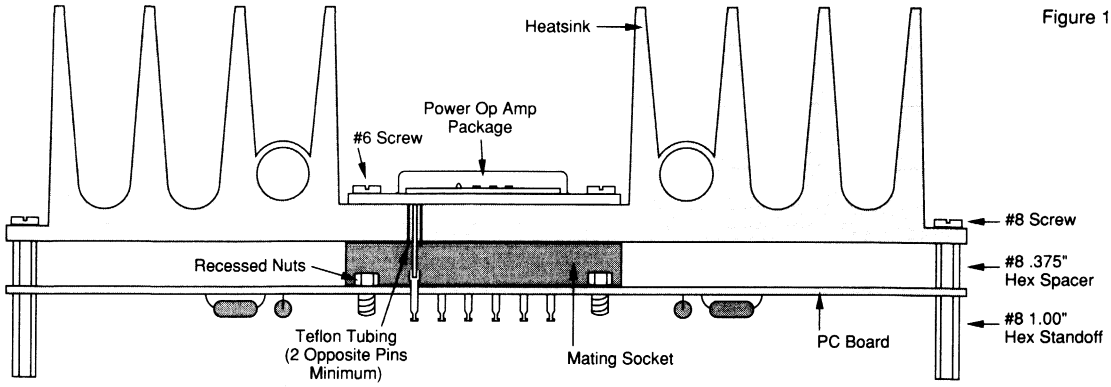
ASSEMBLY

1. Insert a #6 x 1/4" hex nut in each of the nut socket recesses located on the bottom of the mating socket.
2. Insert the socket into the PC board until it is firmly pressed against the ground plane side of the PC board.
3. Solder the socket in place (Figure 1). Be sure the nuts are in the recesses prior to soldering.
4. Mount the PC board assembly to the heatsink using the stand-offs and spacers included.
5. Apply thermal grease to the bottom of the device under evaluation. Insert into the mating socket through the heatsink.
6. Use the #6 x 1.25" panhead screws to mount the amplifier to the heat sink. **Do not overtorque.** Recommended mounting torque is 8-10 in-lbs (.90-1.13 N•M).

Mounting precautions, general operating considerations, and heatsinking information may be found in the APEX HYBRID & IC HANDBOOK.

NOTE: Refer to HS11 Heatsink note on page 3.

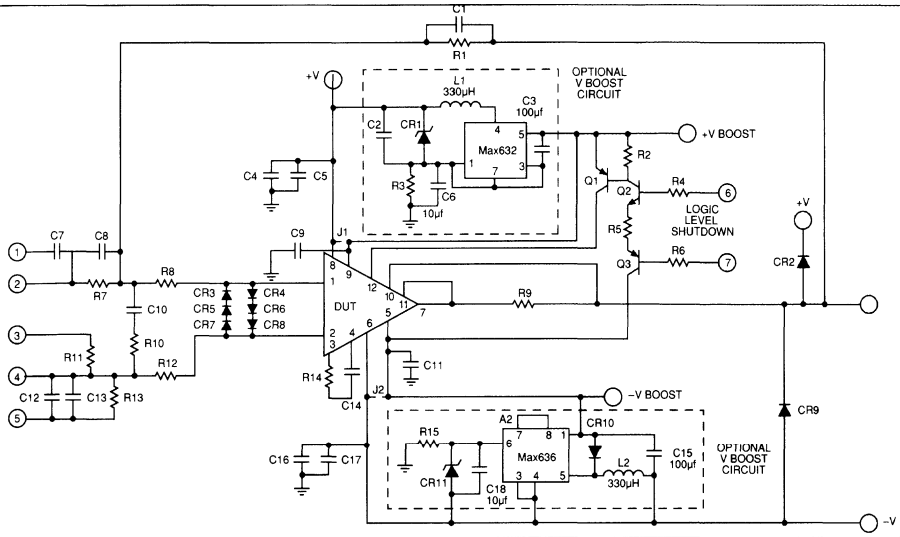
Figure 1



BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions!
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Always use the heatsink included in this kit with thermal grease and torque the part to the specified 8-10 in-lbs (.90-1.13 N•M).
- Do not change connections while the circuit is under power.
- Never exceed any of the absolute maximums listed in the device data sheet.
- Always use adequate power supply bypassing.
- Remember that internal power does not equal load power.
- Do not count on internal diodes to protect the output against sustained, high frequency, high energy kickback pulses.

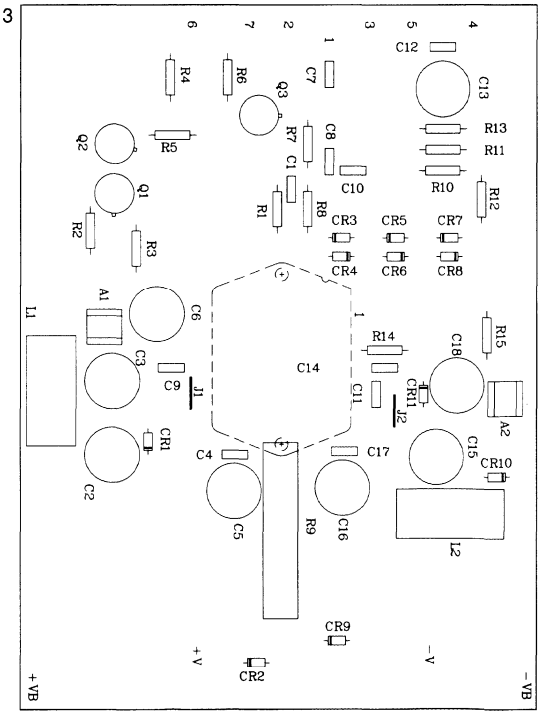
Figure 2



TYPICAL COMPONENT FUNCTIONS

COMPONENT	FUNCTION
R1	Feedback resistor
R2	Logic shutdown
R3	Current setting for CR1
R4	Input resistor logic input
R5	Current setting resistor
R6	Input resistor logic input
R7	Input resistor
R8	Input bias current measurement (Note 4)
R9	Current limit
R10	Noise gain compensation (Note 1)
R11	Resistor divider network for biasing inputs (Note 2)
R12	Input bias current measurement (Note 4)
R13	Resistor divider network for biasing inputs (Note 2)
R14	Compensation resistor
R15	Current setting for CR11
C1	AC gain or stability (Note 1)
C2	Power Supply Bypass (Note 3)
C3	Filter
C4	Power supply bypass (Note 3)
C5	Power supply bypass (Note 3)
C6	Power supply bypass (Note 3)
C7	Input coupling
C8	AC gain set
C9	Power supply bypass (Note 3)
C10	Noise gain compensation (Note 1)
C11	Power supply bypass (Note 3)
C12	Bias node noise bypass (Note 2)
C13	Bias node noise bypass (Note 2)
C14	Compensation
C15	Filter
C16	Power supply bypass (Note 3)
C17	Power supply bypass (Note 3)
C18	Power supply bypass (Note 3)
CR1	Zener reference for MAX632
CR2	Flyback protection (Note 5)
CR3-8	Input protection (Note 5)
CR9	Flyback protection (Note 5)
CR10	Flyback
CR11	Zener reference for MAX636

Figure 3



NOTES: Please refer to the following sections of the APEX HYBRID & IC HANDBOOK as noted.

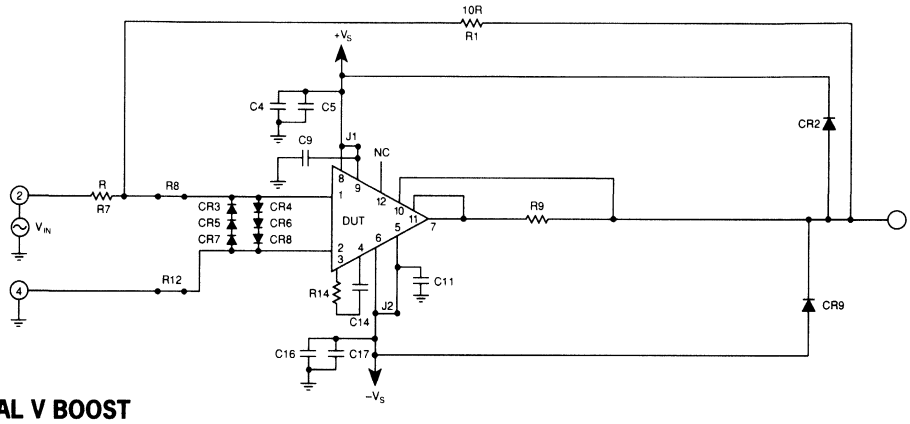
1. See Stability section of "General Operating Considerations."
2. See "General Operating Considerations."
3. See Power Supplies section of "General Operating Considerations."
4. See "Parameter Definitions and Test Methods."
5. See Amplifier Protection section of "General Operating Considerations."

TYPICAL APPLICATION

The PA04 is well suited for wideband, low distortion, high power applications. The circuit in Figure 4 displays the simplicity of use offered by the PA04. The circuit is in an inverting gain of 10. This relatively low gain allows the amplifier to have more than adequate loop gain available, resulting in extremely low distortion at the power levels delivered. The use of the inverting configuration avoids any concern of common mode effects. Typical specs of such a circuit would read as follows:

Po = 200W
F = 10kHz
R_L = 4 Ohms
THD = .0061

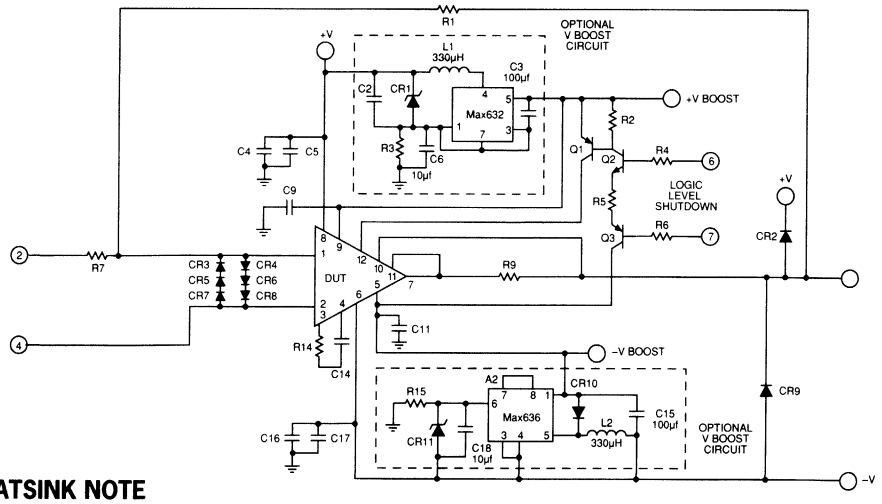
Figure 4



OPTIONAL V BOOST

One of many inexpensive ways to acquire V boost for the PA04 has been included as an option on this evaluation kit. The addition of these parts not only increases swing, but also extends the common mode range of the amplifier. All the formulas for calculating component values are in the vendor catalog.

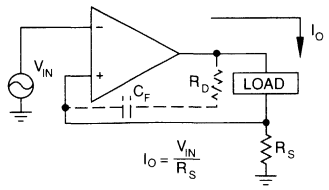
Figure 5



HS11 HEATSINK NOTE

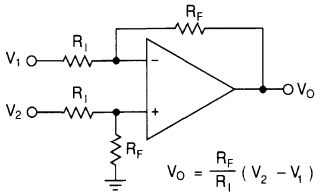
The HS11 Heatsink is provided in this evaluation kit to **guarantee** adequate **thermal** design through heat removal from the part under evaluation. Once maximum power dissipation for the application is determined (refer to "General Operating Considerations" and Application Note 11 in the APEX HYBRID & IC HANDBOOK), the final mechanical design will probably require substantially less heatsinking.

VOLTAGE-TO-CURRENT CONVERSION
NON-INVERTING CONFIGURATION



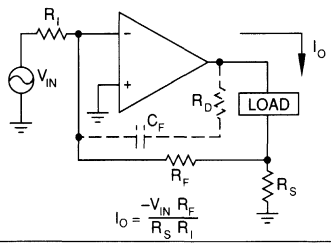
$$I_O = \frac{V_{IN}}{R_S}$$

DIFFERENCE AMPLIFIER



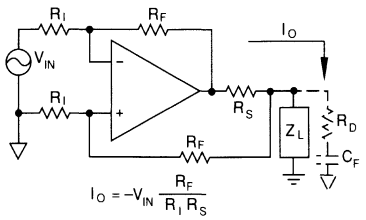
$$V_O = \frac{R_F}{R_I}(V_2 - V_1)$$

VOLTAGE-TO-CURRENT CONVERSION
INVERTING CONFIGURATION



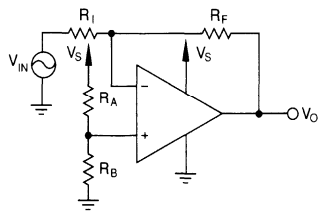
$$I_O = \frac{-V_{IN}\,R_F}{R_S\,R_I}$$

VOLTAGE-TO-CURRENT CONVERSION
IMPROVED HOWLAND CURRENT PUMP



$$I_O = -V_{IN}\frac{R_F}{R_I R_S}$$

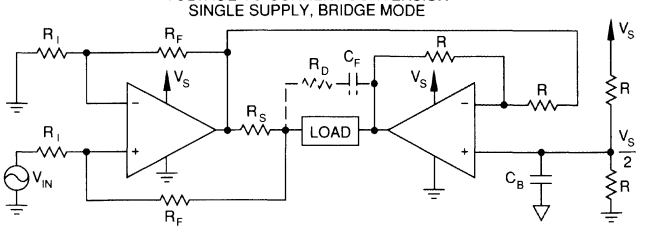
SINGLE SUPPLY OPERATION
INVERTING CONFIGURATION



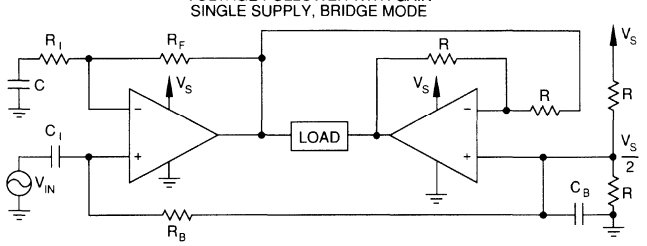
$$V_O\,(\text{Bias}) = \left(\frac{V_S}{R_A + R_B}\right)\left(1 + \frac{R_F}{R_I}\right)$$

$$V_O\,(\text{Signal}) = V_{IN}\left(-\frac{R_F}{R_I}\right)$$

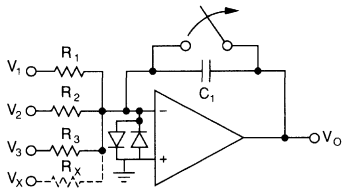
VOLTAGE-TO-CURRENT CONVERSION
SINGLE SUPPLY, BRIDGE MODE



VOLTAGE FOLLOWER WITH GAIN
SINGLE SUPPLY, BRIDGE MODE

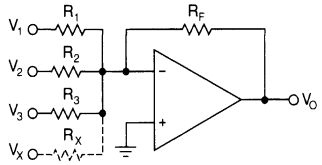


INTEGRATION



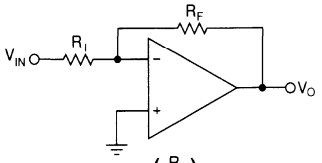
$$V_O = \frac{T}{C_1}\int_0^T \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)dt$$

SUMMING / SCALING



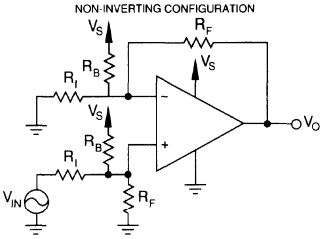
$$V_O = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)$$

INVERTER



$$V_O = -\left(\frac{R_F}{R_I}\right)V_{IN}$$

SINGLE SUPPLY
NON-INVERTING CONFIGURATION



i) $V_O = \frac{R_F}{R_I}$

ii) For $V_{IN} = 0$

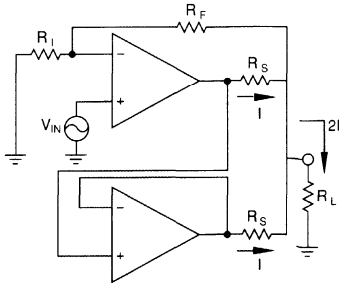
$$V_{CM} = \frac{V_S\,(R_I // R_F)}{R_B + (R_I // R_F)}$$

iii) $V_{CM\Delta} = \frac{V_{IN}\,(R_B // R_F)}{R_I + (R_B // R_F)}$

iv) For $V_{IN} > 0$

$$V_{CM} = V_{CM}\,@\,V_{IN} = 0 + V_{CM\Delta}$$

PARALLEL OPERATION



PA05 • PA05A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

PRELIMINARY

FEATURES

- **HIGH INTERNAL DISSIPATION — 250 WATTS**
- **HIGH VOLTAGE, HIGH CURRENT — 100V, 30A**
- **HIGH SLEW RATE — 100V/μS**
- **4 WIRE CURRENT LIMIT SENSING**
- **LOW DISTORTION**
- **EXTERNAL SHUTDOWN CONTROL**
- **OPTIONAL BOOST VOLTAGE INPUTS**
- **THERMALLY LIMITED OUTPUT STAGE**

APPLICATIONS

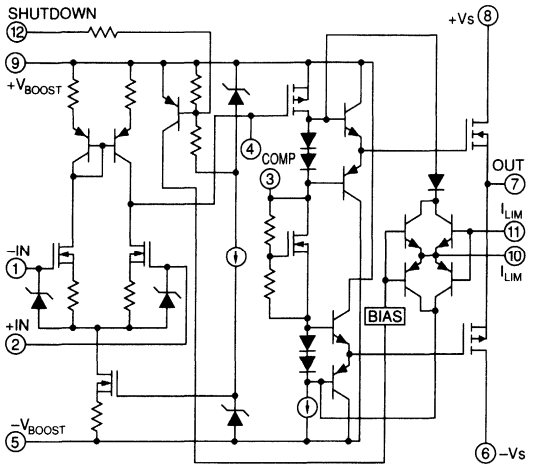
- **LINEAR AND ROTARY MOTOR DRIVES**
- **SONAR TRANSDUCER DRIVER**
- **YOKE/MAGNETIC FIELD EXCITATION**
- **PROGRAMMABLE POWER SUPPLIES TO ±45V**
- **AUDIO UP TO 500W**

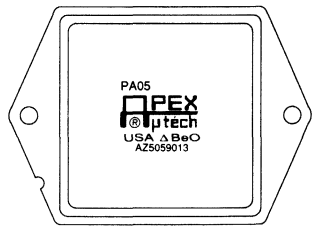
DESCRIPTION

The PA05 is a high voltage MOSFET power operational amplifier that extends the performance limits of power amplifiers in slew rate and power bandwidth, while maintaining high current and power dissipation ratings.

The PA05 is a highly flexible amplifier. The shutdown control feature allows the output stage to be turned off for standby operation or load protection during fault conditions. Boost voltage inputs allow the small signal portion of the amplifier to operate at a higher voltage than the high current output stage. The amplifier is then biased to achieve close linear swings to the supply rails at high currents for extra efficient operation. External compensation tailors slew rate and bandwidth performance to user needs. A four wire sense technique allows precision current limiting without the need to consider internal or external milliohm parasitic resistance in the output line. The output stage is protected by thermal limiting circuits above junction temperatures of 175°C.

EQUIVALENT SCHEMATIC

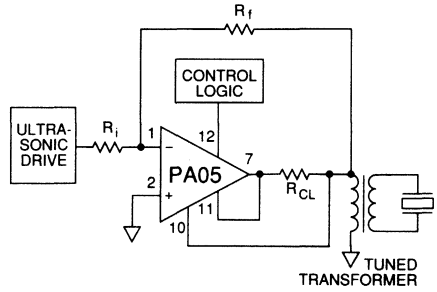




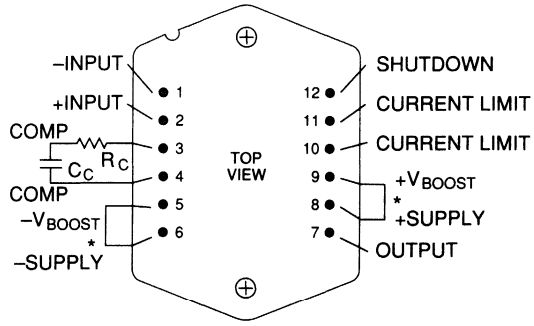
The JEDEC MO-127 12-pin Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Do not use insulating washers.

TYPICAL APPLICATION

The high power bandwidth of the PA05 allows driving sonar transducers via a resonant circuit including the transducer and a matching transformer. The load circuit appears resistive to the PA05. Control logic turns off the amplifier's output during shutdown.



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	470pF	120Ω
>3	220pF	120Ω
≥10	100pF	120Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

*See *BOOST OPERATION* paragraph.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
BOOST VOLTAGE	SUPPLY VOLTAGE +20V
OUTPUT CURRENT, within SOA	30A
POWER DISSIPATION, internal	250W
INPUT VOLTAGE, differential	±20V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[2]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

		PA05			PA05A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			5	10		2	5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		30	50		10	30	µV/°C
OFFSET VOLTAGE, vs. supply			10			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		30			10		µV/W
BIAS CURRENT, initial			10	50		5	20	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial			10	50		5	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			13			*		pF
COMMON MODE VOLTAGE RANGE	Full temperature range	$\pm V_S$–8			*			V
COMMON MODE REJECTION, DC	Full temp. range, V_{CM} = ±20V	86	98		*	*		dB
INPUT NOISE	100KHz BW, R_S = 1KΩ		10			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	Full temperature range, C_C = 100pF	94	102		*	*		dB
GAIN BANDWIDTH PRODUCT	I_O = 10A		3			*		MHz
POWER BANDWIDTH	R_L = 4.5Ω, V_O = $90V_{P-P}$ C_C = 100pF, R_C = 120Ω		360			*		kHz
PHASE MARGIN	Full temperature range, C_C = 330pF		60			*		°
OUTPUT								
VOLTAGE SWING	I_O = 20A	$\pm V_S$–8.8	$\pm V_S$–7.5		*	*		V
VOLTAGE SWING	V_{BOOST} = Vs + 5V, I_O = 30A	$+V_S$–5.8	$+V_S$–5.0		*	*		V
CURRENT, peak		30			*			A
SETTLING TIME to .1%	A_V = 1, 10V step, R_L = 4Ω		2.5			*		µs
SLEW RATE	A_V = 10, C_C = 100pF, R_C = 120Ω	80	100			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = +1	10			*			nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±15	±45	±50	*	*	*	V
CURRENT, quiescent, boost supply			46	56		*	*	mA
CURRENT, quiescent, total			90	120		*	*	mA
CURRENT, quiescent, total, shutdown	Full temperature range		46	56		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	Full temperature range, F>60Hz		.3	.4		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F<60Hz		.4	.5		*	*	°C/W
RESISTANCE, junction to air[4]	Full temperature range		12			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

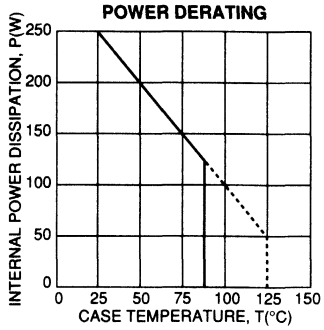
NOTES: * The specification of PA05A is identical to the specification for PA05 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, C_C = 470pF, R_C = 120 ohms. DC input specifications are ± value given. Power supply voltage is typical rating. $\pm V_{BOOST} = \pm V_S$.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to the heatsink data sheet.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.
4. The PA05 must be used with a heatsink or the quiescent power may drive the unit to junction temperatures higher than 150°C.

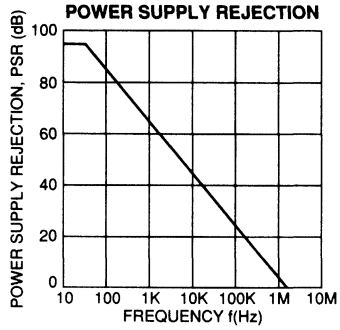
CAUTION The PA05 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

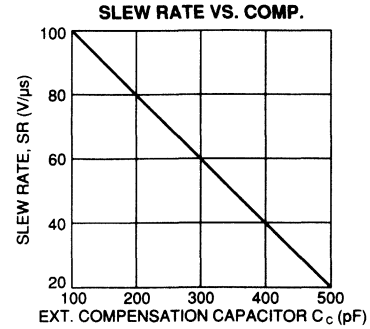
POWER DERATING



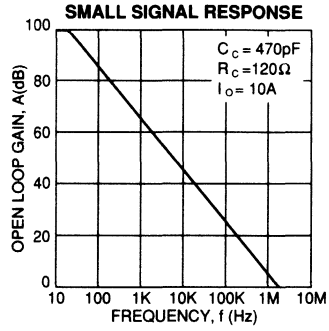
POWER SUPPLY REJECTION



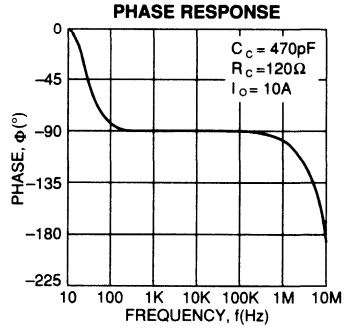
SLEW RATE VS. COMP.



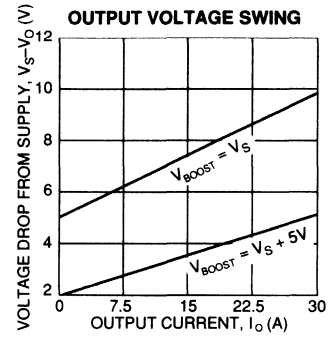
SMALL SIGNAL RESPONSE



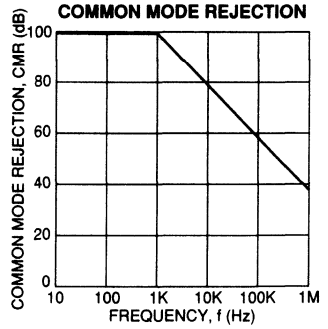
PHASE RESPONSE



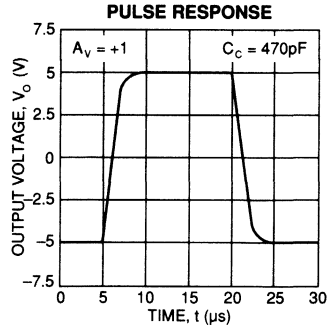
OUTPUT VOLTAGE SWING



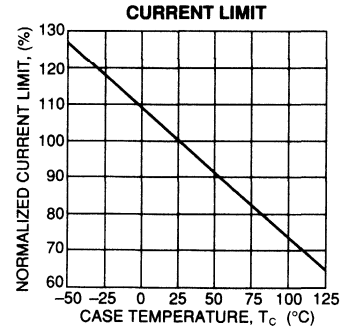
COMMON MODE REJECTION



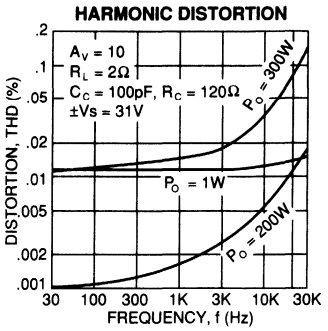
PULSE RESPONSE



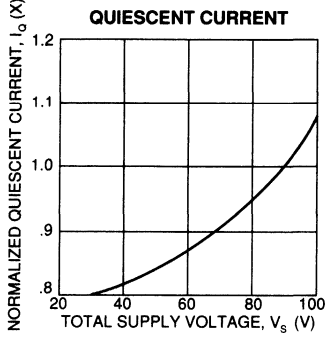
CURRENT LIMIT



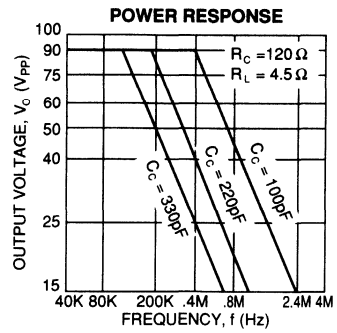
HARMONIC DISTORTION



QUIESCENT CURRENT



POWER RESPONSE



GENERAL

Please read the *General Operating Considerations* section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the *Accessory and Package Mechanical Data* section of the handbook. The EK04 Evaluation Kit makes prototype circuits a snap by providing an EK04PC proto circuit board, MS05 mating socket, HS11 heatsink and hardware kit.

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. *For the current limit to work correctly, pin 11 must be connected to the amplifier output side and pin 10 connected to the load side of the current limit resistor, R_{CL}, as shown in Figure 1.* This connection will bypass any parasitic resistances, R_P formed by sockets and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 1.

The value of the current limit resistor can be calculated as follows:

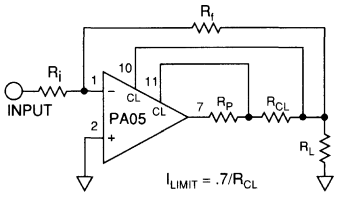


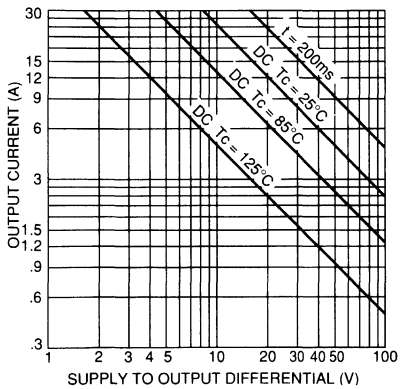
FIGURE 1. CURRENT LIMIT

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



SHUTDOWN OPERATION

To disable the output stage, pin 12 is connected to ground via relay contacts or via an electronic switch. The switching device must be capable of sinking 2mA to complete shutdown and capable of standing off the supply voltage $+V_S$. See Figure 2 for suggested circuits.

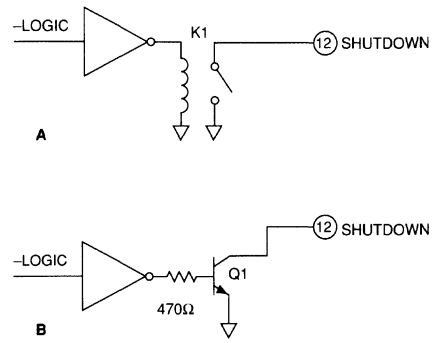


FIGURE 2. SHUTDOWN OPERATION

BOOST OPERATION

With the V_{BOOST} feature, the small signal stages of the amplifier are operated at higher supply voltages than the amplifier's high current output stage. $+V_{BOOST}$ (pin 9), and $-V_{BOOST}$ (pin 5) are connected to the small signal circuitry of the amplifier. $+V_S$ (pin 8) and $-V_S$ (pin 6) are connected to the high current output stage. An additional 5V on the V_{BOOST} pins is sufficient to allow the small signal stages to drive the output transistors into saturation and improve the output voltage swing for extra efficient operation when required. When close swings to the supply rails is not required the $+V_{BOOST}$ and $+V_S$ pins must be strapped together as well as the $-V_{BOOST}$ and $-V_S$ pins. The boost voltage pins must not be at a voltage lower than the V_S pins.

COMPENSATION

The external compensation components C_C and R_C are connected to pins 3 and 4. Unity gain stability can be achieved at any compensation capacitance greater than 330 pF with at least 60 degrees of phase margin. At higher gains, more phase shift can be tolerated in most designs and the compensation capacitance can accordingly be reduced, resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C and R_C for the application.

FET INPUT POWER OPERATIONAL AMPLIFIERS

PA07 • PA07A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421 1865

FEATURES

- LOW BIAS CURRENT — FET Input
- PROTECTED OUTPUT STAGE — Thermal Shutoff
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±12V TO ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

APPLICATIONS

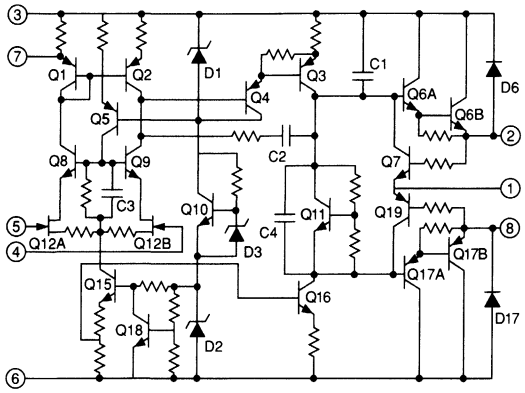
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

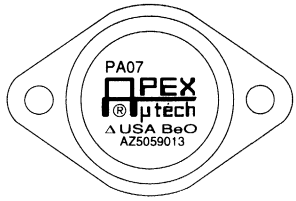
DESCRIPTION

The PA07 is a high voltage, high output current operational amplifier designed to drive resistive, inductive and capacitive loads. Its complementary darlington emitter follower output stage is protected against transient inductive kickback. For optimum linearity, especially at low levels, the output state is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. A thermal shutoff circuit protects against overheating and minimizes heatsink requirements for abnormal operating conditions. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

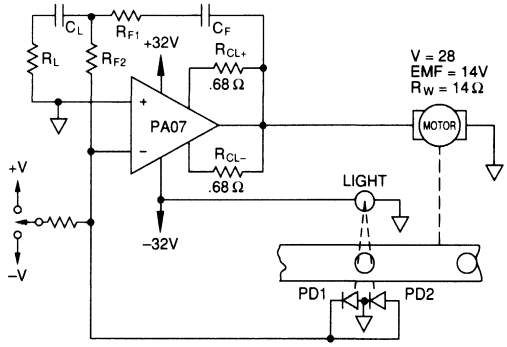
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





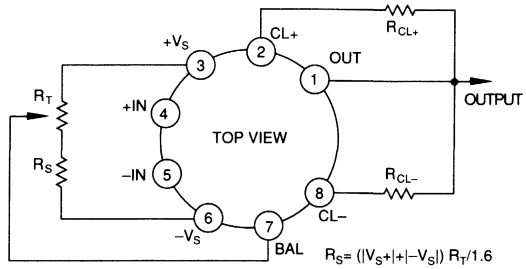
TYPICAL APPLICATION



Negates optoelectronic instabilities
Lead network minimizes overshoot
SEQUENTIAL POSITION CONTROL

Position is sensed by the differentially connected photo diodes, a method that negates the time and temperature variations of the optical components. Off center positions produce an error current which is integrated by the op amp circuit, driving the system back to center position. A momentary switch contact forces the system out of lock and then the integrating capacitor holds drive level while both diodes are in a dark state. When the next index point arrives, the lead network of C1 and R1 optimize system response by reducing overshoot. The very low bias current of the PA07 augments performance of the integrator circuit.

EXTERNAL CONNECTIONS



NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX
8-pin TO-3 package

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	67W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

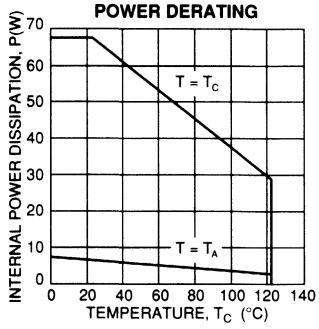
		PA07			PA07A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		8			*		µV/V
OFFSET VOLTAGE, vs. power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT,vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	Full temperature range, V_{CM} = ±20V		120			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	92	98		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, R_L = 15Ω		1.3			*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L = 15Ω		18			*		kHz
PHASE MARGIN	Full temperature range, R_L = 15Ω		70			*		°
OUTPUT								
VOLTAGE SWING[4]	Full temp. range, I_O = 5A	$\pm V_S$–5			*			V
VOLTAGE SWING[4]	Full temp. range, I_O = 2A	$\pm V_S$–5			*			V
VOLTAGE SWING[4]	Full temp. range, I_O = 90mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		1.5			*		µs
SLEW RATE	T_C = 25°C		5			*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±12	±35	±50	*	*	*	V
CURRENT, quiescent	T_C = 25°C		18	30		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F>60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	F<60Hz		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+85	*	*	*	°C

NOTES: * The specification of PA07A is identical to the specification for PA07 in applicable column to the left.

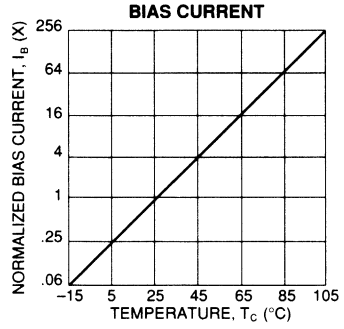
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

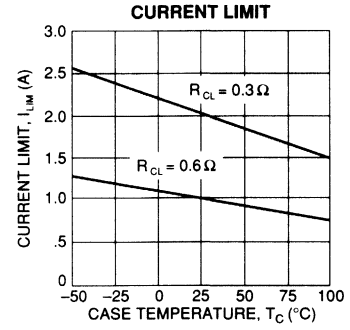
POWER DERATING



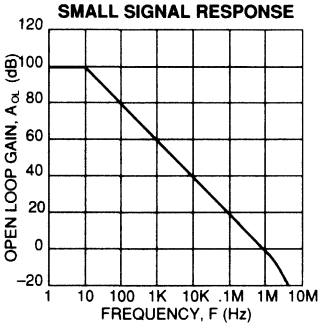
BIAS CURRENT



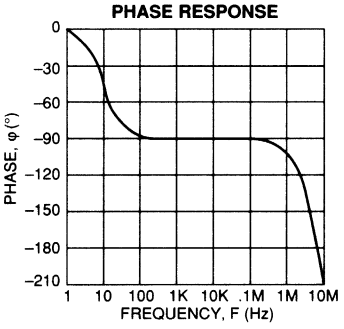
CURRENT LIMIT



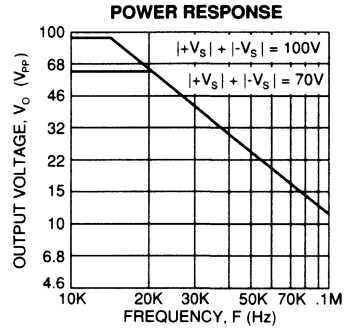
SMALL SIGNAL RESPONSE



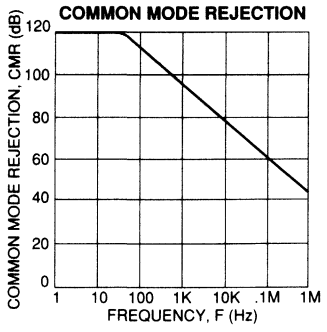
PHASE RESPONSE



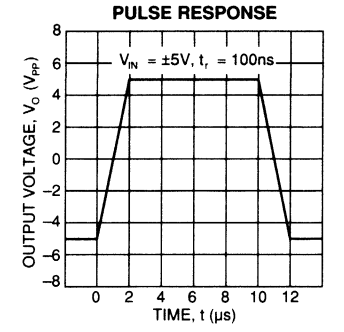
POWER RESPONSE



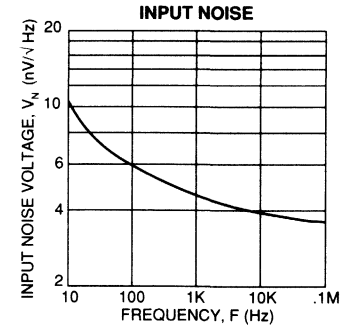
COMMON MODE REJECTION



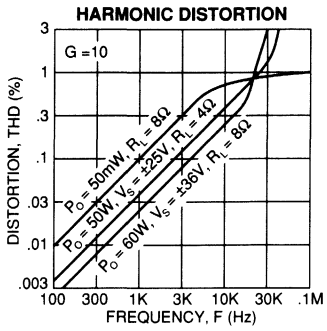
PULSE RESPONSE



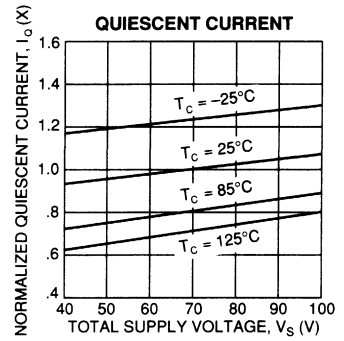
INPUT NOISE



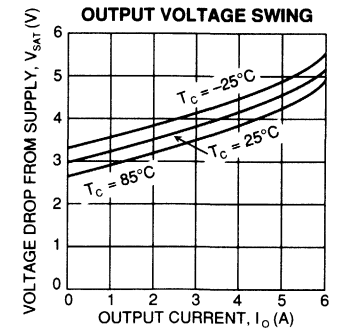
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



GENERAL

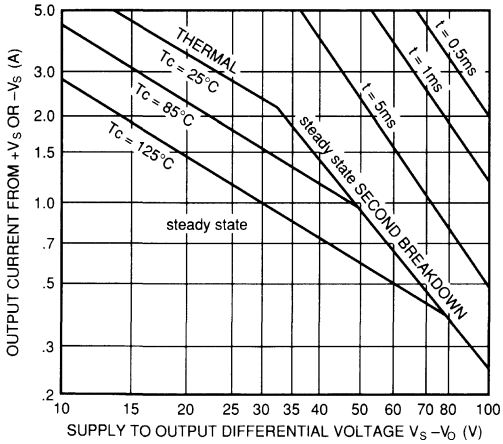
Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.
3. The junction temperature of the output transistors.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and inductive* loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
50V	80µF	75µF	55mH	7.5mH
40V	250µF	150µF	150mH	11mH
30V	1,200µF	500µF	250mH	24mH
20V	20mF	5mF	1.5H	75mH
15V	∞	25mF	∞	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 12V below the supply rail with I_{LIM} = 5A or 32V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any reactive or EMF generating load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.25A	.82A
40V	.37A	1.4A
30V	.65A	2.1A
20V	1.4A	3.3A
15V	2.1A	4.5A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

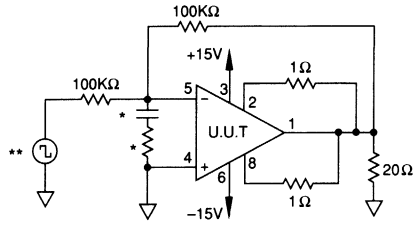
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity and reduce the reliability of the device.

CURRENT LIMIT

Proper operation requires the use of two current limit resistors, connected as shown in the external connections diagram. The minimum value for R_{CL} is .13Ω, however, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		30	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		4.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±50V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±35V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		46	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		6.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±50V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		30	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		7.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±50V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 5A	V_O	25°C	±15.3V	R_L = 2.07Ω	10.3		V
4	Output Voltage, I_O = 90mA	V_O	25°C	±50V	R_L = 500Ω	45		V
4	Output Voltage, I_O = 2A	V_O	25°C	±29V	R_L = 12Ω	24		V
4	Current Limits	I_{CL}	25°C	±16V	R_L = 2.07Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/Noise	E_N	25°C	±35V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500Ω	2.5	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500Ω, F = 10Hz	92		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB
6	Output Voltage, I_O = 5A	V_O	–55°C	±15.3V	R_L = 2.07Ω	10.3		V
6	Output Voltage, I_O = 90mA	V_O	–55°C	±50V	R_L = 500Ω	45		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±29V	R_L = 12Ω	24		V
6	Stability/Noise	EN	–55°C	±35V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500Ω	2.5	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500Ω, F = 10Hz	90		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB
5	Output Voltage, I_O = 3A	V_O	125°C	±11.3V	R_L = 2.07Ω	6.3		V
5	Output Voltage, I_O = 90mA	V_O	125°C	±50V	R_L = 500Ω	45		V
5	Output Voltage, I_O = 2A	V_O	125°C	±29V	R_L = 12Ω	24		V
5	Stability/Noise	E_N	125°C	±35V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500Ω	1.25	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500Ω, F = 10Hz	92		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±24.5V	80		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA08 • PA08A

FEATURES

- **WIDE SUPPLY RANGE — ±15V to ±150V**
- **PROGRAMMABLE OUTPUT CURRENT LIMIT**
- **HIGH OUTPUT CURRENT — Up to ±150mA**
- **LOW BIAS CURRENT — FET Input**
- **PROTECTED OUTPUT STAGE — Thermal Shutoff**

APPLICATIONS

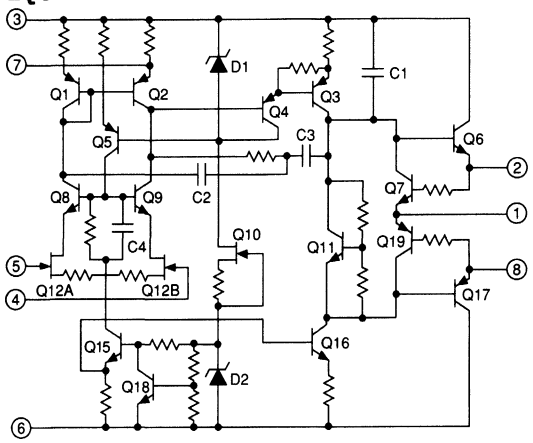
- **HIGH VOLTAGE INSTRUMENTATION**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PROGRAMMABLE POWER SUPPLIES UP TO 290V**
- **ANALOG SIMULATORS**

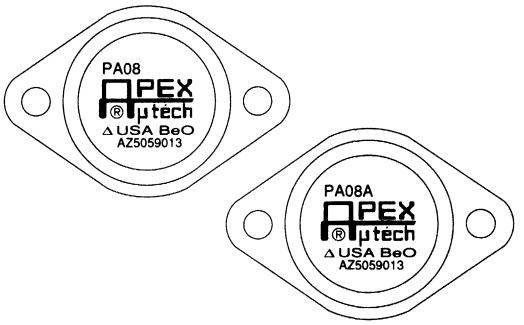
DESCRIPTION

The PA08 is a high voltage operational amplifier designed for output voltage swings of up to ±145V with a dual (±) supply or 290V with a single supply. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

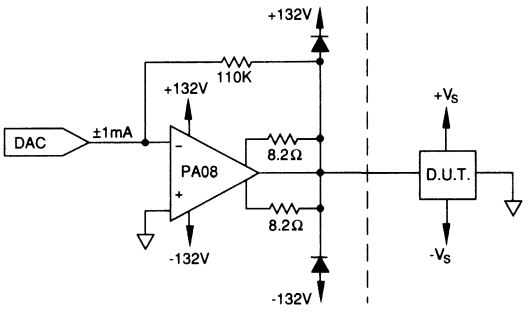
This hybrid integrated circuit utilizes beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





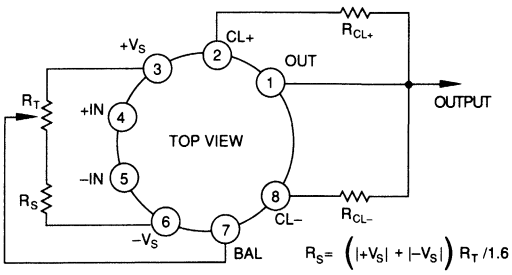
TYPICAL APPLICATION



ATE PIN DRIVER

The PA08 as a pin driver is capable of supplying high test voltages to a device under test (DUT). Due to the possibility of short circuits to any terminal of the DUT, current limit must be set to be safe when limiting with a supply to output voltage differential equal to the amplifier supply plus the largest magnitude voltage applied to any other pin of the DUT. In addition, flyback diodes are recommended when the output of the amplifier exits any equipment enclosure to prevent damage due to electrostatic discharges. Refer to Application Note 7 for details on accuracy considerations of this circuit.

EXTERNAL CONNECTIONS



$R_S = \left(|+V_S| + |-V_S|\right) R_T / 1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	200mA
POWER DISSIPATION, internal at T_C = 25°C	17.5W
INPUT VOLTAGE, differential	±50V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

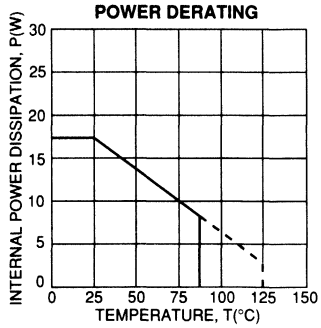
SPECIFICATIONS

		PA08			PA08A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±2		±.25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25°C to +85°C		±15	±30		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			*	2	µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√W
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^5			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		4			*		pF
COMMON MODE VOLTAGE RANGE[4]	T_C = –25°C to +85°C	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	T_C = –25°C to +85°C, V_{CM} = ±90V		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L= ∞		118			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L= 1.2KΩ	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, R_L= 1.2KΩ		5			*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L= 1.2KΩ		90			*		kHz
PHASE MARGIN	T_C = –25 to +85°C		60			*		°
OUTPUT								
VOLTAGE SWING[4]	T_C = 25°C, I_O = 150mA	$\pm V_S$–15	$\pm V_S$–8		*	*		V
VOLTAGE SWING[4]	T_C = –25° C to +85°C, I_O = ±75mA	$\pm V_S$–10	$\pm V_S$–5		*	*		V
VOLTAGE SWING[4]	T_C = –25° C to +85°C, I_O = ±20mA	$\pm V_S$–5	$\pm V_S$–3		*	*		V
CURRENT, peak	T_C = 85°C	150			*			mA
SLEW RATE	T_C = 25°C		30		20	*		V/µs
CAPACITIVE LOAD, A_V = 1	T_C = –25 to +85°C			10			*	nF
CAPACITIVE LOAD, A_V > 4	T_C = –25 to +85°C			SOA			*	
SETTLING TIME to .1%	T_C = 25°C, R_L= 1.2KΩ, 2V step		1			*		µs
POWER SUPPLY								
VOLTAGE	T_C = –55 to +125°C	±15	±100	±150	*	*	*	V
CURRENT, quiescent	T_C = 25°C		6	8.5		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	T_C = –55 to +125°C, F > 60Hz		3.8			*		°C/W
RESISTANCE, DC junction to case	T_C = –55 to +125°C, F < 60Hz		6.0	6.5		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		85	*		*	°C

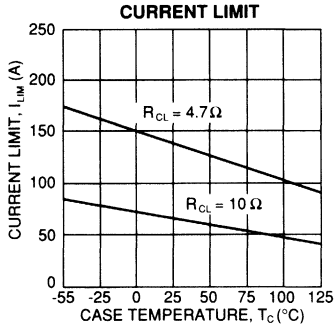
NOTES: * The specification of PA08A is identical to the specification for PA08 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage specified under typical (TYP) applies unless otherwise noted.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

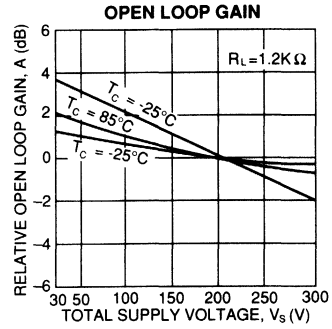
POWER DERATING



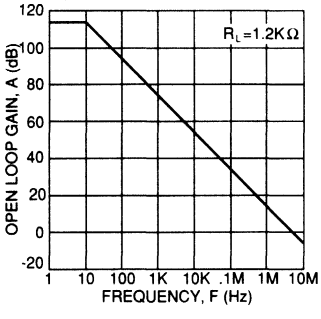
CURRENT LIMIT



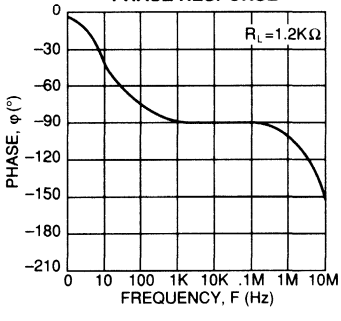
OPEN LOOP GAIN



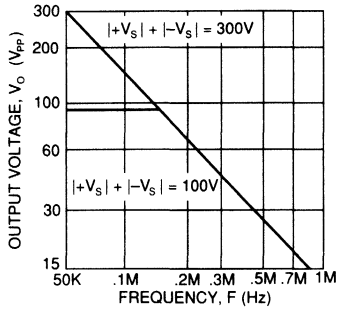
SMALL SIGNAL RESPONSE



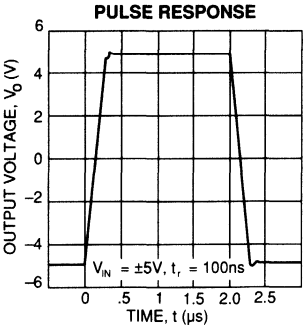
PHASE RESPONSE



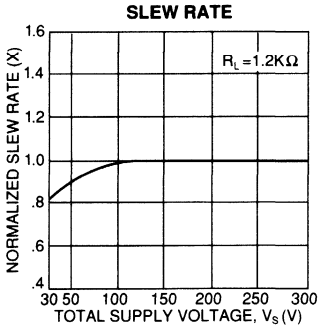
POWER RESPONSE



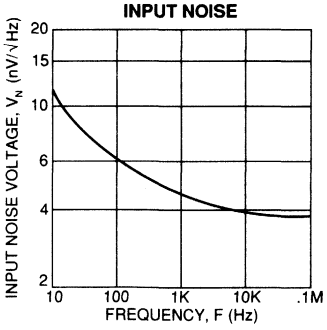
PULSE RESPONSE



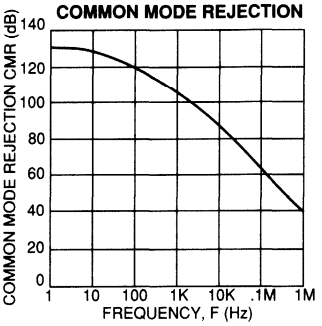
SLEW RATE



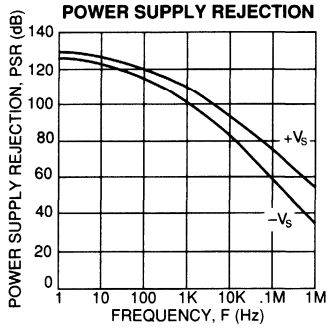
INPUT NOISE



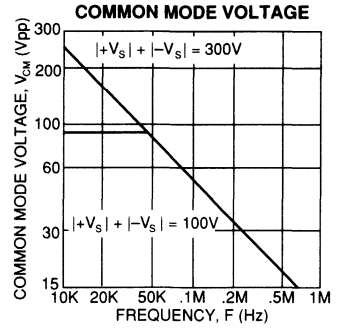
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



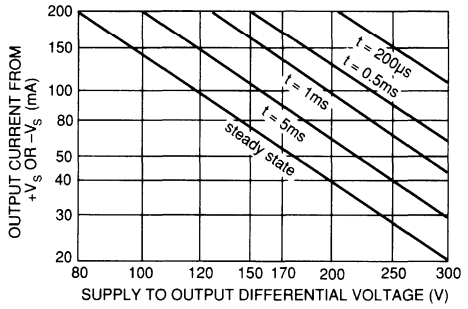
GENERAL

Please read the "General Operating Considerations", which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, see the "Package Outlines" and "Accessories" sections of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has two distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Under transient conditions, the following capacitive and inductive loads are safe with the current limits set to the maximum:

$\pm V_S$	C(MAX)	L(MAX)
150V	.4µF	280mH
125V	.9µF	380mH
100V	2µF	500mH
75V	10µF	1200mH
50V	100µF	13H

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rails or simple shorts to common if the current limits are set as follows:

$\pm V_S$	SHORT TO $\pm V_{SC}$, C, L, OR EMF LOAD	SHORT TO COMMON
150V	20mA	67mA
125V	27mA	90mA
100V	42mA	130mA
75V	67mA	200mA
50V	130mA	200mA

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation with the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

INDUCTIVE LOADS

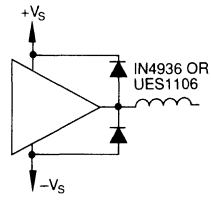
Two external diodes as shown in Figure 1, are required to protect these amplifiers from flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

INPUT PROTECTION

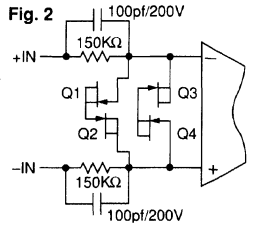
The input is protected against common mode voltages up to the supply rails and differential voltages up to ±50V. Increased protection against differential input voltages can be obtained by adding 2 resistors, 2 capacitors and 4 diode connected FETs as shown in Figure 2.

Fig. 1



PROTECTION, INDUCTIVE LOAD

Fig. 2



PROTECTION, OVERVOLTAGE

CURRENT LIMITING

Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is 3.24Ω. However, for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

PA08V

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- **EXTENDED SUPPLY RANGE**
  UP TO ±175V or
  350V TOTAL
- **PROVIDES PA08 PERFORMANCE**
  UP TO ±150mA
  PROGRAMMABLE CURRENT LIMIT
  LOW DRIFT FET INPUT

APPLICATIONS

- **PROGRAMMABLE POWER SUPPLIES UP TO 340V**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PIEZO ELECTRIC TRANSDUCERS**
- **HIGH VOLTAGE INSTRUMENTATION**

DESCRIPTION

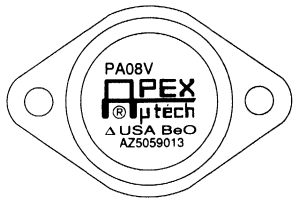
The PA08 is an extended supply range operational amplifier capable of output voltage swings of ±170V with dual supplies or 340V total supply voltage on single or non-symmetric supplies.

High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA08 features an unprecedented supply range and excellent supply rejection. The output stage is biased class A-B for linear operation. Internal phase compensation assures stability at all gain settings. The safe operating area (SOA) can be observed with all types of loads by choosing the appropriate current limiting resistors. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin to TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

SPECIFICATIONS

Specifications of the standard PA08 apply with the benefit of supply ratings being extended to ±175V. Design changes enabling the total supply rating of 350V have no effect on the shape of the typical performance graphs.



GENERAL CONSIDERATIONS

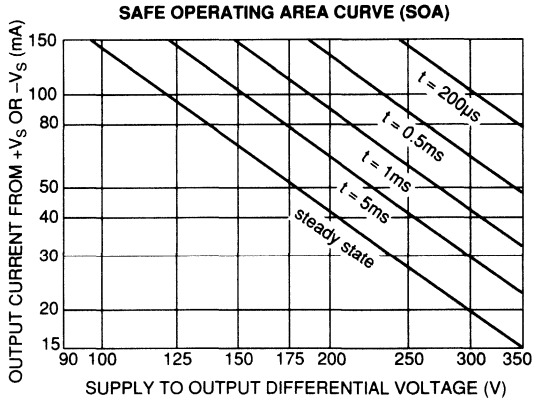
SAFE OPERATING AREA

The extended safe operating area is as follows:

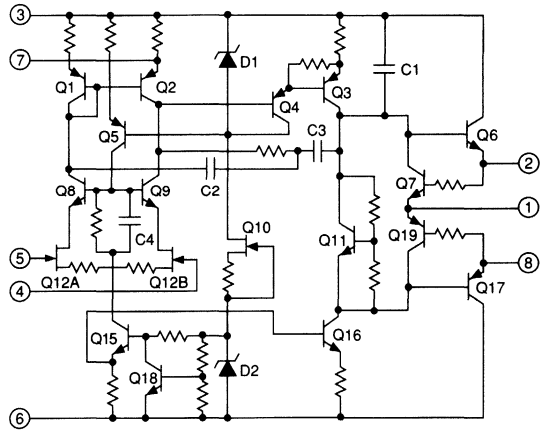
When operating on ±175V, maximum safe values of capacitive and inductive loading are .2µF and 200mH. Maximum safe current limit for a short to common is 50mA, and for a short to supply rails, the maximum is 15mA.

Please consult the PA08 data sheet for basic information on this amplifier, plus the application notes in this APEX Power Op Amp Handbook, for recommendations on stability, current limiting, heatsinks, bypassing, and suggestions for circuit functions.

SAFE OPERATING AREA CURVE (SOA)

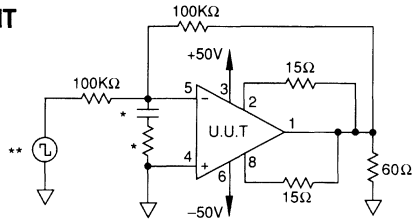


EQUIVALENT SCHEMATIC



SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±100V	V_{IN} = 0, A_V = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±100V	V_{IN} = 0, A_V = 100		2	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		3.7	mV
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±100V	V_{IN} = 0		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±100V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±100V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±100V	V_{IN} = 0, A_V = 100		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±100V	V_{IN} = 0, A_V = 100		4.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		6.1	mV
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		5.4	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±100V	V_{IN} = 0		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±100V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±100V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±100V	V_{IN} = 0, A_V = 100		11	mA
2	Input Offset Voltage	V_{OS}	125°C	±100V	V_{IN} = 0, A_V = 100		5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		6.7	mV
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		6	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±100V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±100V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±100V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 150mA	V_O	25°C	±31V	R_L = 100Ω	15		V
4	Output Voltage, I_O = 29mA	V_O	25°C	±150V	R_L = 5K	145		V
4	Output Voltage, I_O = 80mA	V_O	25°C	± 90V	R_L = 1K	80		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±100V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±100V	R_L = 5K	20	100	V/µs
4	Open Loop Gain	A_{OL}	25°C	±100V	R_L = 5K, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 100mA	V_O	–55°C	±31V	R_L =100Ω	10		V
6	Output Voltage, I_O = 29mA	V_O	–55°C	±150V	R_L = 5K	145		V
6	Output Voltage, I_O = 70mA	V_O	–55°C	±90V	R_L = 1K	70		V
6	Stability/Noise	E_N	–55°C	±100V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±100V	R_L = 5K	20	100	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±100V	R_L = 5K, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 150mA	V_O	125°C	±31V	R_L = 100Ω	15		V
5	Output Voltage, I_O = 29mA	V_O	125°C	±150V	R_L = 5K	145		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±90V	R_L = 1K	80		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K	20	100	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA09 • PA09A

FEATURES

- **POWER MOS TECHNOLOGY — 2A peak rating**
- **HIGH GAIN BANDWIDTH PRODUCT — 150MHz**
- **VERY FAST SLEW RATE — 400V/μs**
- **PROTECTED OUTPUT STAGE — Thermal shutoff**
- **EXCELLENT LINEARITY — Class A/B output**
- **WIDE SUPPLY RANGE — ±12V to ±40V**
- **LOW BIAS CURRENT, LOW NOISE — FET input**

APPLICATIONS

- **VIDEO DISTRIBUTION AND AND AMPLIFICATION**
- **HIGH SPEED DEFLECTION CIRCUITS**
- **POWER TRANSDUCERS TO 5MHz**
- **COAXIAL LINE DRIVERS**
- **POWER LED OR LASER DIODE EXCITATION**

DESCRIPTION

The PA09 is a high voltage, high output current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA09 exhibits superior DC and AC stability over a wide supply and temperature range.

High speed and freedom from second breakdown is assured by a complementary Power MOS output stage. For optimum linearity, especially at low levels, the Power MOS transistors are biased in the class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit protects the amplifier against overloading. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

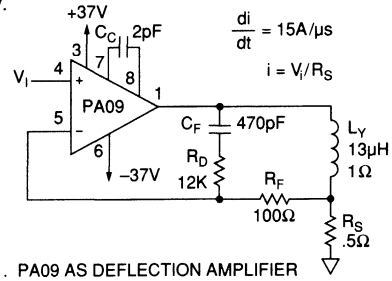
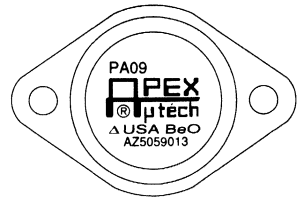


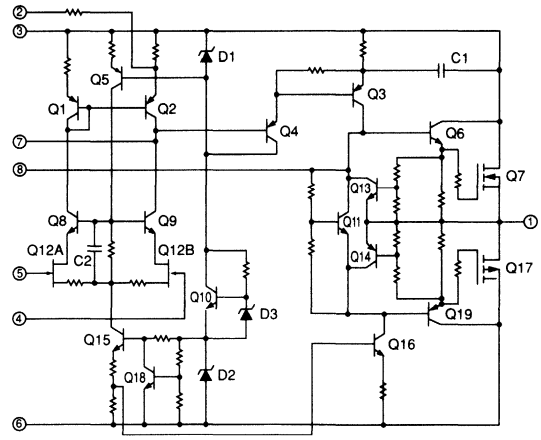
FIGURE 1. PA09 AS DEFLECTION AMPLIFIER



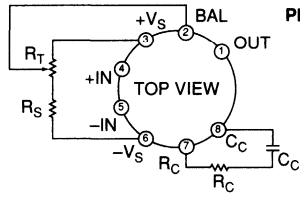
DEFLECTION AMPLIFIER (Figure 1)

The deflection amplifier circuit of Figure 1 achieves arbitrary beam positioning for a fast heads-up display. Maximum transition times are 4μs while delivering 2A pk currents to the 13mH coil. The key to this circuit is the sense resistor (R_S) which converts yoke current to voltage for op amp feedback. This negative feedback forces the coil current to stay exactly proportional to the control voltage. The network consisting of R_D, R_F and C_F serves to shift from a current feedback via R_S to a direct voltage feedback at high frequencies. This removes the extra phase shift caused by the inductor thus preventing oscillation. See Application Note 5 for details of this and other precision magnetic deflection circuits.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	100pF	200Ω
10	15pF	0Ω
100	5pF	0Ω
1000	none	none

$R_S = (|+V_S| + |-V_S|)\ R_T/1.6$

NOTE: Input offset voltage trim optional. R_T = 10KΩ MAX

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal[1]	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

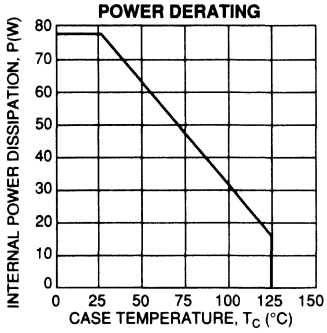
		PA09			PA09A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		.5	± 3		± .25	± .5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25 to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25 to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		5	100		3	20	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		1.5	10	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = –25 to +85°C	$\pm V_S$–10	$\pm V_S$–8		*	*		V
COMMON MODE REJECTION, DC	T_C = –25 to +85°C, V_{CM} = ± 20V		104			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1kΩ		90			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	80	88		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, R_L = 15Ω, C_C = 5pF		150			*		MHz
POWER BANDWIDTH, gain of 100 comp	T_C = 25°C, R_L = 15Ω, C_C = 5pF		1.2			*		MHz
POWER BANDWIDTH, unity gain comp	T_C = 25°C, R_L = 15Ω, C_C = 100pF		.75			*		MHz
OUTPUT								
VOLTAGE SWING[3]	T_C = –25 to +85°C, I_O = 2A	$\pm V_S$ –8	$\pm V_S$ –7		*	*		V
CURRENT, PEAK	T_C = 25°C		4.5			*		A
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, gain of 100 comp	T_C = 25°C, C_C = 5pF		400			*		V/µs
SLEW RATE, unity gain comp	T_C = 25°C, C_C = 100pF		75			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = –25 to +85°C	± 12	± 35	± 40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		70	85		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[4]	T_C = –25 to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	T_C = –25 to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = –25 to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	+ 85	*	*	*	°C

NOTES: * The specification of PA09A is identical to the specification for PA09 in applicable column to the left.

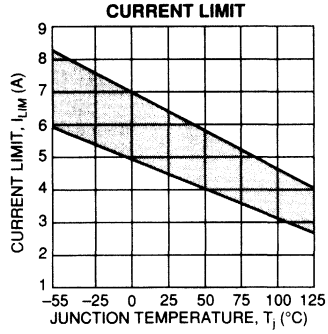
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±35V unless otherwise specified as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

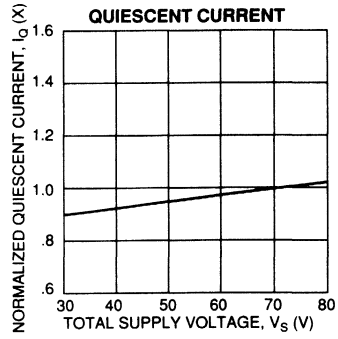
POWER DERATING



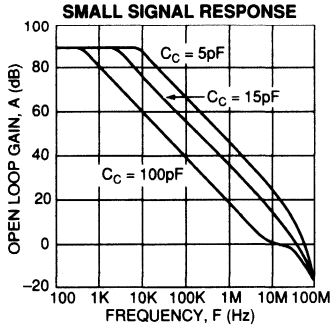
CURRENT LIMIT



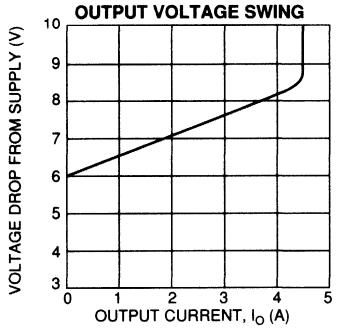
QUIESCENT CURRENT



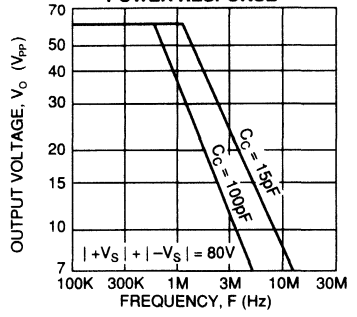
SMALL SIGNAL RESPONSE



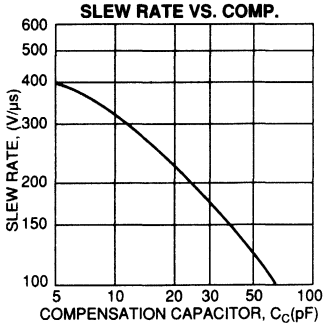
OUTPUT VOLTAGE SWING



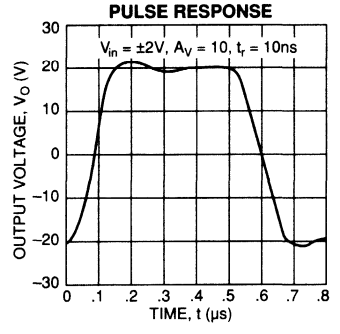
POWER RESPONSE



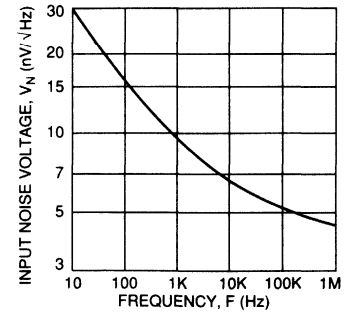
SLEW RATE VS. COMP.



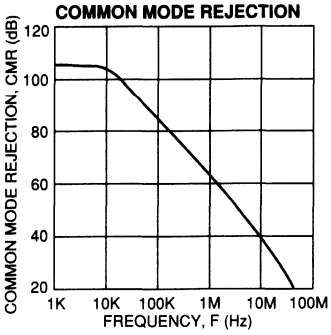
PULSE RESPONSE



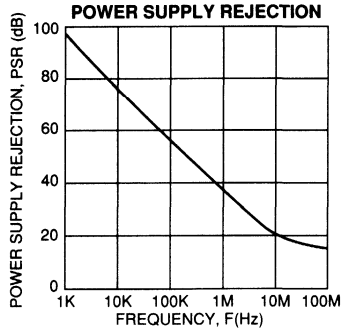
INPUT NOISE



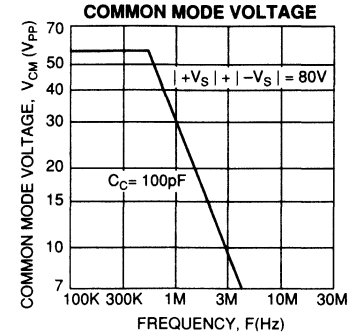
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SUPPLY VOLTAGE

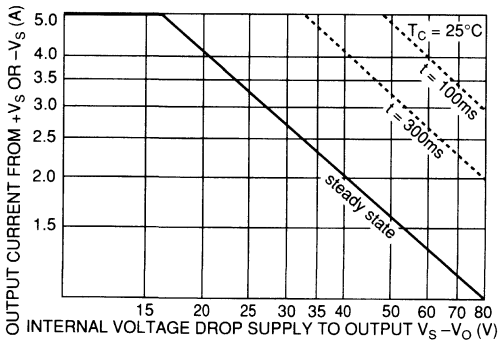
The specified voltage ($\pm V_S$) applies for a dual (±) supply having equal voltages. A nonsymmetrical (ie. +70/–10V) or a single supply (ie. 80V) may be used as long as the total voltage between the $+V_S$ and $-V_S$ rails does not exceed the sum of the voltages of the specified dual supply.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

SAFE OPERATING AREA CURVES



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

1. Capacitive and inductive loads up to the following maximums are safe:

$\pm V_S$	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1µF	11mH
30V	500µF	24mH
20V	2500µF	75mH
15V	∞	100mH

2. Short circuits to ground are safe with dual supplies up to ±20V.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

BYPASSING OF SUPPLIES

Each supply rail must be bypassed to common with a tantalum capacitor of at least 47µF in parallel with a .47µF ceramic capacitor directly connected from the power supply pins to the ground plane.

OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductance, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

GROUNDING

Single point grounding of the input resistors and the input signal to a common ground plane will prevent undesired current feedback, which can cause large errors and/or instabilities.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier, If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth the PA09 is more likely to oscillate than lower bandwidth Power Operational Amplifiers. To prevent oscillations a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections on the first page of this data sheet and interpolate if necessary. The phase margin can be increased by using a larger capacitor and a smaller resistor than the slew rate optimized values listed in the table.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or bypassing of the feedback resistor.
3. Connect the case to a local AC ground potential.

CURRENT LIMIT

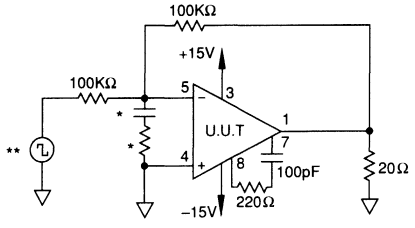
Internal current limiting is provided in the PA09. Note the current limit curve given under typical performance graphs is based on junction temperature. If the amplifier is operated at cold junction temperatures, current limit could be as high as 8 amps. This is above the maximum allowed current on the SOA curve of 5 amps. Systems using this part must be designed to keep the maximum output current to less than 5 amps under all conditions. The internal current limit only provides this protection for junction temperatures of 80°C and above.

TABLE 4 GROUP A INSPECTION

PA09M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±35V	V_{IN} = 0, A_V = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±35V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±12V	V_{IN} = 0, A_V = 100		5.3	mV
1	Input Offset Voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		3.5	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Inout Bias Current, –IN	$-I_B$	25°C	±35V	V_{IN} = 0		100	pA
1	Input Offset Current	I_{OS}	25°C	±35V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±35V	V_{IN} = 0, A_V = 100		165	mA
3	Input Offset Voltage	V_{OS}	–55°C	±35V	V_{IN} = 0, A_V = 100		5.4	mV
3	Input Offset Voltage	V_{OS}	–55°C	±12V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Offset Voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		5.9	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±35V	V_{IN} = 0		100	pA
3	Input Offset Current	I_{OS}	–55°C	±35V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±35V	V_{IN} = 0, A_V = 100		140	mA
2	Input Offset Voltage	V_{OS}	125°C	±35V	V_{IN} = 0, A_V = 100		6	mV
2	Input Offset Voltage	V_{OS}	125°C	±12V	V_{IN} = 0, A_V = 100		8.3	mV
2	Input Offset Voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		6.5	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±35V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±35V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 3A	V_O	25°C	±21.3V	R_L = 3.75Ω	11.3		V
4	Output Voltage, I_O = 66mA	V_O	25°C	±40V	R_L = 500Ω	33		V
4	Output Voltage, I_O = 2A	V_O	25°C	± 38V	R_L = 15Ω	30		V
4	Current Limits	I_{CL}	25°C	±32.2V	R_L = 3.75Ω	3.4	6	A
4	Stability/Noise	E_N	25°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew Rate	SR	25°C	±35V	R_L = 500Ω, A_V =1	25	500	V/µs
4	Open Loop Gain	A_{OL}	25°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
4	Common Mode Rejection	CMR	25°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
6	Output Voltage, I_O = 3A	V_O	–55°C	±21.3V	R_L = 3.75Ω	11.3		V
6	Output Voltage, I_O = 66mA	V_O	–55°C	±40V	R_L = 500Ω	33		V
6	Output Voltage, I_O = 2A	V_O	–55°C	±38V	R_L = 15Ω	30		V
6	Stability/Noise	E_N	–55°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew Rate	SR	–55°C	±35V	R_L = 500Ω, A_V =1	25	500	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
6	Common Mode Rejection	CMR	–55°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V	64		dB
5	Output Voltage, I_O = 1A	V_O	125°C	±14V	R_L = 3.75Ω	3.75		V
5	Output Voltage, I_O = 66mA	V_O	125°C	±40V	R_L = 500Ω	33		V
5	Output Voltage, I_O = 1A	V_O	125°C	±23.5V	R_L = 15Ω	15		V
5	Stability/Noise	E_N	125°C	±35V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew Rate	SR	125°C	±35V	R_L = 500Ω, A_V = 1	20	500	V/µs
5	Open Loop Gain	A_{OL}	125°C	±35V	R_L = 500Ω, F = 10Hz	80		dB
5	Common Mode Rejection	CMR	125°C	±34.5V	R_L = 500Ω, F = DC, V_{CM} = ±22.5V+	64		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA10 • PA10A

FEATURES

- GAIN BANDWIDTH PRODUCT — 4MHz
- TEMPERATURE RANGE — -55 to +125°C (PA10A)
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — ±5A Peak

APPLICATIONS

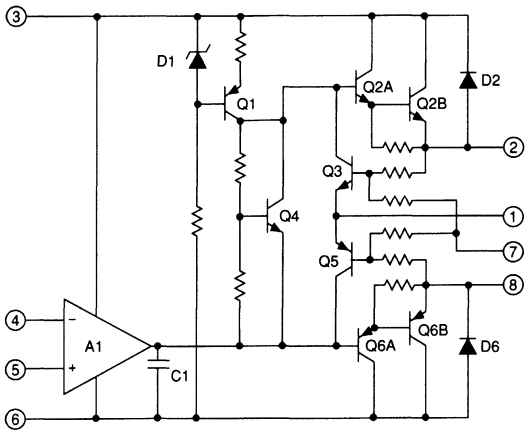
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 4A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 180W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 60W RMS

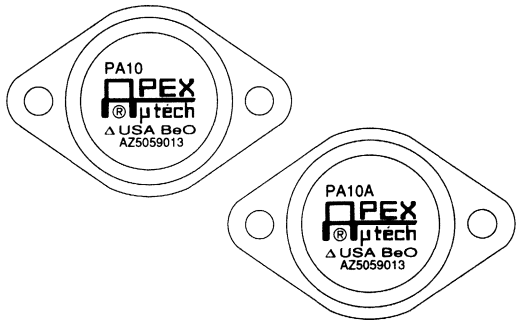
DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary darlington emitter follower output stages are protected against transient inductive kickback. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

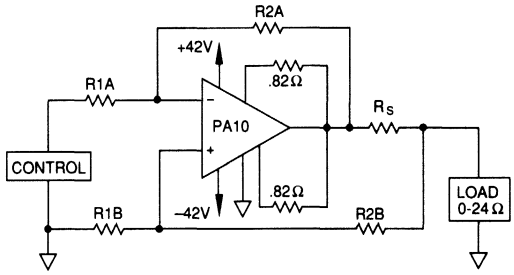
This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





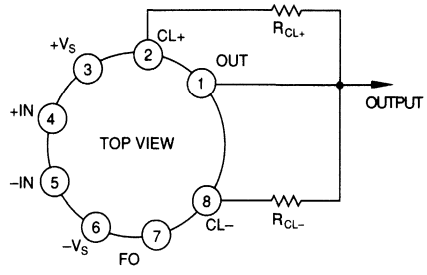
TYPICAL APPLICATION



DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	67W
INPUT VOLTAGE, differential	$\pm V_S$ –3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +100°C

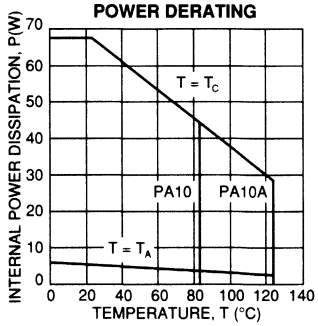
SPECIFICATIONS

		PA10			PA10A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±.1	±.3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µVW
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±400		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 15Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 15Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 15Ω load	10	15		*	*		kHz
PHASE MARGIN	Full temp. range, 15Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–8	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 2A	$\pm V_S$–6			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	5			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2	5		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1			.68			*	nF
CAPACITIVE LOAD	Full temperature range, A_V = 2.5			10			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C	8	15	30	*	*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		1.9	2.1		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		2.4	2.6		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

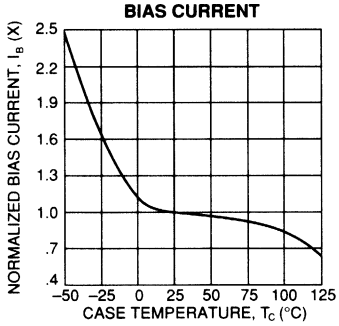
NOTES: * The specification of PA10A is identical to the specification for PA10 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

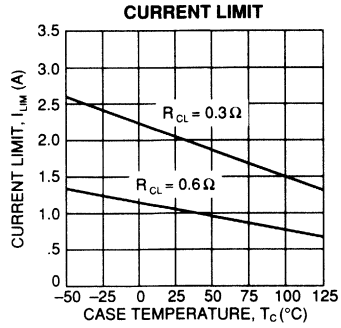
POWER DERATING



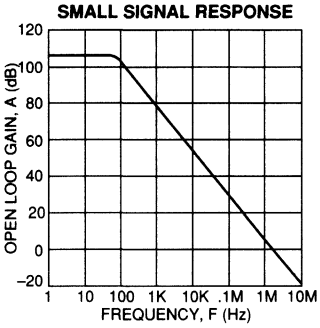
BIAS CURRENT



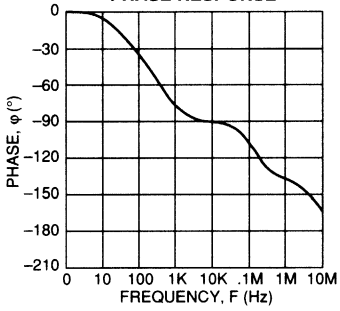
CURRENT LIMIT



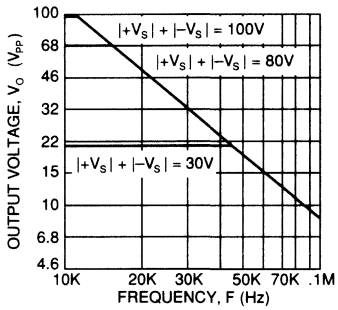
SMALL SIGNAL RESPONSE



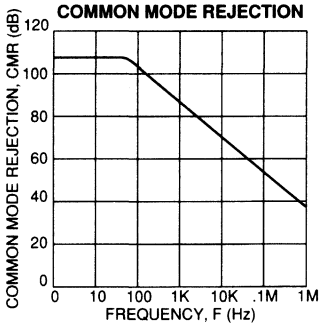
PHASE RESPONSE



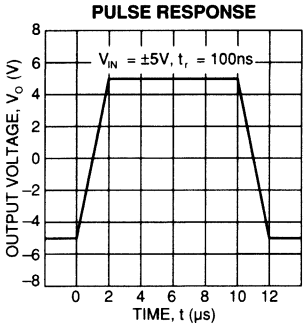
POWER RESPONSE



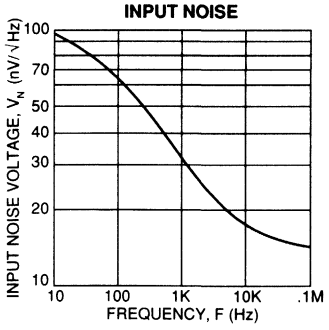
COMMON MODE REJECTION



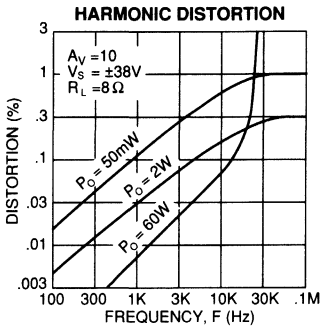
PULSE RESPONSE



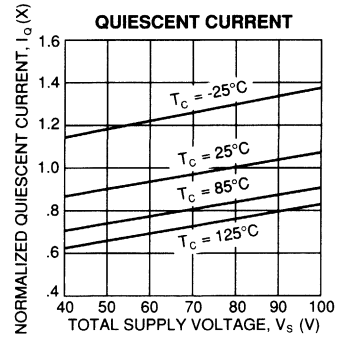
INPUT NOISE



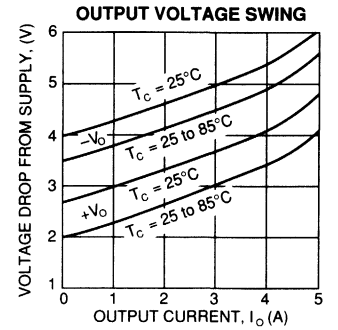
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



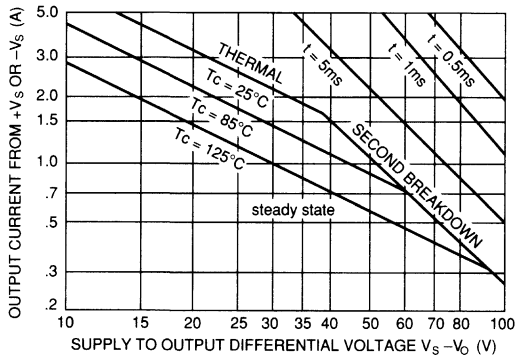
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 2A	I_{LIM} = 5A	I_{LIM} = 2A	I_{LIM} = 5A
50V	80µF	75µF	55mH	7.5mH
40V	250µF	150µF	150mH	11mH
35V	500µF	250µF	200mH	15mH
30V	1,200µF	500µF	250mH	24mH
25V	4,000µF	1,600µF	400mH	38mH
20V	20,000µF	5,000µF	1,500mH	75mH
15V	**	25,000µF	**	100mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 5A or 20V below the supply rail with I_{LIM} = 2A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

**Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.26A	.84A
40V	.38A	1.1A
35V	.49A	1.2A
30V	.65A	1.4A
25V	.84A	1.7A
20V	1.1A	2.2A
15V	1.4A	2.9A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMITING

To use standard current limiting, leave pin 7 open and proceed per "General Operating Considerations" section of the handbook, where initial setting and variation with temperature are described. Foldover action is described in detail in Application Note 9.

For certain applications, foldover protection allows for increased output current as the output of the Power Op Amp swings close to the supply rail. This function can be achieved by connecting pin 7 directly or through a resistor to ground, and controlled by the following equation:

$$I_{LIM} = \frac{.65 + \frac{.28V_O}{20 + R_{FO}}}{R_{CL} = .01} \quad (1)$$

Where:
I_{LIM} is the current limit, in Amps, at a given output voltage V_O.
R_{FO} is the current foldover resistor pin 7 to ground in KΩ.
R_{CL} is the current limit resistor in Ω.
V_O is the instantaneous output voltage in V.*

*The basic equation assumes V_O and the current carrying supply are of the same polarity. If these polarities differ, assign V_O a negative value.
**.01Ω = wire bond and pin resistance to R_{CL} connections.

PROCEDURE

1. Select R_{CL} to provide a safe current limit at V_O = 0:

$$R_{CL}\ (\Omega) = (.65/I_{LIM}) - .01 \quad (2)$$

2. Find the current limit for the maximum output voltage swing and pin 7 connected to ground/common:

$$I_{LIM} = \frac{.65 + \frac{.28V_O}{20}}{R_{CL} + .01} \quad (3)$$

This is the highest current limit possible at maximum output. It may be decreased without affecting the short circuit current limit by putting a resistor in series with pin 7 to ground.

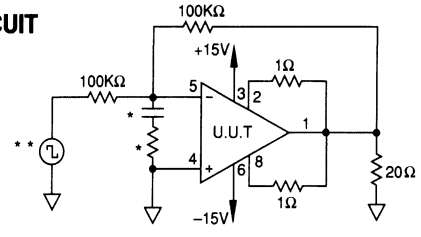
The following equation can be used to calculate R_{FD} (KΩ) using a lower current limit:

$$R_{FD} = \frac{.28V_O}{I_{LIM}\ (R_{CL} + .01) - .65} - 20 \quad (4)$$

3. To calculate the current limit at any output voltage (V_O), use equation "one". If V_O is of opposite polarity to the current carrying supply, assign V_O a negative value and check the calculated current against the SOA graph.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input bias current, –IN	$-I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		75	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input bias current, –IN	$-I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent current	I_Q	125°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		30	mA
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input bias current, –IN	$-I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output voltage, I_O = 5A	V_O	25°C	±18V	R_L = 2.07Ω	10		V
4	Output voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output voltage, I_O = 2A	V_O	25°C	±30V	R_L = 12Ω	24		V
4	Current limits	I_{CL}	25°C	±16.5V	R_L = 2.07Ω, R_{CL} = .2Ω	2.6	3.9	A
4	Stability/noise	E_N	25°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
4	Slew rate	SR	25°C	±40V	R_L = 500Ω	2	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output voltage, I_O = 5A	V_O	–55°C	±18V	R_L = 2.07Ω	10		V
6	Output voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Output voltage, I_O = 2A	V_O	–55°C	±30V	R_L = 12Ω	24		V
6	Stability/noise	E_N	–55°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
6	Slew rate	SR	–55°C	±40V	R_L = 500Ω	2	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	R_L = 500Ω, F = 10Hz	96		db
6	Common mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output voltage, I_O = 3A	V_O	125°C	±14.3V	R_L = 2.07Ω	6.3		V
5	Output voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output voltage, I_O = 2A	V_O	125°C	±30V	R_L = 12Ω	24		V
5	Stability/noise	E_N	125°C	±40V	R_L = 500Ω, A_V = 1, C_L = .68nF		1	mV
5	Slew rate	SR	125°C	±40V	R_L = 500Ω	2	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA12 • PA12A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- LOW THERMAL RESISTANCE — 1.4°C/W
- CURRENT FOLDOVER PROTECTION — NEW
- HIGH TEMPERATURE VERSION — PA12H
- EXCELLENT LINEARITY — Class A/B Output
- WIDE SUPPLY RANGE — ±10V to ±50V
- HIGH OUTPUT CURRENT — Up to ±15A Peak

APPLICATIONS

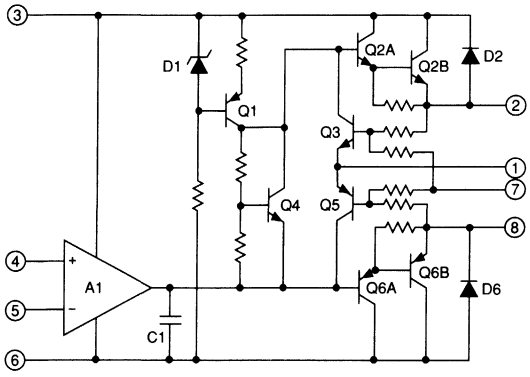
- MOTOR, VALVE AND ACTUATOR CONTROL
- MAGNETIC DEFLECTION CIRCUITS UP TO 10A
- POWER TRANSDUCERS UP TO 100kHz
- TEMPERATURE CONTROL UP TO 360W
- PROGRAMMABLE POWER SUPPLIES UP TO 90V
- AUDIO AMPLIFIERS UP TO 120W RMS

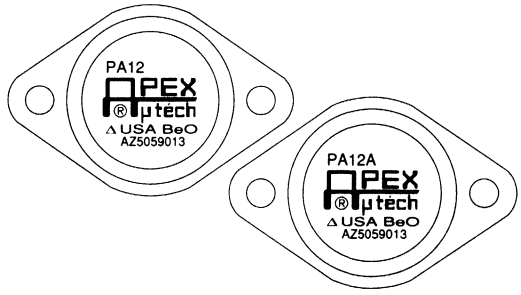
DESCRIPTION

The PA12 is a state of the art high voltage, very high output current operational amplifier designed to drive resistive, inductive and capacitive loads. The complementary darlington emitter follower output stage is protected against transient inductive kickback. For optimum linearity, especially at low levels, the output stage is biased for class A/B operation using a thermistor compensated base-emitter voltage multiplier circuit. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





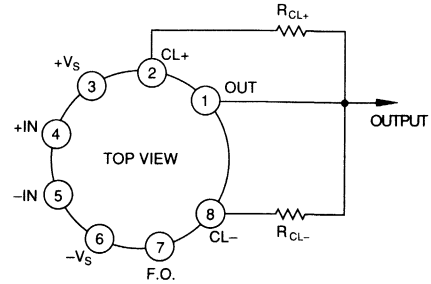
POWER RATING

Not all vendors use the same method to rate the power handling capability of a Power Op Amp. APEX rates the internal dissipation, which is consistent with rating methods used by transistor manufacturers and gives conservative results. Rating delivered power is highly application dependent and therefore can be misleading. For example, the 125W internal dissipation rating of the PA12 could be expressed as an output rating of 250W for audio (sine wave) or as 440W if using a single ended DC load. Please note that all vendors rate maximum power using an infinite heatsink.

THERMAL STABILITY

APEX has eliminated the tendency of class A/B output stages toward thermal runaway and thus has vastly increased amplifier reliability. This feature, not found in most other Power Op Amps, was pioneered by APEX in 1981 using thermistors which assure a negative temperature coefficient in the quiescent current. The reliability benefits of this added circuitry far outweigh the slight increase in component count.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

	PA12/PA12A
SUPPLY VOLTAGE, +Vs to –Vs	100V
OUTPUT CURRENT, within SOA	15A
POWER DISSIPATION, internal	125W
INPUT VOLTAGE, differential	$\pm V_S$ –3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

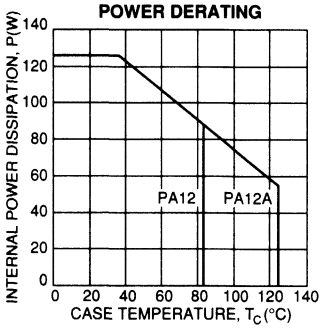
SPECIFICATIONS

		PA12			PA12A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		12	±30		10	20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±50	±400		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC	Full temp. range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, 1KΩ1 load		110			*		dB
OPEN LOOP GAIN at 10Hz	Full temp. range, 8Ω load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, 8Ω load		4			*		MHz
POWER BANDWIDTH	T_C = 25°C, 8Ω load	13	20		*	*		kHz
PHASE MARGIN	Full temp. range, 8Ω load		20			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, PA12 = 10A, PA12A = 15A	$\pm V_S$–6			*			V
VOLTAGE SWING[3]	T_C = 25°C, I_O = 5A	$\pm V_S$–5			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = 80mA	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	10			15			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C	2.5	4		*	*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1			1.5			*	nF
CAPACITIVE LOAD	Full temperature range, A_V > 10			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±40	±45	*	*	±50	V
CURRENT, quiescent	T_C = 25°C		25	50		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = –55 to +125°C, F > 60Hz		.8	.9		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = –55 to +125°C		1.25	1.4		*	*	°C/W
RESISTANCE, junction to air	T_C = –55 to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25		+85	–55		+125	°C

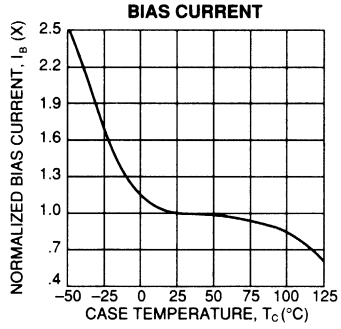
NOTES: * The specification of PA12A is identical to the specification for PA12 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is ±40, unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

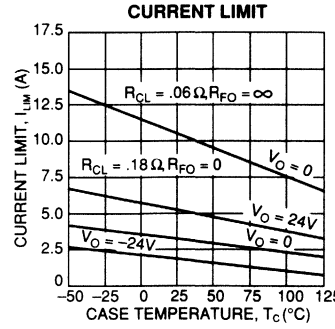
POWER DERATING



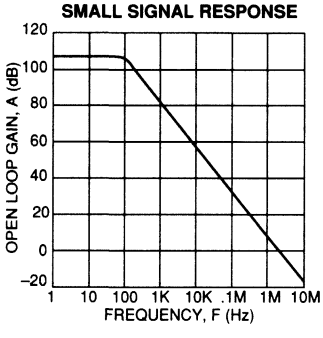
BIAS CURRENT



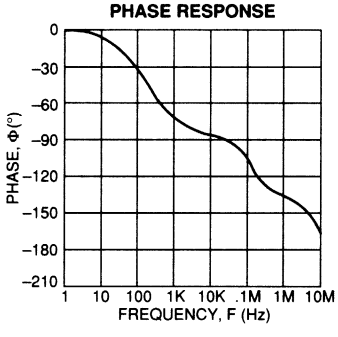
CURRENT LIMIT



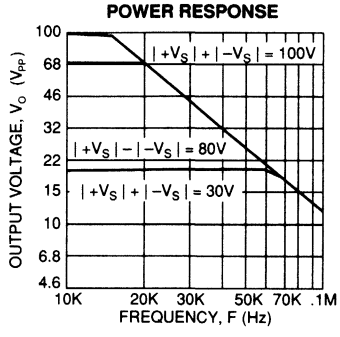
SMALL SIGNAL RESPONSE



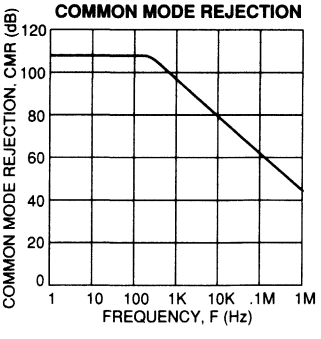
PHASE RESPONSE



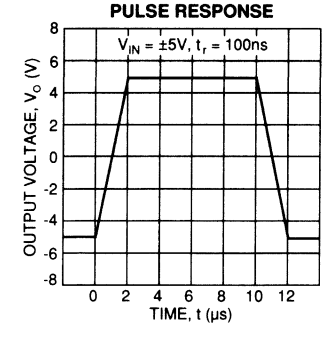
POWER RESPONSE



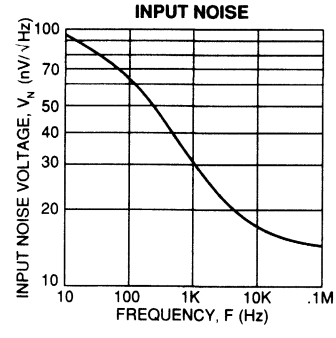
COMMON MODE REJECTION



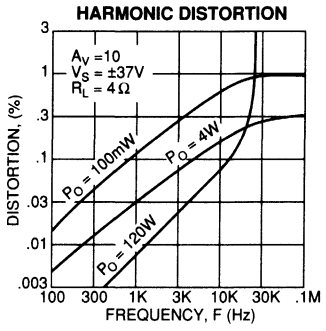
PULSE RESPONSE



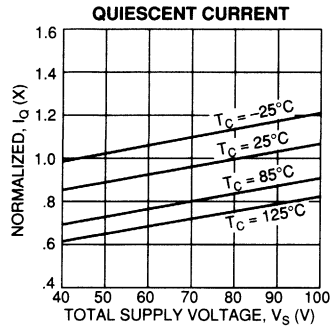
INPUT NOISE



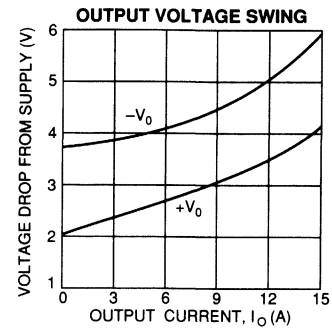
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



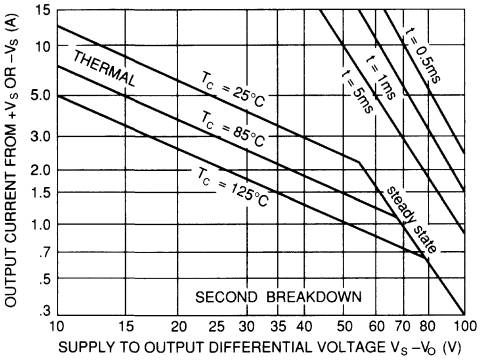
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts.

1. Capacitive and dynamic* inductive loads up to the following maximum are safe with the current limits set as specified.

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
50V	200µF	125µF	5mH	2.0mH
40V	500µF	350µF	15mH	3.0mH
35V	2.0mF	850µF	50mH	5.0mH
30V	7.0mF	2.5mF	150mH	10mH
25V	25mF	10mF	500mH	20mH
20V	60mF	20mF	1,000mH	30mH
15V	150mF	60mF	2,500mH	50mH

*If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 15A or 25V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor must be capacitively coupled or the current limit must be lowered to meet SOA criteria.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or common if the current limits are set as follows at T_C = 25°C:

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
50V	.30A	2.4A
40V	.58A	2.9A
35V	.87A	3.7A
30V	1.5A	4.1A
25V	2.4A	4.9A
20V	2.9A	6.3A
15V	4.2A	8.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMITING

To use standard current limiting, leave pin 7 open and proceed per "General Operating Considerations" section of the handbook, where initial setting and variation with temperature are described. Foldover action is described in detail in Application Note 9.

For certain applications, foldover protection allows for increased output current as the output of the Power Op Amp swings close to the supply rail. This function can be activated by connecting pin 7 directly or through a resistor to ground, and controlled by the following equation:

$$I_{LIM} = \frac{.65 + \frac{.28Vo}{20 + R_{FO}}}{R_{CL} = .01^{**}} \quad (1)$$

Where:
I_{LIM} is the current limit, in Amps, at a given output voltage V_O.
R_{FO} is the current foldover resistor pin 7 to ground in KΩ.
R_{CL} is the current limit resistor in Ω.
V_O is the instantaneous output voltage in V.*

*The basic equation assumes V_O and the current carrying supply are of the same polarity. If these polarities differ, assign V_O a negative value.
**.01Ω = wire bond and pin resistance to R_{CL} connections.

PROCEDURE

1. Select R_{CL} to provide a safe current limit at V_O = 0:

$$R_{CL}\ (\Omega) = (.65/I_{LIM}) - .01 \quad (2)$$

2. Find the current limit for the maximum output voltage swing and pin 7 connected to ground/common:

$$I_{LIM} = \frac{.65 + \frac{.28V_O}{20}}{R_{CL} + .01} \quad (3)$$

This is the highest current limit possible at maximum output. It may be decreased without affecting the short circuit current limit by putting a resistor in series with pin 7 to ground.

The following equation can be used to calculate R_{FD} (KΩ) using a lower current limit:

$$R_{FD} = \frac{.28V_O}{I_{LIM}\ (R_{CL} + .01) - .65} - 20 \quad (4)$$

3. To calculate the current limit at any output voltage (V_O), use equation "one". If V_O is of opposite polarity to the current carrying supply, assign V_O a negative value and check the calculated current against the SOA graph.

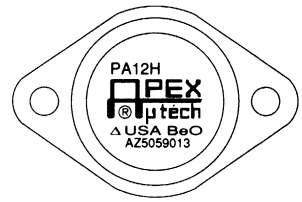
POWER OPERATIONAL AMPLIFIER

PA12H

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421 1865

FEATURES

- **LOW COST 200°C VERSION OF PA12**
- **OUTPUT CURRENT at 200°C — ±1A**
- **FULL SPECIFICATIONS — -25°C to +125°C**
- **WIDE SUPPLY RANGE — ±10 to ±45V**
- **CURRENT FOLDOVER PROTECTION**
- **EXCELLENT LINEARITY — Class A/B Output**



APPLICATIONS

- **MOTOR, VALVE AND ACTUATOR CONTROL**
- **POWER TRANSDUCERS UP TO 100kHz**
- **PROGRAMMABLE POWER SUPPLIES UP TO 80V**
- **TRANSMISSION LINE DRIVER**

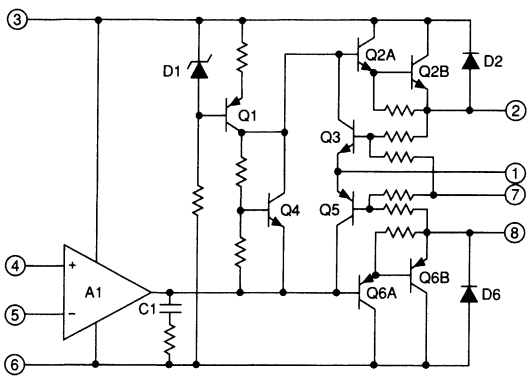
DESCRIPTION

The PA12H is a low cost, high temperature Power Op Amp made especially for short term use in extreme environmental situations such as down hole instrumentation. The amplifier can power mechanical or electronic transducers and can drive the long transmission lines associated with these applications.

The PA12H, based on the standard PA12's very high power level, leaves a six watt capability after being derated for operation at a case temperature of 200°C. To meet the high temperature requirements for up to 200 hours, polyimid has replaced the standard epoxy for attaching the small signal devices. the melting point of the power transistor attach solder is 264°C.

These hybrid integrated circuits utilize thick film conductors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC



SPECIFICATIONS

Specifications of the standard PA12 apply to the PA12H with the exception of the temperature range extensions

1. The operating and storage temperature ranges extend to +200°C.
2. Static and dynamic tests are performed at +125°C as shown in SG 2 and SG 5 of the military PA12M data sheet.
3. Additional tests at T_C = 200°C:
   A. Quiescent current = 100mA max at $\pm V_S$ = 45.
   B. Voltage swing = $\pm V_S$ –4 (I_O = 1A, $\pm V_S$ = 15)

GENERAL CONSIDERATIONS

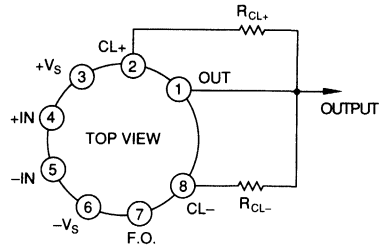
The primary aim of the PA12H is to provide a reasonable level of power output at a minimum cost. To achieve this end, full dynamic tests are performed up to 125°C, with only minimal 100% testing at 200°C. This approach saves nearly an order of magnitude over the cost of a fully tested long life product, but does require recognition of two limitations.

First, input parameters such as voltage offset and bias current are not tested above 125°C. This could lead to accuracy problems if the PA12H is used as a precision computational element. Solutions to this limitation include contacting the factory regarding additional testing at higher temperatures or using high temperature small signal amplifiers for computational tasks.

The second limitation of life span requires the PA12H to be used in short term applications. This requirement is mandated by the low cost design concept. At 200°C component degradation is nearly as severe during storage as during actual operation. This must be taken into account when scheduling actual implementation of the finished package.

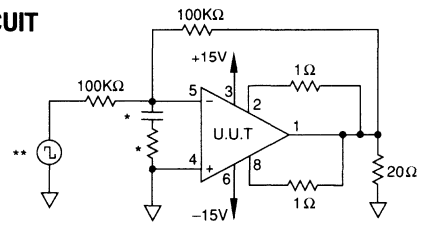
Please consult the PA12 data sheet for basic information on this amplifier; the PA12M data sheet for details on +125°C tests, and Power Operational Amplifier handbook section "General Operating Considerations," for recommendations on supplies, stability, heatsinks and bypassing.

EXTERNAL CONNECTIONS



SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		50	mA
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±6	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±12	mV
1	Input offset voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±7	mV
1	Input bias current, +IN	$+I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Inout bias current,–IN	$-I_B$	25°C	±40V	V_{IN} = 0		±30	nA
1	Input offset current	I_{OS}	25°C	±40V	V_{IN} = 0		±30	nA
3	Quiescent current	I_Q	–55°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		100	mA
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±17.2	mV
3	Input offset voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±12.2	mV
3	Input bias current, +IN	$+I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input bias current,–IN	$-I_B$	–55°C	±40V	V_{IN} = 0		±115	nA
3	Input offset current	I_{OS}	–55°C	±40V	V_{IN} = 0		±115	nA
2	Quiescent current	I_Q	125°C	±40V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		50	mA
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±18.5	mV
2	Input offset voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±13.5	mV
2	Input bias current, +IN	$+I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input bias current, –IN	$-I_B$	125°C	±40V	V_{IN} = 0		±70	nA
2	Input offset current	I_{OS}	125°C	±40V	V_{IN} = 0		±70	nA
4	Output voltage, I_O = 10A	V_O	25°C	±16V	R_L = 1Ω	10		V
4	Output voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output voltage, I_O = 5A	V_O	25°C	±35V	R_L = 6Ω	30		V
4	Current limits	I_{CL}	25°C	±14V	R_L = 1Ω, R_{CL} = .1Ω	5	7.9	A
4	Stability/noise	E_N	25°C	±40V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
4	Slew rate	SR	25°C	±40V	R_L = 500Ω	2.5	10	V/µs
4	Open loop gain	A_{OL}	25°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
4	Common mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output voltage, I_O = 8A	V_O	–55°C	±14V	R_L = 1Ω	8		V
6	Output voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Stability/noise	E_N	–55°C	±40V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
6	Slew rate	SR	–55°C	±40V	R_L = 500Ω	2.5	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
6	Common mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output voltage, I_O = 8A	V_O	125°C	±14V	R_L = 1Ω	8		V
5	Output voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Stability/noise	E_N	125°C	±40V	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1	mV
5	Slew rate	SR	125°C	±40V	R_L = 500Ω	2.5	10	V/µs
5	Open loop gain	A_{OL}	125°C	±40V	R_L = 500Ω, F = 10Hz	96		dB
5	Common mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

PA19 • PA19A

FEATURES

- **VERY FAST SLEW RATE — 900 V/μs**
- **POWER MOS TECHNOLOGY — 4A peak rating**
- **LOW INTERNAL LOSSES — 2V at 2A**
- **PROTECTED OUTPUT STAGE — Thermal Shutoff**
- **WIDE SUPPLY RANGE — ±15V TO ±40V**

APPLICATIONS

- **VIDEO DISTRIBUTION AND AMPLIFICATION**
- **HIGH SPEED DEFLECTION CIRCUITS**
- **POWER TRANSDUCERS UP TO 5 MHz**
- **MODULATION OF RF POWER STAGES**
- **POWER LED OR LASER DIODE EXCITATION**

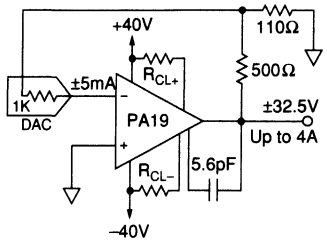
DESCRIPTION

The PA19 is a high voltage, high current operational amplifier optimized to drive a variety of loads from DC through the video frequency range. Excellent input accuracy is achieved with a dual monolithic FET input transistor which is cascoded by two high voltage transistors to provide outstanding common mode characteristics. All internal current and voltage levels are referenced to a zener diode biased on by a current source. As a result, the PA19 exhibits superior DC and AC stability over a wide supply and temperature range.

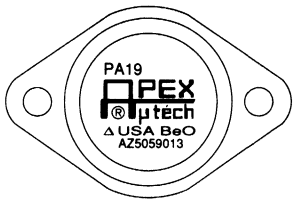
High speed and freedom from second breakdown is assured by a complementary power MOS output stage. For optimum linearity, especially at low levels, the power MOS transistors are biased in a class A/B mode. Thermal shutoff provides full protection against overheating and limits the heatsink requirements to dissipate the internal power losses under normal operating conditions. A built-in current limit of 0.5A can be increased with the addition of two external resistors. Transient inductive load kickback protection is provided by two internal clamping diodes. External phase compensation allows the user maximum flexibility in obtaining the optimum slew rate and gain bandwidth product at all gain settings. A heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film (cement) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers may void the warranty.

TYPICAL APPLICATION



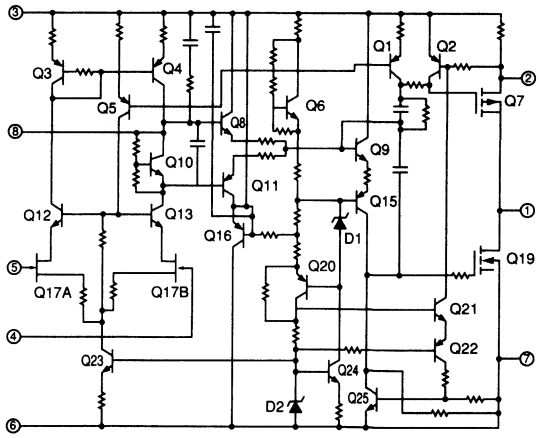
PA19 AS FAST POWER DRIVER



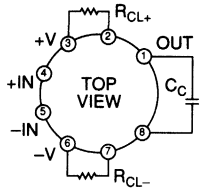
TYPICAL APPLICATION

This fast power driver utilizes the 900V/μs slew rate of the PA19 and provides a unique interface with a current output DAC. By using DAC's internal 1KΩ feedback resistor, temperature drift errors are minimized, since the temperature drift coefficients of the internal current source and the internal feedback resistor of the DAC are closely matched. Gain of V_{OUT} to I_{IN} is –6.5/mA. The DAC's internal 1K resistor together with the external 500Ω and 110Ω form a "tee network" in the feedback path around the PA19. This effective resistance equals 6.5KΩ. Therefore the entire circuit can be modeled as 6.5KΩ feedback resistor from output to inverting input and a 5mA current source into the inverting input of the PA19. Now we see the familiar current to voltage conversion for a DAC where $V_{OUT} = -I_{IN} \times R_{FEEDBACK}$.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C
1	330pF
10	22pF
100	2.2pF
1000	none

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	5A
POWER DISSIPATION, internal	78W
INPUT VOLTAGE, differential	40V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder — 10 sec	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to 155°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

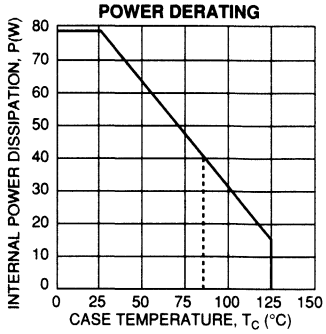
SPECIFICATIONS

		PA19			PA19A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±.5	±3		±25	±.5	mV
OFFSET VOLTAGE, vs. temperature	T_C = 25°C to +85°C		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		10			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C to +85°C		20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		10	200		5	50	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET VOLTAGE, initial	T_C = 25°C		5	100		3	25	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	T_C = 25°C to +85°C	$\pm V_S$–12	$\pm V_S$–10		*	*		V
COMMON MODE REJECTION, DC	T_C = 25°C to +85°C, V_{CM} = ±120V	70	104		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 1KΩ		111			*		dB
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 15Ω	74	78		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, C_C = 2.2pF		100			*		MHz
POWER BANDWIDTH, A_V = 100	T_C = 25°C, C_C = 2.2pF		3.5			*		MHz
PHASE MARGIN, A_V = 1	T_C = 25°C, C_C = 330pF		250			*		kHz
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 4A	$\pm V_S$–5	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 2A	$\pm V_S$–3	$\pm V_S$–2		*	*		V
VOLTAGE SWING[3]	T_C = 25°C to +85°C, I_O = 78mA	$\pm V_S$–1	$\pm V_S$–5		*	*		V
SETTLING TIME to .1%	T_C = 25°C, 2V step		.3			*		µs
SETTLING TIME to .01%	T_C = 25°C, 2V step		1.2			*		µs
SLEW RATE, A_V = 100	T_C = 25°C, C_C = 2.2pF	600	900		800	*		V/µs
SLEW RATE, A_V = 10	T_C = 25°C, C_C = 22pF		650			*		V/µs
POWER SUPPLY								
VOLTAGE	T_C = 25°C to +85°C	±15	±35	±40	*	*	*	V
CURRENT, quiescent	T_C = 25°C		100	120		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	T_C = 25°C to +85°C, F > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC, junction to case	T_C = 25°C to +85°C, F < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	T_C = 25°C to +85°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

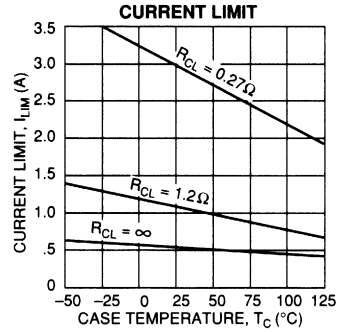
NOTES: * The specification of PA19A is identical to the specification for PA19 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

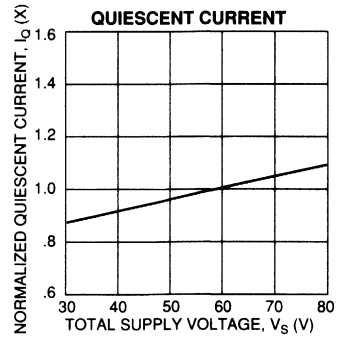
POWER DERATING



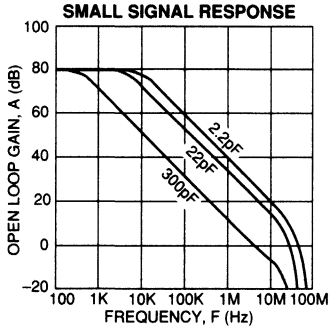
CURRENT LIMIT



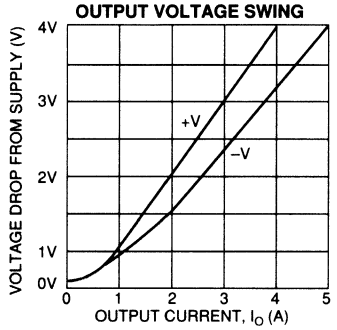
QUIESCENT CURRENT



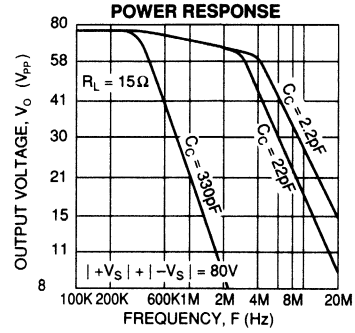
SMALL SIGNAL RESPONSE



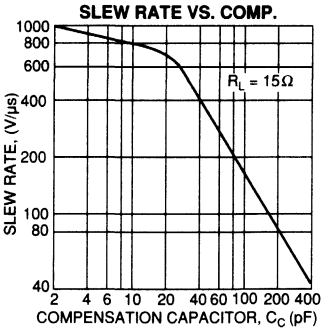
OUTPUT VOLTAGE SWING



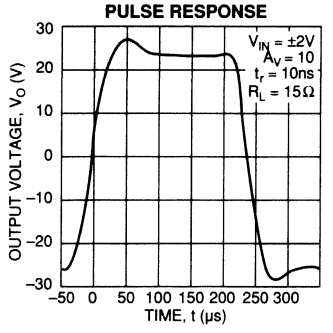
POWER RESPONSE



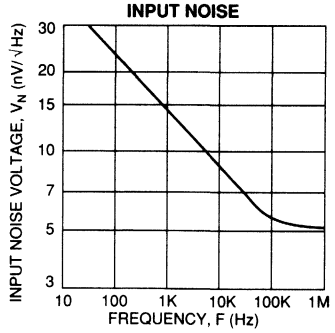
SLEW RATE VS. COMP.



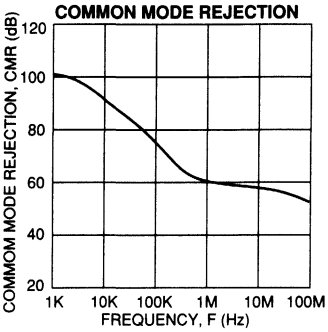
PULSE RESPONSE



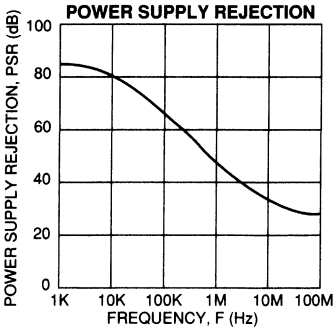
INPUT NOISE



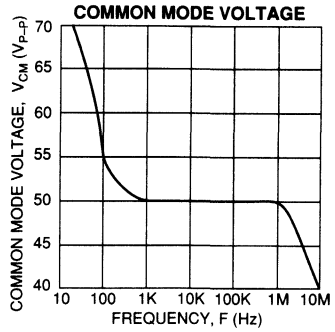
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

Q2 (and Q25) limit output current by turning on and removing gate drive when voltage on pin 2 (pin 7) exceeds .65V differential from the positive (negative) supply rail. With internal resistors equal to 1.2Ω, current limits are approximately 0.5A with no external current limit resistors. With the addition of external resistors current limit will be:

$$I_{LIM} = \frac{.65V}{R_{CL}} + .54A$$

To determine values of external current limit resistors:

$$R_{CL} = \frac{.65V}{I_{CL} - .54A}$$

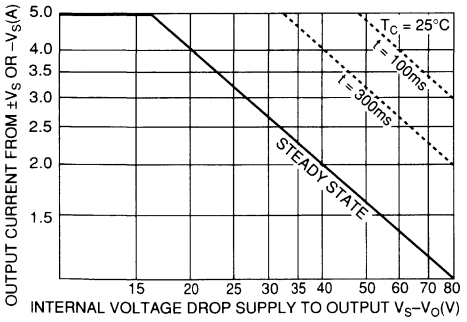
PHASE COMPENSATION

At low gain settings, an external compensation capacitor is required to insure stability. In addition to the resistive feedback network, roll off or integrating capacitors must also be considered when determining gain settings. The capacitance values listed in the external connection diagram, along with good high frequency layout practice, will insure stability. Interpolate values for intermediate gain settings.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.



The SOA curves combine the effect of these limits and allow for internal thermal delays. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts:

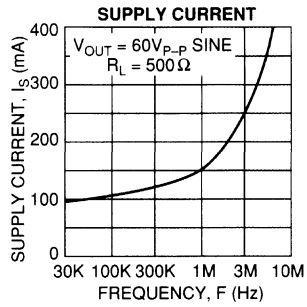
1. Capacitive and inductive loads up to the following maximums are safe:

V_S	CAPACITIVE LOAD	INDUCTIVE LOAD
40V	.1μF	11mH
30V	500μF	24mH
20V	2500μF	75mH
15V	∞	100mH

2. Safe short circuit combinations of voltage and current are limited to a power level of 100W.
3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SUPPLY CURRENT

The PA19 features a class A/B driver stage to charge and discharge gate capacitance of Q7 and Q19. As these currents approach 0.5A, the savings of quiescent current over that of a class A driver stage is considerable. However, supply current drawn by the PA19, even with no load, varies with slew rate of the output signal as shown below.



OUTPUT LEADS

Keep the output leads as short as possible. In the video frequency range, even a few inches of wire have significant inductances, raising the interconnection impedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows the heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_c = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

STABILITY

Due to its large bandwidth, the PA19 is more likely to oscillate than lower bandwidth power operational amplifiers. To prevent oscillations a reasonable phrase margin must be maintained by:

1. Selection of the proper phase compensation capacitor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a larger capacitor at the expense of slew rate. Total physical length (pins of the PA19, capacitor leads plus printed circuit traces) should be limited to a maximum of 3.5 inches.
2. Keep the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistances can be used with increased phase compensation and/or by bypassing the feedback resistor.
3. Connect the case to any AC ground potential.

PA21 • PA21A

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FEATURES

- **LOW COST**
- **WIDE COMMON MODE RANGE — Includes negative supply**
- **WIDE SUPPLY VOLTAGE RANGE**
  - **Single supply: 5V to 40V**
  - **Split supplies: ±2.5V to ±20V**
- **HIGH EFFICIENCY — IVs-2.0VI at 2.5A typ**
- **HIGH OUTPUT CURRENT — 3A min (PA21A)**
- **INTERNAL CURRENT LIMIT**
- **INTERNAL THERMAL SHUTDOWN**
- **LOW DISTORTION**

APPLICATIONS

- **HALF & FULL BRIDGE MOTOR DRIVERS**
- **AUDIO POWER AMPLIFIER**
  - **STEREO — 30W RMS per channel**
  - **BRIDGE — 60W RMS per package**
- **IDEAL FOR SINGLE SUPPLY SYSTEMS**
  - **5V — Peripherals**
  - **12V — Automotive**
  - **28V — Avionic**

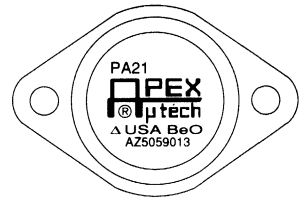
DESCRIPTION

The PA21 consists of monolithic dual power op amp and output compensation network in a 8-pin hermetic TO-3 package. Putting two power op amps in one package and on one die results in an extremely cost effective solution for applications requiring multiple amplifiers per board or bridge mode configurations. The addition of an internal output stage compensation network eliminates the parasitic oscillations usually found in monolithic op amp output stages, and eliminates the need for an external "snubber" network.

The wide common mode input range includes the negative rail, facilitating single supply applications. It is possible to have a "ground based" input driving a single supply amplifier with ground acting as the "second" or "bottom" supply of the amplifier.

The output stage is also well protected in the PA21. It possesses internal current limit circuits as well as internal thermal shutdown circuitry. The thermal shutdown operates with hysteresis, first engaging at approximately Tj = 165°C and not disengaging until Tj < 150°C. While the device is well protected, the Safe Operating Area (SOA) curve must be observed. Proper heatsinking is required for maximum reliability.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor ships to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.



TYPICAL APPLICATION

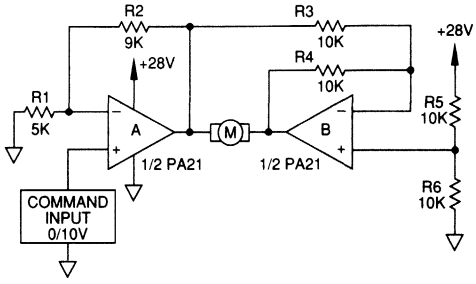
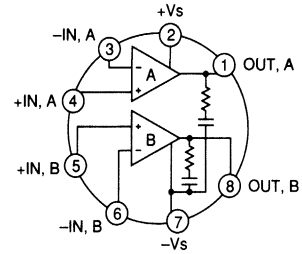


FIGURE 1: BIDIRECTIONAL SPEED CONTROL FROM A SINGLE SUPPLY

R1 and R2 set up amplifier A in a non-inverting gain of 2.8. Amp B is set up as a unity gain inverter driven from the output of amp A. Note that amp B inverts signals about the reference node, which is set at mid-supply (14V) by R5 and R6. When the command input is 5V, the output of amp A is 14V. Since this is equal to the reference node voltage, the output of amp B is also 14V, resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 1). Inputs less positive than 5V drive the motor in the opposite direction.

The PA21 is especially well-suited for this application. The extended common mode range of the PA21 allows command inputs as low as 0V. Its superior output swing abilities let it drive within 2V of supply at an output current of 2A. This means that a command input that ranges from 0V to 10V will drive a 24V motor from full scale CCW to full scale CW at up to ±2A. A single power op amp with an output swing capability of Vs –6 would require ±30V supplies and would be required to swing 48V p-p at twice the speed to deliver an equivalent drive.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, total	5V to 50V
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (per amplifier)	25W
POWER DISSIPATION, internal (both amplifiers)	36W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S$–.5V
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE RANGE, storage	–65°C to 150°C
OPERATING TEMPERATURE RANGE, case	–55°C to 125°C

SPECIFICATIONS

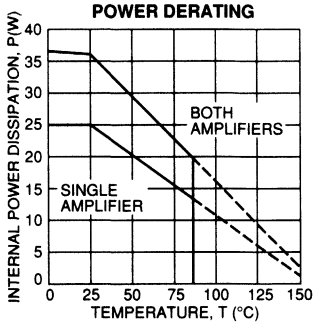
		PA21			PA21A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			1.5	10		.5	4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		15			10		µV/°C
BIAS CURRENT, initial			35	1000		*	250	nA
COMMON MODE RANGE	Full temperature range	$-V_S$–.3		$+V_S$–2	*		*	V
COMMON MODE REJECTION, DC	Full temperature range	60	85		*	*		dB
POWER SUPPLY REJECTION	Full temperature range	60	80		*	*		dB
CHANNEL SEPARATION	I_{OUT} = 1A, F = 1kHz	50	68		*	*		dB
GAIN								
OPEN LOOP GAIN	Full temperature range	80	100		*	*		dB
GAIN BANDWIDTH PRODUCT	A_V = 40dB		600			*		kHz
PHASE MARGIN	Full temperature range		65			*		°
POWER BANDWIDTH	$V_{O(P-P)}$ = 28V		13.6			*		kHz
OUTPUT								
CURRENT, peak		2.5			3			A
CURRENT, limit			3.0			4.0		A
SLEW RATE		.5	1.2		*	*		V/µs
CAPACITIVE LOAD DRIVE	A_V = 1		.22			*		µF
VOLTAGE SWING	Full temp. range, I_O = 100mA	$\|V_S\|$ –1.0	$\|V_S\|$ –0.8		*	*		V
VOLTAGE SWING	Full temp. range, I_O = 1A	$\|V_S\|$ –1.8	$\|V_S\|$ –1.3		*	*		V
VOLTAGE SWING	I_O = 2.5A (PA21), 3A (PA21A)	$\|V_S\|$ –3.0	$\|V_S\|$ –2.0		$\|V_S\|$ –3.5	$\|V_S\|$ –3		V
POWER SUPPLY								
VOLTAGE, V_{SS}[3]		5[4]	30	40	*	*	*	V
CURRENT, quiescent, total			45	90		*	*	mA
THERMAL								
RESISTANCE, junction to case								
DC, single amplifier			5.0			*		°C/W
DC, both amplifiers[5]			3.4			*		°C/W
AC, single amplifier			3.7					°C/W
AC, both amplifiers[5]			2.4					°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	–25		85	°C

NOTES: * The specification of PA21A is identical to the specification for PA21 in applicable column to the left.

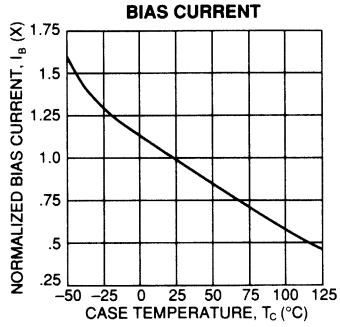
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $\pm V_S = \pm 15V$, $T_C = 25°C$.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Thermal shutdown and current limit may not function properly below V_{SS} = 6V, however SOA violations are unlikely in this area.
5. Rating applies when power dissipation is equal in the two amplifiers.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

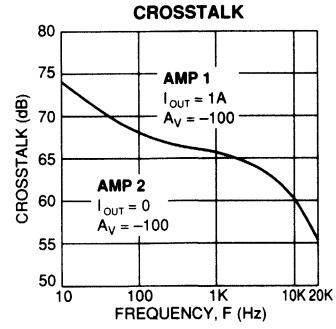
POWER DERATING



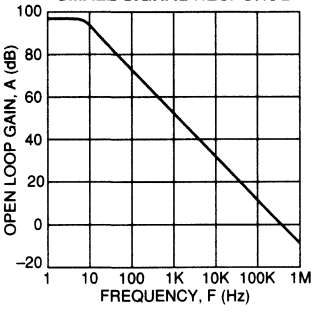
BIAS CURRENT



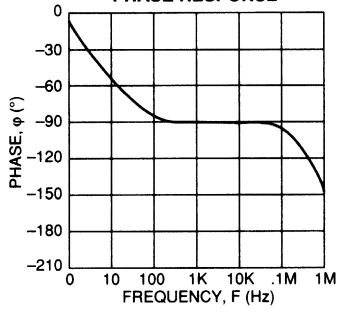
CROSSTALK



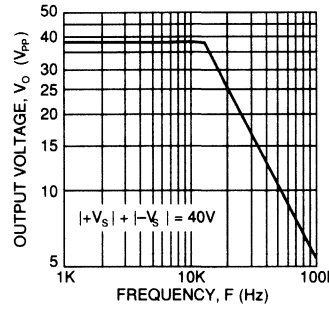
SMALL SIGNAL RESPONSE



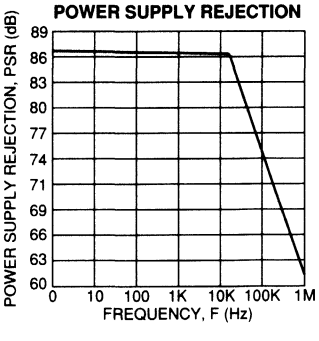
PHASE RESPONSE



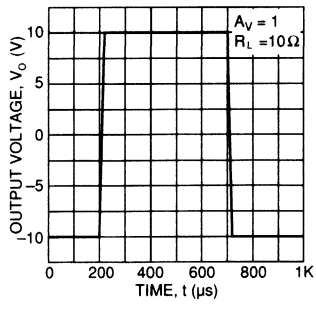
POWER RESPONSE



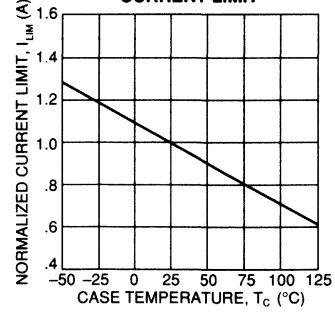
POWER SUPPLY REJECTION



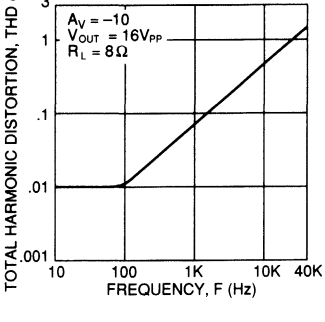
PULSE RESPONSE



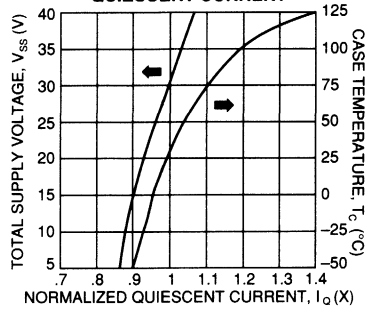
CURRENT LIMIT



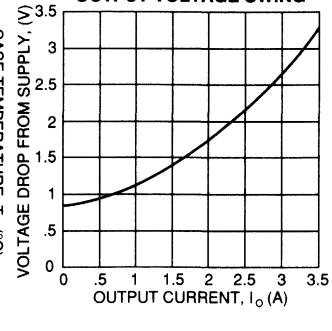
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING



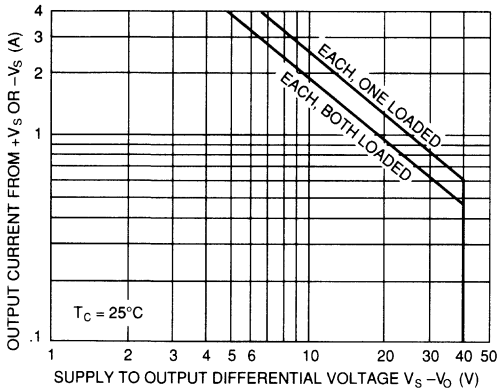
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

Current limit is internal to the PA21, the typical value is shown in the current limit specification.

SAFE OPERATING AREA (SOA)



The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

±Vs	CAPACITIVE LOAD	INDUCTIVE LOAD
20V	200µF	7.5mH
15V	500µF	25mH
10V	5mF	35mH
5V	50mF	150mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 6V below the supply rail while the amplifier is current limiting, the inductor should be capacitively coupled or the supply voltage must be lowered to meet SOA criteria.

NOTE: For protection against sustained, high energy flyback, external fast-recovery diodes should be used.

STABILITY

The PA21 is internally compensated for unity gain stability, no additional compensation is required.

THERMAL SHUTDOWN PROTECTION

The PA21 has a sophisticated circuit that shuts off internal current supplies when the die temperature exceeds approximately 165°C. This circuit has thermal hysteresis, that is, after being activated it keeps the amplifier shut off until the die temperature drops below approximately 150°C. This capability provides an extra safety margin under fault conditions or in any case where there is a transient overpower condition within the amplifier.

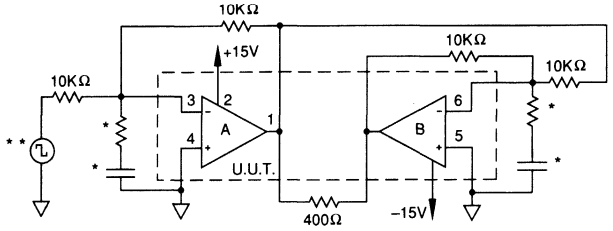
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

TABLE 4 GROUP A INSPECTION

PA21M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiesent Current	I_Q	25°C	15	V_{IN} = 0, A_V = 100		75	mA
1	Input Offset Voltage	V_{OS}	25°C	2.5	V_{IN} = 0, A_V = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	15	V_{IN} = 0, A_V = 100		10	mV
1	Input Offset Voltage	V_{OS}	25°C	20	V_{IN} = 0, A_V = 100		14	mV
1	Input Bias Current + IN	$+I_B$	25°C	15	V_{IN} = 0		1000	nA
1	Input Bias Current –IN	$-I_B$	25°C	15	V_{IN} = 0		1000	nA
1	Input Offset Current	I_{OS}	25°C	15	V_{IN} = 0		500	nA
3	Quiesent Current	I_Q	–55°C	15	V_{IN} = 0, A_V = 100		75	mA
3	Input Offset Voltage	V_{OS}	–55°C	2.5	V_{IN} = 0, A_V = 100		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	15	V_{IN} = 0, A_V = 100		14	mV
3	Input Offset Voltage	V_{OS}	–55°C	20	V_{IN} = 0, A_V = 100		18	mV
3	Input Bias Current + IN	$+I_B$	–55°C	15	V_{IN} = 0		1000	nA
3	Input Bias Current –IN	$-I_B$	–55°C	15	V_{IN} = 0		1000	nA
3	Input Offset Current	I_{OS}	–55°C	15	V_{IN} = 0		500	nA
2	Quiesent Current	I_Q	125°C	15	V_{IN} = 0, A_V = 100		105	mA
2	Input Offset Voltage	V_{OS}	125°C	2.5	V_{IN} = 0, A_V = 100		15	mV
2	Input Offset Voltage	V_{OS}	125°C	15	V_{IN} = 0, A_V = 100		15	mV
2	Input Offset Voltage	V_{OS}	125°C	20	V_{IN} = 0, A_V = 100		19	mV
2	Input Bias Current + IN	$+I_B$	125°C	15	V_{IN} = 0		1000	nA
2	Input Bias Current –IN	$-I_B$	125°C	15	V_{IN} = 0		1000	nA
2	Input Offset Current	I_{OS}	125°C	15	V_{IN} = 0		500	nA
4	Output Voltage I_O= 3A	V_O	25°C	12.5	R_L = 3Ω	9.0		V
4	Output Voltage I_O= 100mA	V_O	25°C	11	R_L = 100Ω	10		V
4	Output Voltage I_O= 1A	V_O	25°C	4.8	R_L = 3Ω	3.0		V
4	Current Limits	I_{CL}	25°C	16	R_L = 3Ω	9.0		V
4	Stability/Noise	E_N	25°C	15	R_L = 500Ω, A_V = 1 C_L = 1.5nF		1.0	mV
4	Crosstalk	XTLK	25°C	15	R_L = 3Ω	50		dB
4	Slew Rate	SR	25°C	15	R_L = 500Ω	.5		V/µS
4	Open Loop Gain	A_{OL}	25°C	15	R_L = 500Ω, F =10Hz	75		dB
4	Common-mode Rejection	CMR	25°C	15	R_L = 500Ω, V_{CM} = 24V	62		dB
6	Output Voltage I_O= 2.67A	V_O	–55°C	12.5	R_L = 3Ω	8.0		V
6	Output Voltage I_O= 100mA	V_O	–55°C	11	R_L = 100Ω	9.8		V
6	Output Voltage I_O= 1A	V_O	–55°C	4.8	R_L = 3Ω	3.0		V
6	Stability/Noise	E_N	–55°C	15	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1.0	mV
6	Slew Rate	SR	–55°C	15	R_L = 500Ω	.5		V/µS
6	Open Loop Gain	A_{OL}	–55°C	15	R_L = 500Ω, F = 10Hz	75		dB
6	Common-mode Rejection	CMR	–55°C	15	R_L = 500Ω, V_{CM} = 24V	62		dB
5	Output Voltage I_O= 1A	V_O	125°C	4.8	R_L = 3Ω	3.1		V
5	Output Voltage I_O= 100mA	V_O	125°C	11	R_L = 100Ω	10		V
5	Output Voltage I_O= 750mA	V_O	125°C	4.0	R_L = 3Ω	2.25		V
5	Stability/Noise	E_N	125°C	15	R_L = 500Ω, A_V = 1, C_L = 1.5nF		1.0	mV
5	Slew Rate	SR	125°C	15	R_L = 500Ω	.5		V/µS
5	Open Loop Gain	A_{OL}	125°C	15	R_L = 500Ω, F = 10Hz	75		dB
5	Common-mode Rejection	CMR	125°C	15	R_L = 500Ω, V_{CM} = 24V	62		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

EVALUATION KIT FOR PA21 PIN-OUT
EK21

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

INTRODUCTION

This easy-to-use kit provides a platform for the evaluation of power op amps that use the PA21 pin-out configuration. It can be used to analyze a multitude of standard or proprietary circuit configurations. In addition, it is flexible enough to do most standard amplifier test configurations.

The schematic for 1/2 of the PC board is shown in Figure 2. The schematic for the other half is identical except part reference designators are primed (i.e. R1 = R1'). Note that all of the components shown on the schematic will probably not be used for any single circuit. The component locations on the PC board (See Figure 3) provide maximum flexibility for a variety of configurations. Also included are loops for current probes as well as connection pads on the edge of the PC board for easy interconnects.

The hardware required to mount the PC board and the device under evaluation to the heatsink are included in the kit. Because of the limitless combination of configurations and component values that can be used, no other parts are included in this kit. However, generic formulas and guidelines are included in the APEX HYBRID & IC HANDBOOK and this evaluation kit documentation.

ASSEMBLY HINTS

The mating sockets included with this kit have recessed nut sockets for mounting the device under evaluation. This allows assembly from one side of the heatsink, making it easy to swap devices under evaluation. The sizes of the stand-offs were selected to allow proper spacing of the board-to-heatsink and allow enough height for components when the assembly is inverted.

PARTS LIST

Part #	Description	Quantity
HS11	Heatsink	1
EK21PC	PC Board	1
MS03	Mating Socket	2
HWRE01	Hardware Kit	1

HWRE01 contains the following:

4	#8 Panhead Screw	4	#6 x 1.25" Panhead Screw
4	#8 .375" Hex Spacer	4	#6 x 5/16" Hex Nut
4	#8 1.00" Hex Stand Off	2	#6 x 1/4" Hex Nut

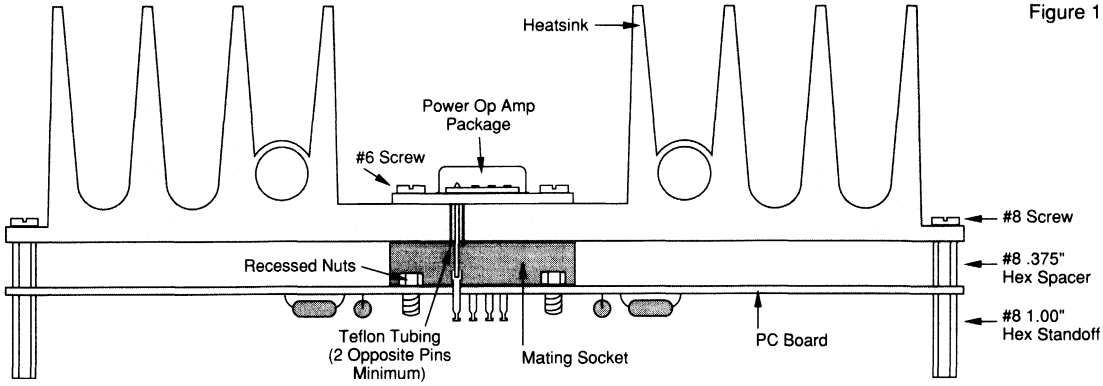
ASSEMBLY

1. Insert a #6 x 5/16" hex nut in each of the nut socket recesses located on the bottom of the mating socket.
2. Insert the socket into the pc board until it is firmly pressed against the ground plane side of the pc board.
3. Solder the socket in place (see Figure 1). Be sure the nuts are in the recesses prior to soldering.
4. Mount the PC board assembly to the heatsink using the stand-offs and spacers included.
5. Apply thermal grease to the bottom of the device under evaluation. Insert into the mating socket through the heatsink.
6. Use the #6 x 1.25" panhead screws to mount the amplifier to the heat sink. Do not overtorque. Recommended mounting torque is 4-7 in-lbs (.45-.79 N•M).

Mounting precautions, general operating considerations, and heatsinking information may be found in the APEX HYBRID & IC HANDBOOK.

NOTE: Refer to HS11 Heatsink note on page 3.

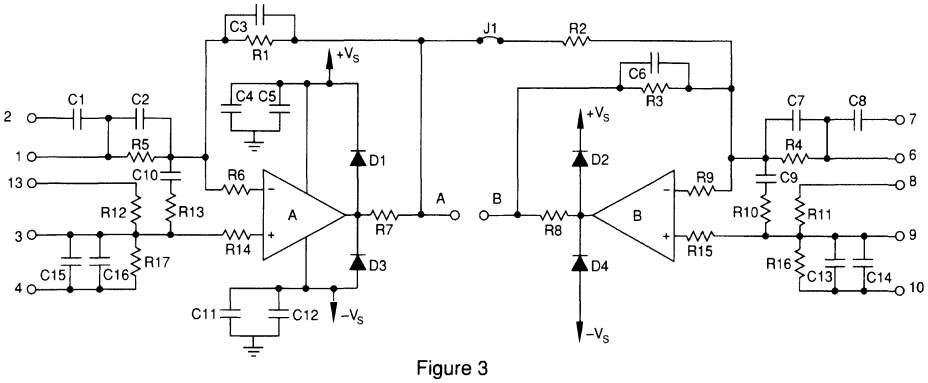
Figure 1



BEFORE YOU GET STARTED

- All Apex amplifiers should be handled using proper ESD precautions!
- Initially set all power supplies to the minimum operating levels allowed in the device data sheet.
- Check for oscillations.
- Always use the heatsink included in this kit with thermal grease and torque the part to the specified 4-7 in-lbs (.45-.79 N•M).
- Do not change connections while the circuit is under power.
- Never exceed any of the absolute maximums listed in the device data sheet.
- Always use adequate power supply bypassing.
- Remember that internal power does not equal load power.
- Do not count on internal diodes to protect the output against sustained, high frequency, high energy kickback pulses.

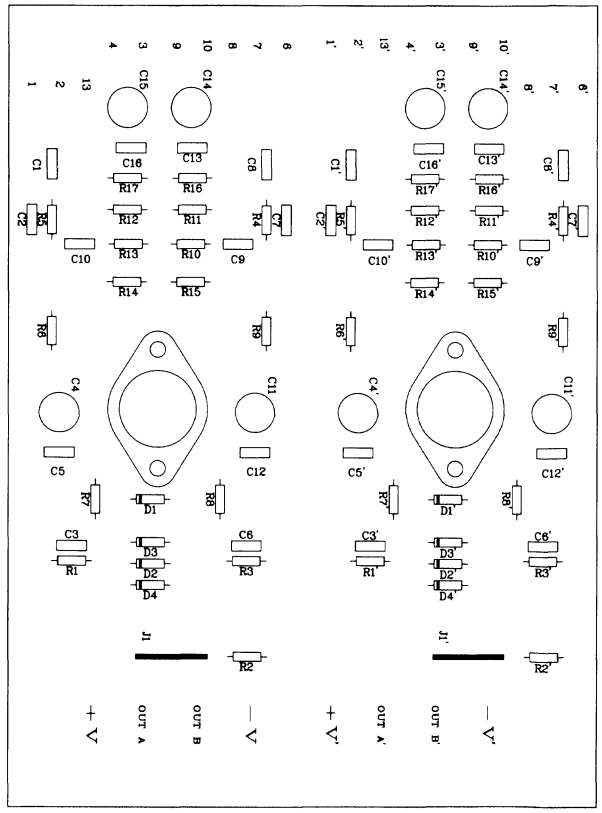
Figure 2



TYPICAL COMPONENT FUNCTIONS

COMPONENT	FUNCTION
R1	Feedback resistor, A side
R2	Input resistor, B side, bridge mode
R3	Feedback resistor, B side
R4	Input resistor, B side
R5	Input resistor, A side
R6	Input bias current measurement (Note 4)
R7	Output current sense resistor or loop for current probe
R8	Output current sense resistor or loop for current probe
R9	Input bias current measurement (Note 4)
R10	Noise gain compensation (Note 1)
R11	Resistor divider network for single supply bias (Note 2)
R12	Resistor divider network for single supply bias (Note 2)
R13	Noise gain compensation (Note 1)
R14	Input bias current measurement
R15	Input bias current measurement
R16	Resistor divider network for single supply bias (Note 2)
R17	Resistor divider network for single supply bias (Note 2)
C1	Input coupling
C2	AC gain set
C3	AC gain or stability (Note 1)
C4	Power supply bypass
C5	Power supply bypass
C6	AC gain or stability (Note 1)
C7	AC gain set
C8	Input coupling
C9	Noise gain compensation (Note 1)
C10	Noise gain compensation (Note 1)
C11	Power supply bypass (Note 3)
C12	Power supply bypass (Note 3)
D1,2,3,4	Flyback protection (Note 5)
C13-16	Bias node noise bypass (Note 2)

Figure 3



NOTES: Refer to the following sections of the APEX HYBRID & IC HANDBOOK as noted.

1. See Stability section of "General Operating Considerations."
2. See "Gen. Operating Considerations," and AN3 "Bridge Circuit Drives."
3. See Power Supplies section of "General Operating Considerations."
4. See "Parameter Definitions and Test Methods."
5. See Amplifier Protection section of "Gen. Operating Considerations."

BRIDGE MODE OPERATION

There are two types of bridge mode operation that will be covered in this section; dual (or split) supply and single supply. The PA21 is well suited for both types of bridge mode operation. If another vendor's pin compatible part is to be compared to the PA21, a close look at output swing and input common mode range is in order. The features that make the PA21 an excellent choice for bridge operation are not included in most other amplifiers. A lack of common mode range may cause permanent damage to other pin compatible parts and the inability of other amplifiers to swing close to the supply rails may cause a lack of available output voltage at the load as well as increase internal dissipation.

The circuit shown in Figure 4 is a dual supply bridge using the "master-slave" configuration. Resistors R 6,7,8,9,14,15 and J1 should be shorts. The available output voltage swing is Vss–(2*Vsat). If operating a PA21A at 3 Amps and 30 Volts total supply this translates to:

$$V_{AB}(max) = 30–(2*3.5) = 23$$

Of course this 23 volts may be applied in either direction across the load. To set the gain of the circuit you must determine the desired voltage across the load at Vin = full scale. Inserting these values into the following equation will yield the ratio of R1 to R5.

$$(V_{AB}/(2*Vin)) = R1/R5$$

The values of R 1,2,3, and 5 should be chosen such that input bias current will not cause an error voltage that is unacceptable. Set R2

Figure 4
Dual Supply Bridge

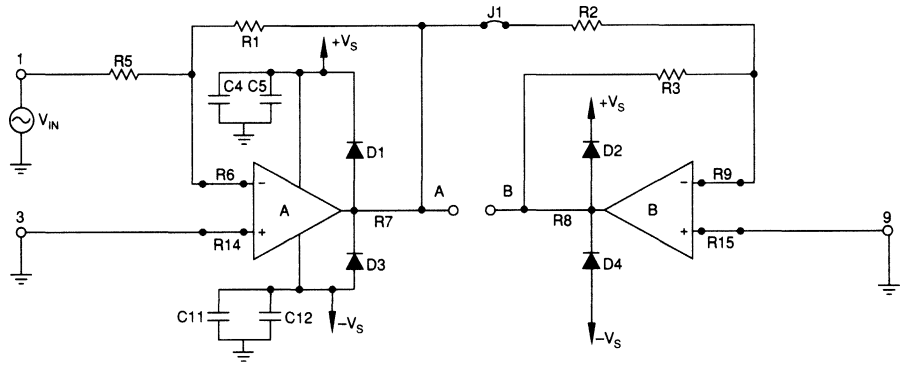
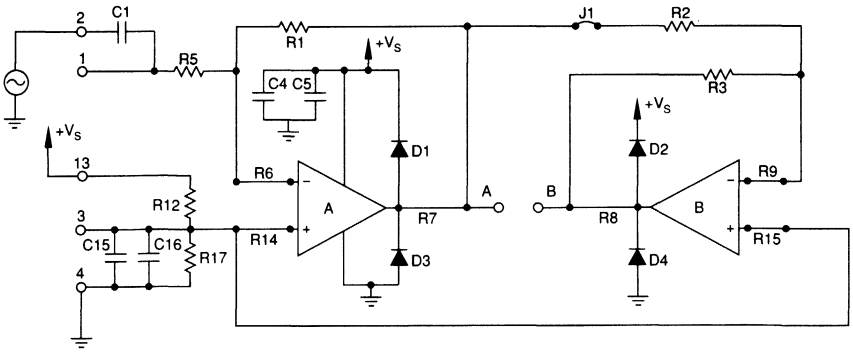


Figure 5
Single Supply Bridge



equal to R3 to configure the slave amplifier as a unity gain inverter.

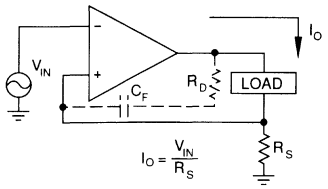
Figure 5 shows a typical single supply bridge circuit for an AC coupled input signal. DC coupled inputs may require a different topology to accommodate proper gain and offset terms for a desired transfer function.

The gain and output voltage capability for the single supply bridge are determined the same way as the dual supply bridge (see AN#2). The difference is the bias requirement for the slave amplifier. The noninverting input of the slave amplifier should be biased at mid supply, and must be bypassed.

HS11 HEATSINK NOTE

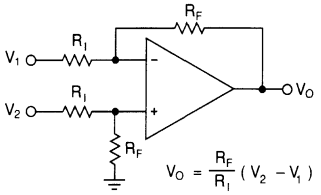
The HS11 Heatsink is provided in this evaluation kit to **guarantee** adequate **thermal** design through heat removal from the part under evaluation. Once maximum power dissipation for the application is determined (refer to "General Operating Considerations" and Application Note 11 in the APEX HYBRID & IC HANDBOOK), the final mechanical design will probably require substantially less heatsinking.

VOLTAGE-TO-CURRENT CONVERSION
NON-INVERTING CONFIGURATION



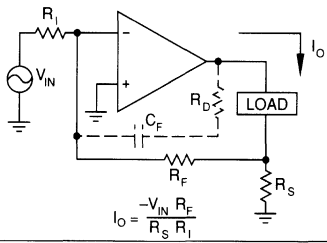
$$I_O = \frac{V_{IN}}{R_S}$$

DIFFERENCE AMPLIFIER



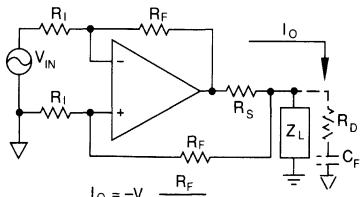
$$V_O = \frac{R_F}{R_I}(V_2 - V_1)$$

VOLTAGE-TO-CURRENT CONVERSION
INVERTING CONFIGURATION



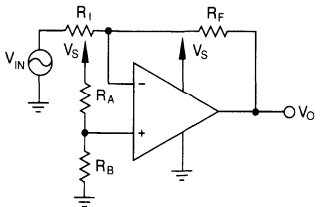
$$I_O = \frac{-V_{IN}}{R_S}\frac{R_F}{R_I}$$

VOLTAGE-TO-CURRENT CONVERSION
IMPROVED HOWLAND CURRENT PUMP



$$I_O = -V_{IN}\frac{R_F}{R_I R_S}$$

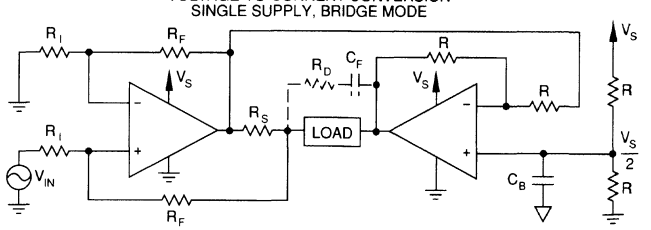
SINGLE SUPPLY OPERATION
INVERTING CONFIGURATION



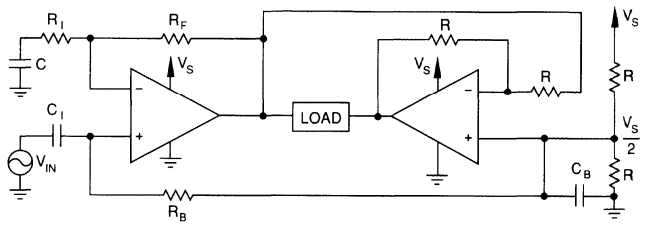
$$V_O\ (\text{Bias}) = \left(\frac{V_S}{R_A + R_B}\frac{R_B}{}\right)\left(1 + \frac{R_F}{R_I}\right)$$

$$V_O\ (\text{Signal}) = V_{IN}\left(-\frac{R_F}{R_I}\right)$$

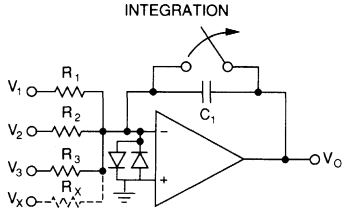
VOLTAGE-TO-CURRENT CONVERSION
SINGLE SUPPLY, BRIDGE MODE



VOLTAGE FOLLOWER WITH GAIN
SINGLE SUPPLY, BRIDGE MODE

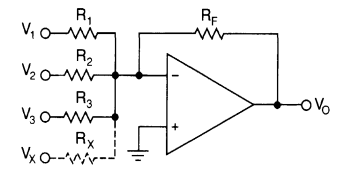


INTEGRATION



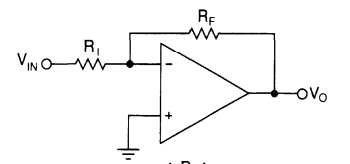
$$V_O = \frac{T}{C_1}\int_0^T \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)dt$$

SUMMING / SCALING



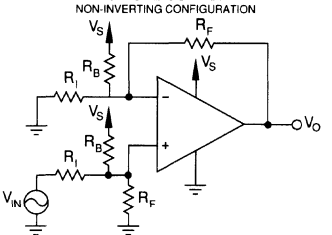
$$V_O = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_X}{R_X}\right)$$

INVERTER



$$V_O = -\left(\frac{R_F}{R_I}\right)V_{IN}$$

SINGLE SUPPLY
NON-INVERTING CONFIGURATION



i) $V_O = \frac{R_F}{R_I}$

ii) For $V_{IN} = 0$

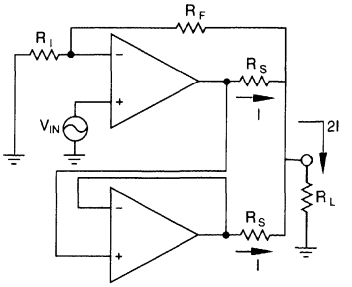
$$V_{CM} = \frac{V_S\ (R_I // R_F)}{R_B + (R_I // R_F)}$$

iii) $V_{CM\Delta} = \frac{V_{IN}\ (R_B // R_F)}{R_I + (R_B // R_F)}$

iv) For $V_{IN} > 0$

$$V_{CM} = V_{CM}\ @\ V_{IN} = 0 + V_{CM\Delta}$$

PARALLEL OPERATION



POWER DUAL OPERATIONAL AMPLIFIERS

PA25 • PA25A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- **PIN COMPATIBLE WITH OPA2541**
- **LOW COST DUAL POWER OP AMP**
- **WIDE COMMON MODE RANGE—**
  Includes negative supply
- **WIDE SUPPLY VOLTAGE RANGE**
  Single supply: 5V to 40V
  Split supplies: ±2.5V to ±20V
- **HIGH EFFICIENCY — IVs-2.0VI at 2.5A typ**
- **HIGH OUTPUT CURRENT — 3A min (PA25A)**
- **INTERNAL CURRENT LIMIT**
- **INTERNAL THERMAL SHUTDOWN**
- **LOW DISTORTION**

APPLICATIONS

- **HALF & FULL BRIDGE MOTOR DRIVERS**
- **AUDIO POWER AMPLIFIER**
  STEREO — 30W RMS per channel
  BRIDGE — 60W RMS per package
- **IDEAL FOR SINGLE SUPPLY SYSTEMS**
  5V — Peripherals
  12V — Automotive
  28V — Avionic

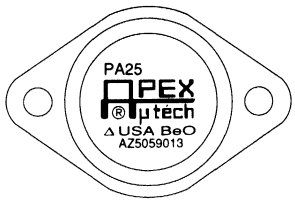
DESCRIPTION

The PA25 consists of monolithic dual power op amp in a 8-pin hermetic TO-3 package. Putting two power op amps in one package and on one die results in an extremely cost effective solution for applications requiring multiple amplifiers per board or bridge mode configurations. The addition of an external output stage compensation network will eliminate the possibility of parasitic oscillations usually found in monolithic op amp output stages.

The wide common mode input range includes the negative rail, facilitating single supply applications. It is possible to have a "ground based" input driving a single supply amplifier with ground acting as the "second" or "bottom" supply of the amplifier.

The output stage is also well protected in the PA25. It possesses internal current limit circuits as well as internal thermal shutdown circuitry. The thermal shutdown operates with hysteresis, first engaging at approximately Tj = 165°C and not disengaging until Tj < 150°C. While the device is well protected, the Safe Operating Area (SOA) curve must be observed. Proper heatsinking is required for maximum reliability.

This hybrid integrated circuit utilizes thick film conductors and a semiconductor chip to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.



TYPICAL APPLICATION

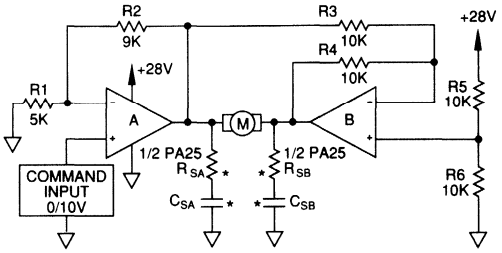
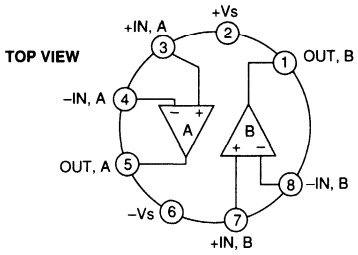


Figure 1: Bidirectional Speed Control from a Single Supply
* See "Monolithic Amplifier Stability Considerations"

R1 and R2 set up amplifier A in a non-inverting gain of 2.8. Amp B is set up as a unity gain inverter driven from the output of amp A. Note that amp B inverts signals about the reference node, which is set at mid-supply (14V) by R5 and R6. When the command input is 5V, the output of amp A is 14V. Since this is equal to the reference node voltage, the output of amp B is also 14V, resulting in 0V across the motor. Inputs more positive than 5V result in motor current flow from left to right (see Figure 1). Inputs less positive than 5V drive the motor in the opposite direction.

The PA25 is especially well-suited for this application. The extended common mode range of the PA25 allows command inputs as low as 0V. Its superior output swing abilities let it drive within 2V of supply at an output current of 2A. This means that a command input that ranges from 0V to 10V will drive a 24V motor from full scale CCW to full scale CW at up to ±2A. A single power op amp with an output swing capability of Vs –6 would require ±30V supplies and would be required to swing 48V p-p at twice the speed to deliver an equivalent drive.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, total	5V to 40V, 45V (50ms)
OUTPUT CURRENT	SOA
POWER DISSIPATION, internal (per amplifier)	25W
POWER DISSIPATION, internal (both amplifiers)	36W
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S$, $-V_S$–.5V
JUNCTION TEMPERATURE, max[1]	150°C
TEMPERATURE, pin solder - 10 sec max	300°C
TEMPERATURE RANGE, storage	–65°C to 150°C
OPERATING TEMPERATURE RANGE, case	–55°C to 125°C

SPECIFICATIONS

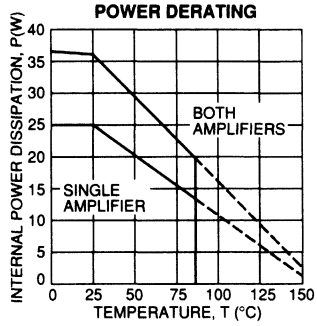
		PA25			PA25A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			1.5	10		.5	4	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		–15			–10		µV/°C
BIAS CURRENT, initial			35	1000		*	250	nA
COMMON MODE RANGE	Full temperature range	$-V_S$–.3		$+V_S$–2	*		*	V
COMMON MODE REJECTION, DC	Full temperature range	60	85		*	*		dB
POWER SUPPLY REJECTION	Full temperature range	60	80		*	*		dB
CHANNEL SEPARATION	I_{OUT} = 1A, F = 1KHz	50	68		*	*		dB
GAIN								
OPEN LOOP GAIN	Full temperature range	80	100		*	*		dB
GAIN BANDWIDTH PRODUCT	Av = 40dB		800			*		kHz
PHASE MARGIN	Full temperature range		65			*		°
POWER BANDWIDTH	V_O(p-p) = 28V		13.6			*		kHz
OUTPUT								
CURRENT, peak		2.5			3			A
CURRENT, limit			3.0			4.0		A
SLEW RATE		.5	1.2		*	*		V/µs
CAPACITIVE LOAD DRIVE	A_V = 1		.22			*		µF
VOLTAGE SWING	Full temp. range, I_O = 100mA	$\|V_S\|$ –1.0	$\|V_S\|$ –0.8		*	*		V
VOLTAGE SWING	Full temp. range, I_O = 1A	$\|V_S\|$ –1.8	$\|V_S\|$ –1.3		*	*		V
VOLTAGE SWING	I_O = 2.5A (PA25), 3A (PA25A)	$\|V_S\|$ –3.0	$\|V_S\|$ –2.0		$\|V_S\|$ –3.5	$\|V_S\|$ –3		V
POWER SUPPLY								
VOLTAGE, V_{SS}[3]		5[4]	30	40	*	*	*	V
CURRENT, quiescent, total			45	90		*	*	mA
THERMAL								
RESISTANCE, junction to case								
DC, single amplifier			5.0			*		°C/W
DC, both amplifiers[5]			3.4			*		°C/W
AC, single amplifier			3.7					°C/W
AC, both amplifiers[5]			2.4					°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		85	–25		85	°C

NOTES: * The specification of PA25A is identical to the specification for PA25 in applicable column to the left.

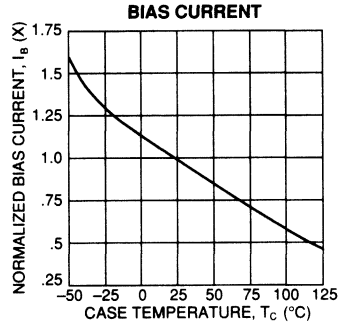
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Unless otherwise noted, the following conditions apply: $\pm V_S = \pm 15V$, $T_C = 25°C$.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. V_{SS} denotes the total rail-to-rail supply voltage.
4. Thermal shutdown and current limit may not function properly below V_{SS} = 6V, however SOA violations are unlikely in this area.
5. Rating applies when power dissipation is equal in the two amplifiers.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

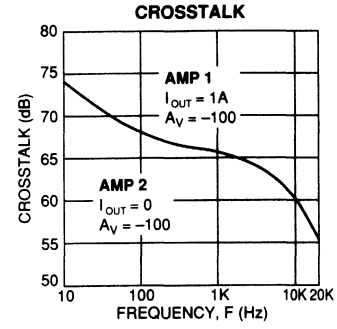
POWER DERATING



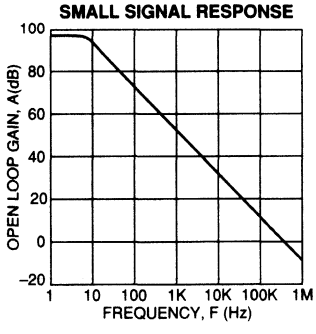
BIAS CURRENT



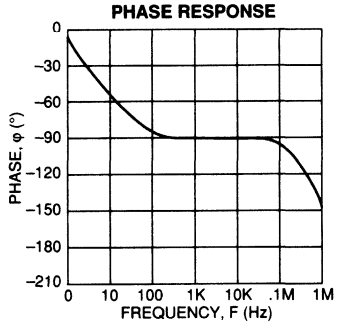
CROSSTALK



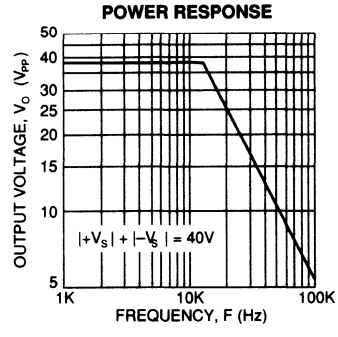
SMALL SIGNAL RESPONSE



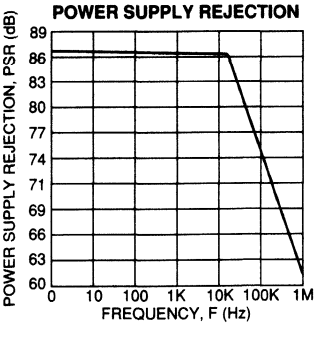
PHASE RESPONSE



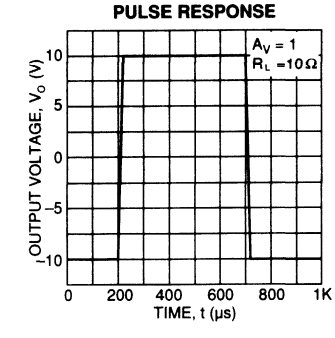
POWER RESPONSE



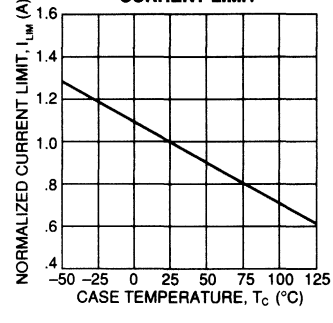
POWER SUPPLY REJECTION



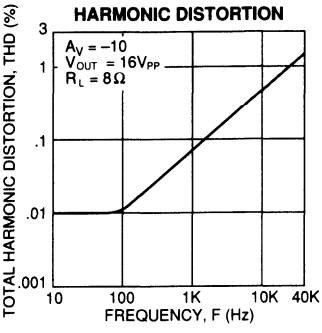
PULSE RESPONSE



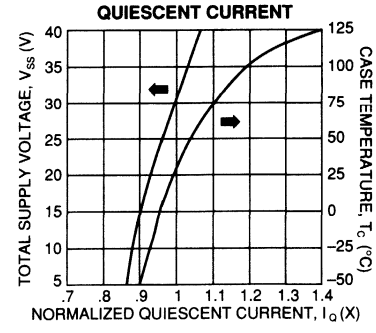
CURRENT LIMIT



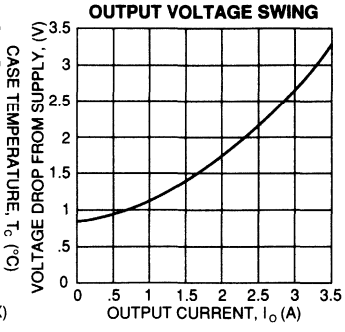
HARMONIC DISTORTION



QUIESCENT CURRENT



OUTPUT VOLTAGE SWING

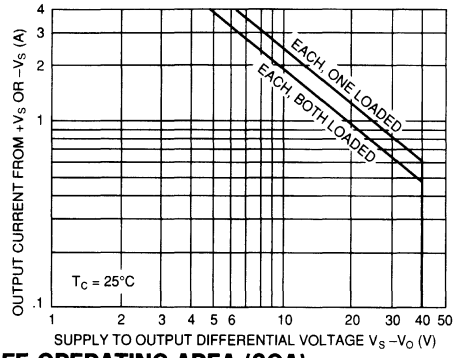


GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

Current limit is internal to the PA25, the typical value is shown in the current limit specification.



SAFE OPERATING AREA (SOA)

The SOA curves combine the effect of all limits for this power op amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

$\pm V_s$	CAPACITIVE LOAD	INDUCTIVE LOAD
20V	200µF	7.5mH
15V	500µF	25mH
10V	5mF	35mH
5V	50mF	150mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 6V below the supply rail while the amplifier is current limiting, the inductor should be capacitively coupled or the supply voltage must be lowered to meet SOA criteria.

NOTE: For protection against sustained, high energy flyback, external fast-recovery diodes should be used.

STABILITY

The PA25 is internally compensated for unity gain stability, no additional compensation is required.

THERMAL SHUTDOWN PROTECTION

The PA25 has a sophisticated circuit that shuts off internal current supplies when the die temperature exceeds approximately 165°C. This circuit has thermal hysteresis, that is, after being activated it keeps the amplifier shut off until the die temperature drops below approximately 150°C. This capability provides an extra safety margin under fault conditions or in any case where there is a transient overpower condition within the amplifier.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the Tc = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

MONOLITHIC AMPLIFIER STABILITY CONSIDERATIONS

All monolithic power op amps use output stage topologies that present special stability problems. This is primarily due to non-complementary (both devices are NPN) output stages with a mismatch in gain and phase response for different polarities of output current. It is difficult for the op amp manufacturer to optimize compensation for all operating conditions.

The problem manifests itself most often as a parasitic oscillation, meaning that it occurs only at certain values of output current and/or voltage, and can be load dependent. This parasitic oscillation may not always reveal itself when designing with these parts, but should be guarded against and compensated for to insure maximum reliability. High frequency oscillations quickly raise output stage junction temperatures in power op amps.

Figure 2 illustrates a circuit useful for evaluating the "parasitic stability" of a power op amp. The gain of 100 is high enough that any oscillation observed is likely to be due to a "local oscillation" problem in the output stage, rather than an overall oscillation of the entire power amplifier. The 10 ohm load is selected to draw current from the amplifier without loading it enough to swamp out the oscillations. The high test frequency of 10kHz improves the visibility of any small parasitics likely to occur. A sine-wave is the ideal waveform to display a parasitic, although a triangle waveform may be used. Whatever the waveform, and especially with a square wave, sweep the waveform amplitude from zero to output voltage clipping while checking for parasitics.

The PA25 will pass this test with the recommended R-C network of 1 ohm in series with 0.1µF from output to AC common (ground or a supply rail, with adequate bypass capacitors). It will be noted that this test will also reveal other deficiencies in amplifiers such as distortion including crossover distortion. The PA25 will be observed to perform well in this regard.

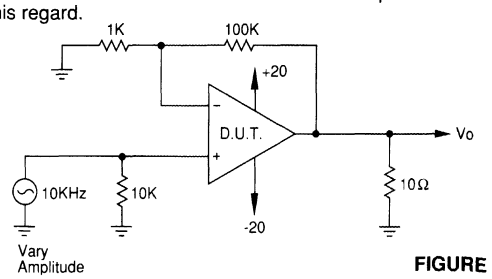


FIGURE 2

DUAL OPERATIONAL AMPLIFIER
PA25DIE

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ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	40V
OUTPUT CURRENT, continuous	2.5A
INPUT VOLTAGE, differential	$\pm V_S$
INPUT VOLTAGE, common mode	$+V_S - V_S - 0.3$
TEMPERATURE, junction	150°C

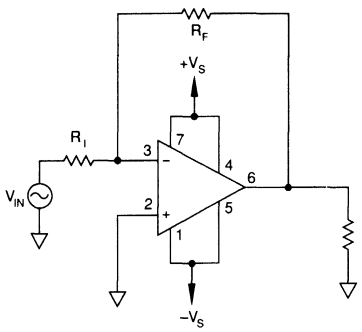
NOTE: Refer to parent product data sheet PA21 for typical AC electrical characteristics, precautions, applications and other test parameters.

TYPICAL SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
POWER SUPPLY VOLTAGE	$+V_S$ to $-V_S$	5	12	40	V
OFFSET VOLTAGE	V_{OUT} = 0, I_{OUT} = 0		±2		mV
QUIESCENT CURRENT	$+I_S$ Total		35		mA
BIAS CURRENT	V_{OUT} = 0		80		nA
OPEN LOOP GAIN	F = 0 Hz		100		dB
COMMON MODE REJECTION RATIO	Delta V_{CM} = 3V		85		dB
SLEW RATE	A =1, V_{OUT} = $6V_{P-P}$		1		V/µs
CHANNEL SEPARATION	I_{OUT} = 100mA, F = 1kHz		60		dB
VOLTAGE SWING	I_{OUT} = 1A, V_{CC} = ±6V		10.0		V_{P-P}
VOLTAGE SWING	I_{OUT} = 1A, V_{CC} = V_{CC} = $\pm 6V_{BOOST}$ = ±9V		10.5		V_{P-P}
POWER SUPPLY REJECTION RATIO	V_S = ±15V		80		dB

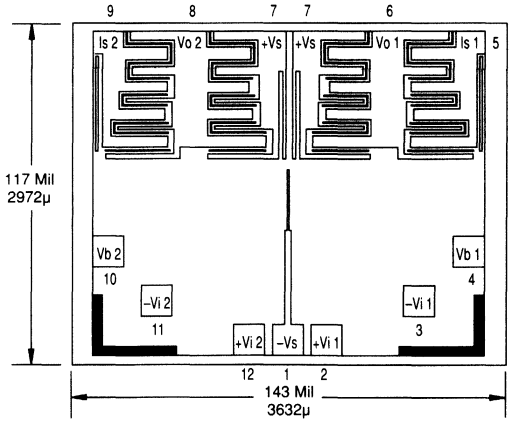
NOTES: 1. V_S = ±150 V unless otherwise stated. T_A = 25°C.

TYPICAL EXTERNAL CONNECTIONS



Pad	Function
2	Non-inverting Input —AMP 1
3	Inverting Input— AMP 1
4	V_{BOOST} Input — AMP 1
5	Current Sense Output — AMP 1
6	Output — AMP 1
12	Non-inverting Input —AMP 2
11	Inverting Input— AMP 2
10	V_{BOOST} Input — AMP 2
9	Current Sense Output — AMP 2
8	Output — AMP 2
7	Positive Supply Input — Both Amplifiers
1	Negative Supply Input — Both Amplifiers

DIE LAYOUT



Thickness: 18 Mil ±2 Mil
Backside: Ni Ag 20,000 Å (min)
Bond pad: 10 Mil sq (254µ)
NOTE: Backside at $-V_S$ potential.

NOTES:

HIGH VOLTAGE POWER OPERATIONAL AMPLIFIER

PA41

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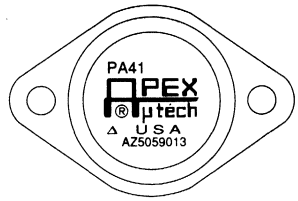
FEATURES

- MONOLITHIC MOS TECHNOLOGY
- LOW COST
- HIGH VOLTAGE OPERATION — 350V
- LOW QUIESCENT CURRENT — 2mA
- NO SECOND BREAKDOWN
- HIGH OUTPUT CURRENT — 60 mA



APPLICATIONS

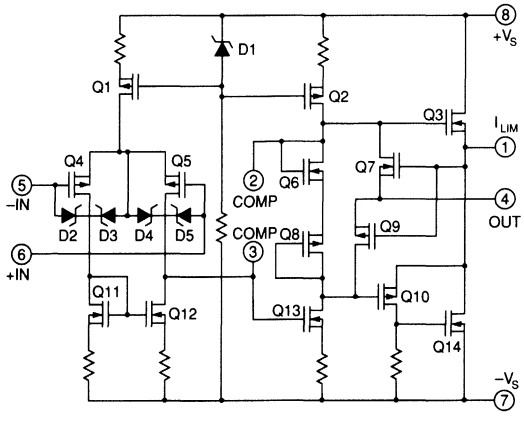
- PIEZO ELECTRIC POSITIONING
- ELECTROSTATIC TRANSDUCER & DEFLECTION
- DEFORMABLE MIRROR FOCUSING
- BIOCHEMISTRY STIMULATORS
- COMPUTER TO VACUUM TUBE INTERFACE

DESCRIPTION

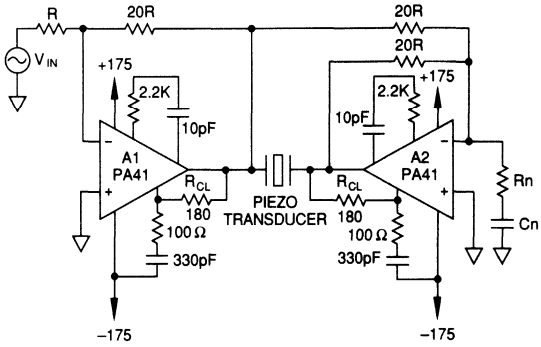
The PA41 is a high voltage monolithic MOSFET operational amplifier achieving performance features previously found only in hybrid designs while increasing reliability. Inputs are protected from excessive common mode and differential mode voltages. The safe operating area (SOA) has no second breakdown limitations and can be observed with all type loads by choosing an appropriate current limiting resistor. External compensation provides the user flexibility in choosing optimum gain and bandwidth for the application.

The PA41 is hermetically sealed and all circuitry is isolated from the case by an aluminum nitride (AlN) substrate.

EQUIVALENT SCHEMATIC



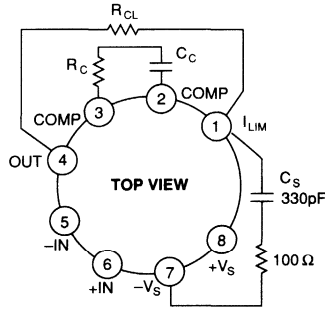
TYPICAL APPLICATION



LOW COST 660V p-p PIEZO DRIVE

Two PA41 amplifiers operated as a bridge driver for a piezo transducer provides a low cost 660 volt total drive capability. The R_N C_N network serves to raise the apparent gain of A2 at high frequencies. If R_N is set equal to R the amplifiers can be compensated identically and will have matching bandwidths.

EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	18pF	2.2KΩ
≥10	10pF	2.2KΩ
≥30	3.3pF	2.2KΩ

C_S, C_C ARE NPO RATED FOR FULL SUPPLY VOLTAGE.

$$R_{CL} = \frac{3}{I_{LIM}}$$

NOTE: Recommended mounting torque is 4-7 in•lbs (.45 -.79 N•m)

CAUTION: The use of compressible, thermally conductive insulators may void warranty.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous within SOA	60 mA
POWER DISSIPATION, continuous @ T_C = 25°C	12W
INPUT VOLTAGE, differential	±16 V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder – 10 sec	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
TEMPERATURE RANGE, powered (case)	–55 to +125°C

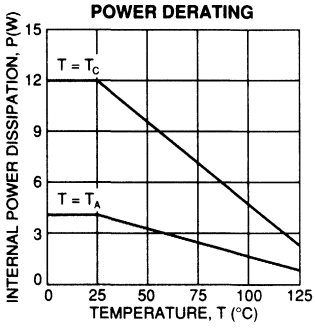
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. temperature[4]	Full temperature range		40	65	µV/°C
OFFSET VOLTAGE, vs supply			20	32	µV/V
OFFSET VOLTAGE, vs time			75		µV √kh
BIAS CURRENT, initial			5	50	pA
BIAS CURRENT, vs supply			.2	.5	pA/V
OFFSET CURRENT, initial			2.5	50	pA
INPUT IMPEDANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			5		pF
COMMON MODE, voltage range		$\pm V_S$–12			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V DC	84	94		dB
NOISE, broad band	10kHz BW, R_S = 1KΩ		50		µV RMS
NOISE, low frequency	1-10 Hz		110		µV p-p
GAIN					
OPEN LOOP at 15Hz	R_L = 5KΩ	94	106		dB
BANDWIDTH, open loop			1.6		MHz
POWER BANDWIDTH	C_C = 10pf, 280V p-p		26		kHz
PHASE MARGIN	Full temperature range		60		°
OUTPUT					
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–9		V
CURRENT, peak[5]		80			mA
CURRENT, continuous		60			mA
SETTLING TIME to .1%	C_C = 10pF, 10V step, A_V = –10		12		µs
SLEW RATE	C_C = OPEN		40		V/µs
CAPACITIVE LOAD	A_V = +1	10			nF
RESISTANCE[6], no load	R_{CL} = 0		150		Ω
RESISTANCE, 20mA load	R_{CL} = 0		25		Ω
POWER SUPPLY					
VOLTAGE[3]	See Note 3	±50	±150	±175	V
CURRENT, quiescent		.9	1.4	2.0	mA
THERMAL					
RESISTANCE, AC junction to case	F > 60Hz		5.4	6.5	°C/W
RESISTANCE, DC junction to case	F < 60Hz		9	10.4	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	°C

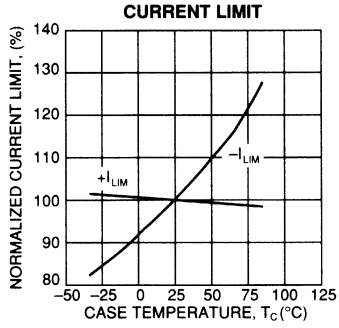
NOTES:
1. Unless otherwise noted T_C = 25°C, C_C = 18pF, R_C = 2.2KΩ. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF. For guidance, refer to heatsink data sheet.
3. Derate maximum supply voltage .5 V/°C below case temperature of 25°C. No derating is needed above T_C = 25°C.
4. Sample tested by wafer lot to 95%.
5. Guaranteed but not tested.
6. The selected value of R_{CL} must be added to the values given for total output resistance.

CAUTION The PA41 is constructed from MOSFET transistors. ESD handling procedures must be observed.

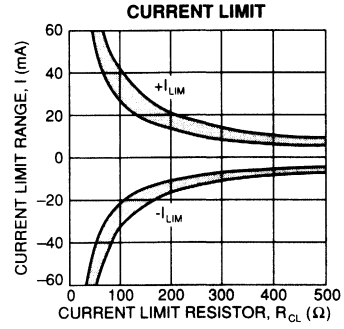
POWER DERATING



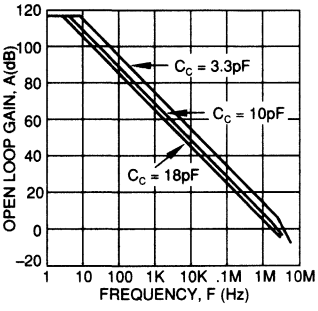
CURRENT LIMIT



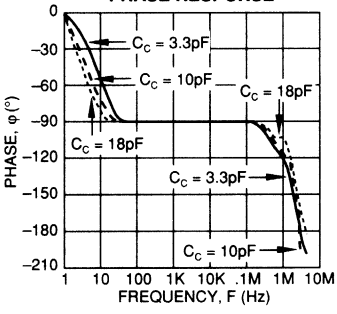
CURRENT LIMIT



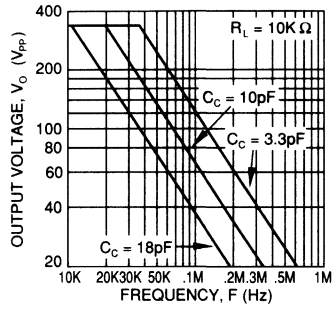
SMALL SIGNAL RESPONSE



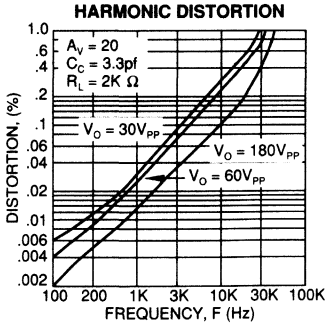
PHASE RESPONSE



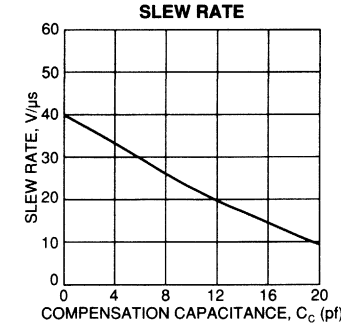
POWER RESPONSE



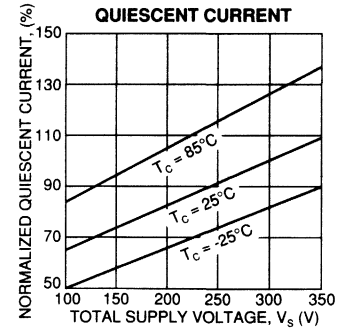
HARMONIC DISTORTION



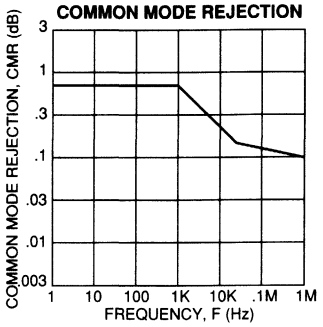
SLEW RATE



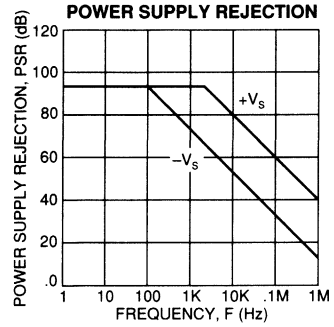
QUIESCENT CURRENT



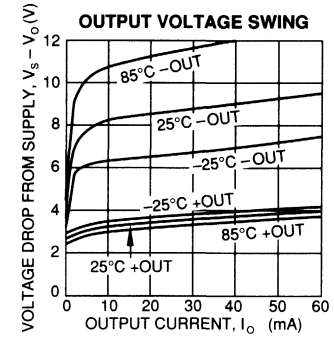
COMMON MODE REJECTION



POWER SUPPLY REJECTION



OUTPUT VOLTAGE SWING



GENERAL

Please read the "General Operating Considerations" section of the handbook, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the applications notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation the current limit resistor, R_{CL}, must be connected as shown in the external connection diagram. The minimum value is 33 ohms, however for optimum reliability the resistor value should be set as high as possible. The value can be estimated as follows with the maximum practical value of 500 ohms.

$$R_{CL} = \frac{3}{I_{LIM}}$$

Use the typical performance graphs as a guide for expected variations in current limit value with a given R_{CL} and variations over temperature. The selected value of R_{CL} must be added to the specified typical value of output resistance to calculate the total output resistance. Since the load current passes through R_{CL} the value selected also affects the output voltage swing according to:

$$V_R = I_O * R_{CL}$$

where V_R is the voltage swing reduction.

When the amplifier is current limiting, there may be small signal spurious oscillation present during the current limited portion of the negative half cycle. The frequency of the oscillation is not predictable and depends on the compensation, gain of the amplifier, and load. The oscillation will cease as the amplifier comes out of current limit.

INPUT PROTECTION

The PA41 inputs are protected against common mode voltages up the supply rails and differential voltages up to ±16 volts as well as static discharge. Differential voltages exceeding 16 volts will be clipped by the protection circuitry. However, if more than a few milliamps of current is available from the overload source, the protection circuitry could be destroyed. The protection circuitry includes 300 ohm current limiting resistors at each input, but this may be insufficient for severe overloads. It may be necessary to add external resistors to the application circuit where severe overload conditions are expected. Limiting input current to 1mA will prevent damage.

STABILITY

The PA41 has sufficient phase margin when compensated for unity gain to be stable with capacitive loads of at least 10 nF. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 1K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

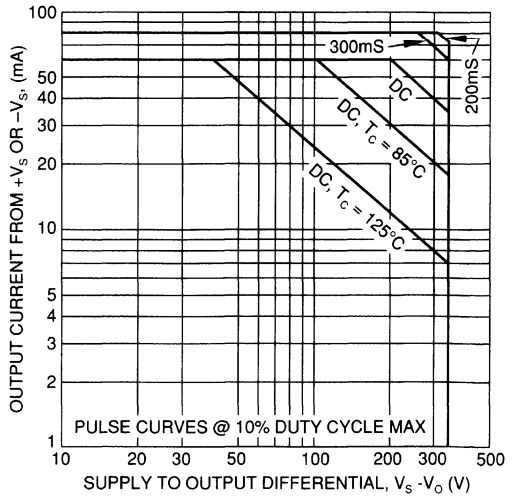
The PA41 is externally compensated and performance can be tailored to the application. Use the graphs of small signal gain and phase response as well as the graphs for slew rate and power response as a guide. The compensation capacitor C_C must be rated at 350V working voltage. The compensation capacitor and associated resistor R_C must be mounted closely to the amplifier pins to avoid spurious oscillation. An NPO capacitor is recommended for compensation.

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the die metallization.
2. The temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



HIGH VOLTAGE OPERATIONAL AMPLIFIER
PA41DIE

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	350V
OUTPUT CURRENT, continuous	60mA
INPUT VOLTAGE, differential	±16V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction	150°C

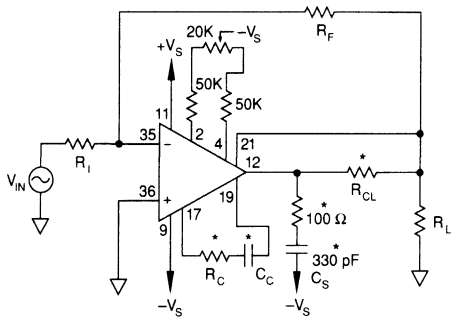
NOTE: Refer to parent product data sheet PA41 for typical AC electrical characteristics, precautions, applications and other test parameters.

DC WAFER PROBED SPECIFICATIONS

PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
OFFSET VOLTAGE, initial			15	30	mV
OFFSET VOLTAGE, vs. supply	V_S = ±50 V to ±175 V		20	32	µV/V
BIAS CURRENT, initial			10	50	pA
COMMON MODE REJECTION	V_{CM} = ±90V DC	84	94		dB
VOLTAGE SWING	I_O = 40mA	$\pm V_S$–12	$\pm V_S$–9		V
SUPPLY CURRENT, quiescent		.9	1.4	2.0	mA

NOTES: 1. V_S = ±150 V unless otherwise stated. T_A = 25°C.

TYPICAL EXTERNAL CONNECTIONS

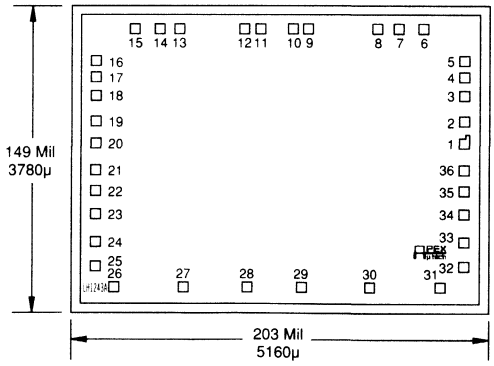


* Required component and value if given.
Optional balance components are recommended values.
C_S, C_C are NPO, rated for full supply voltage $-V_S$ to $+V_S$.

NOTE: Diagram for connection illustration only.
All op amp configurations are possible.

Pad	Function	Pad	Function
2	Balance	17	Compensation
4	Balance	19	Compensation
9	– Supply	21	Current Limit
11	+ Supply	35	– Input
12	Output	36	+ Input

DIE LAYOUT



Thickness: 20 Mil (508µ)
Backside: Ti (500Å) Au (3000Å)
Bond pad: 4.9 Mil sq (125µ) Al
Bond pads 17 and 10 are connected
Make no connection to bond pads not listed by function
NOTE: Backside at $-V_S$ potential.
Make no connection.

CAUTION PA41DIE is a MOSFET amplifier. ESD handling procedures must be observed.

NOTES:

POWER OPERATIONAL AMPLIFIERS
PA51 • PA51A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- WIDE SUPPLY RANGE — ±10 to ±40V
- HIGH OUTPUT CURRENT — ±10A Peak
- SECOND SOURCEABLE — OPA501, 8785
- CLASS "C" OUTPUT — Low Cost
- LOW QUIESCENT CURRENT — 2.6mA

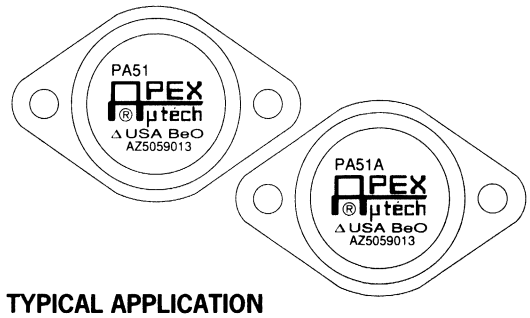
APPLICATIONS

- DC SERVO AMPLIFIER
- MOTOR/SYNCHRO DRIVER
- VALVE AND ACTUATOR CONTROL
- DC OR AC POWER REGULATOR

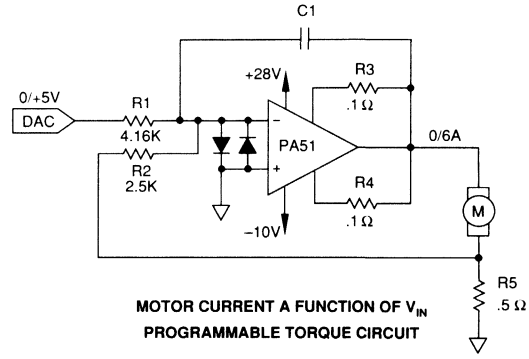
DESCRIPTION

The PA51 and PA51A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary common emitter output stage is protected against transient inductive kickback and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended. Do not use isolation washers!

This hybrid integrated circuit utilizes thick film conductors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible isolation washers may void the warranty.



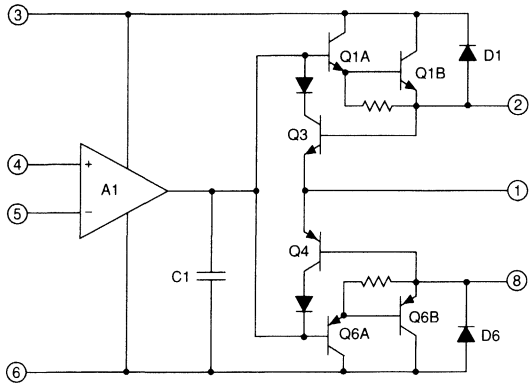
TYPICAL APPLICATION



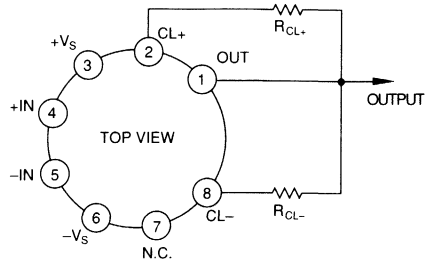
MOTOR CURRENT A FUNCTION OF V_{IN}
PROGRAMMABLE TORQUE CIRCUIT

The linear relationship of torque output to current input of the modern torque motor makes this simple control circuit ideal for many material processing and testing applications. The sense resistor develops a feedback voltage proportional to motor current and the small signal properties of the Power Op Amp insure accuracy. With this closed loop operation, temperature induced impedance variations of the motor winding are automatically compensated.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	80V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	$\pm V_S$ –3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, junction[1]	200°C
TEMPERATURE, pin solder -10s	300°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

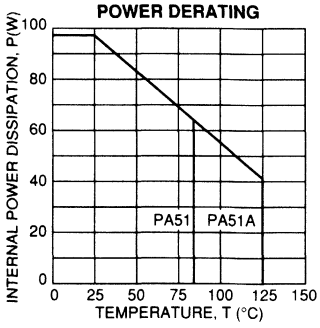
SPECIFICATIONS

		PA51			PA51A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±5	±10		±2	±.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±35			*		µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		±15	±40		*	±20	nA
BIAS CURRENT, vs. temperature	Full temperature range		±.05			*		nA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±.02			*		nA/V
OFFSET CURRENT, initial	T_C = 25°C		±5	±12		±2	±3	nA
OFFSET CURRENT, vs. temperature	Full temperature range		±.01			*		nA/°C
INPUT IMPEDANCE, common mode	T_C = 25°C		250			*		MΩ
INPUT IMPEDANCE, differential	T_C = 25°C		10			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range	$\pm V_S$–6	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	T_C = 25°C, $V_{CM} = \pm V_S$ –6V	70	110		80	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	94	115		94	*		dB
GAIN BANDWIDTH PRODUCT @ 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, $V_O = 40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S$–8	$\pm V_S$–5		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S$–6	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S$–6			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.6		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±28	±36	*	±34	±40	V
CURRENT, quiescent	T_C = 25°C		2.6	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	–55		+125	°C

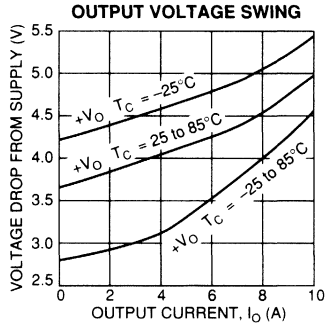
NOTES: * The specification of PA51A is identical to the specification for PA51 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage specified under the TYP rating applies unless otherwise noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

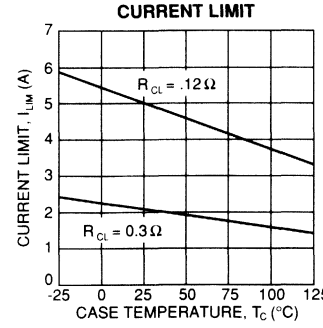
POWER DERATING



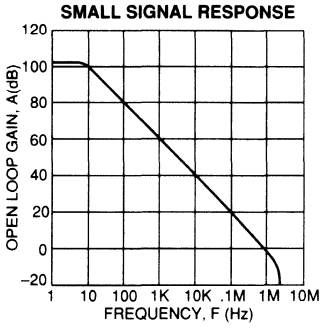
OUTPUT VOLTAGE SWING



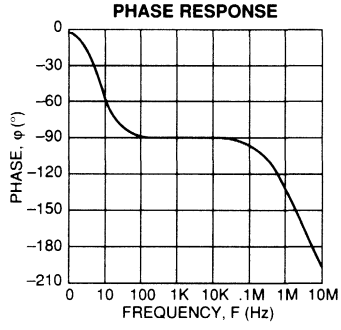
CURRENT LIMIT



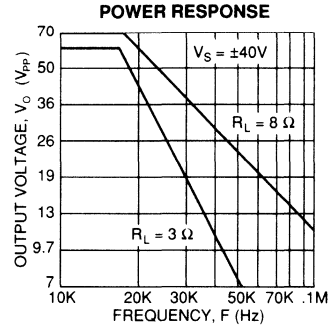
SMALL SIGNAL RESPONSE



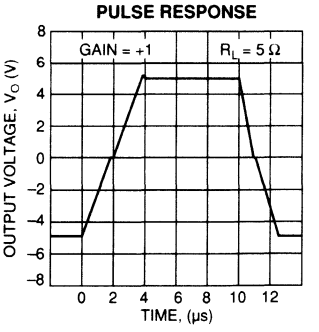
PHASE RESPONSE



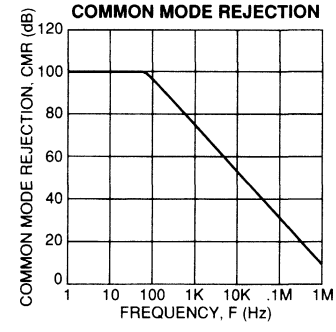
POWER RESPONSE



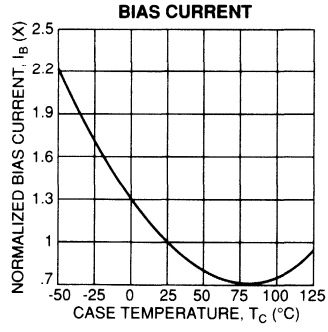
PULSE RESPONSE



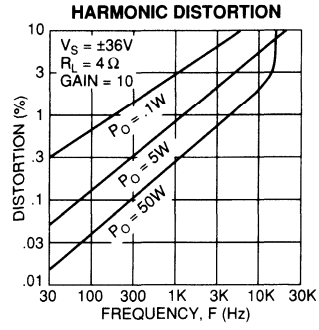
COMMON MODE REJECTION



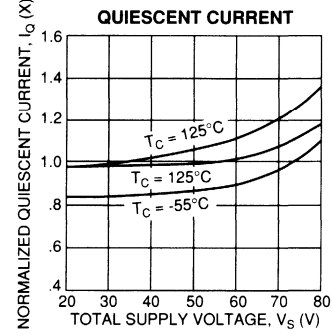
BIAS CURRENT



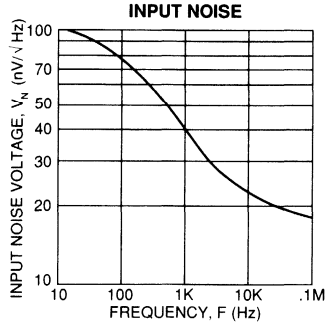
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



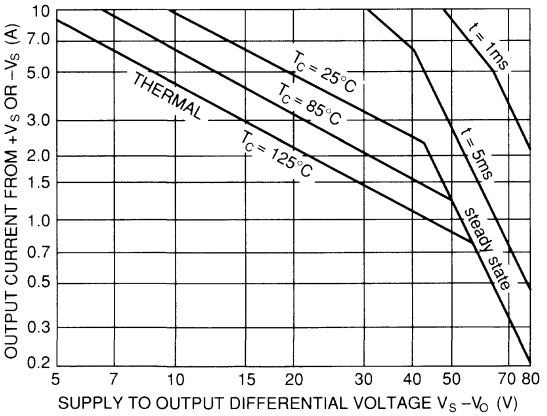
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.



The SOA curves combine the effect of of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximums are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
$\pm V_S$	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
40V	400µF	200µF	11mH	4.3mH
35V	800µF	400µF	20mH	5.0mH
30V	1,600µF	800µF	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C.

$\pm V_S$	SHORT TO $\pm V_S$ C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

CURRENT LIMIT

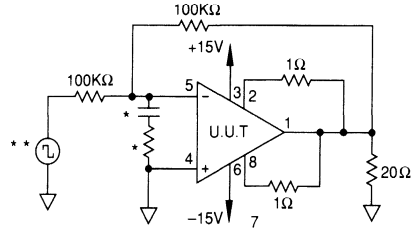
Proper operation requires the use of two current limit resistors, connected as shown in the external connection diagram. The minimum value for R_{CL} is .06 ohm, however for optimum reliability it should be set as high as possible. Refer to the "General Operating Considerations" section of the handbook for current limit adjust details.

TABLE 4 GROUP A INSPECTION

PA51M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		10	mA
1	Input offset voltage	V_{OS}	25°C	±34V	V_{IN} = 0, A_V = 100		±10	mV
1	Input offset voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±16	mV
1	Input offset voltage	V_{OS}	25°C	±40V	V_{IN} = 0, A_V = 100		±11.2	mV
1	Input bias current, +IN	$+I_B$	25°C	±34V	V_{IN} = 0		±40	nA
1	Input bias current, – IN	$-I_B$	25°C	±34V	V_{IN} = 0		±40	nA
1	Input offset current	I_{OS}	25°C	±34V	V_{IN} = 0		±10	nA
3	Quiescent current	I_Q	–55°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		10	mA
3	Input offset voltage	V_{OS}	–55°C	±34V	V_{IN} = 0, A_V = 100		±15.2	mV
3	Input offset voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±21.2	mV
3	Input offset voltage	V_{OS}	–55°C	±40V	V_{IN} = 0, A_V = 100		±16.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±34V	V_{IN} = 0		±72	nA
3	Input bias current, –IN	$-I_B$	–55°C	±34V	V_{IN} = 0		±72	nA
3	Input offset current	I_{OS}	–55°C	±34V	V_{IN} = 0		±26	nA
2	Quiescent current	I_Q	125°C	±34V	V_{IN} = 0, A_V = 100, R_{CL} = .1Ω		13	mA
2	Input offset voltage	V_{OS}	125°C	±34V	V_{IN} = 0, A_V = 100		±16.5	mV
2	Input offset voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±22.5	mV
2	Input offset voltage	V_{OS}	125°C	±40V	V_{IN} = 0, A_V = 100		±17.7	mV
2	Input bias current, +IN	$+I_B$	125°C	±34V	V_{IN} = 0		±80	nA
2	Input bias current, –IN	$-I_B$	125°C	±34V	V_{IN} = 0		±80	nA
2	Input offset current	I_{OS}	125°C	±34V	V_{IN} = 0		±30	nA
4	Output voltage, I_O =10A	V_O	25°C	±18V	R_L = 1Ω	10		V
4	Output voltage, I_O = 68mA	V_O	25°C	±40V	R_L = 500Ω	34		V
4	Output voltage, I_O = 4A	V_O	25°C	±30V	R_L = 6Ω	24		V
4	Current limits	I_{CL}	25°C	±16V	R_{CL} = 1Ω, R_{CL} = .1Ω	5	7.9	A
4	Stability/noise	E_N	25°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
4	Slew rate	SR	25°C	±34V	R_L = 500Ω	1.0	10	V/µs
4	Open loop gain	A_{OL}	25°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
4	Common-mode rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
6	Output voltage, I_O =10A	V_O	–55°C	±18V	R_L = 1Ω	10		V
6	Output voltage, I_O = 68mA	V_O	–55°C	±40V	R_L = 500Ω	34		V
6	Output voltage, I_O = 4A	V_O	–55°C	±30V	R_L = 6Ω	24		V
6	Stability/noise	E_N	–55°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
6	Slew rate	SR	–55°C	±34V	R_L = 500Ω	1.0	10	V/µs
6	Open loop gain	A_{OL}	–55°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
6	Common-mode rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB
5	Output voltage, I_O = 8A	V_O	125°C	±16V	R_L =1Ω	8		V
5	Output voltage, I_O = 68mA	V_O	125°C	±40V	R_L = 500Ω	34		V
5	Output voltage, I_O = 4A	V_O	125°C	±30V	R_L = 6Ω	24		V
5	Stability/noise	E_N	125°C	±34V	R_L = 500Ω, A_V = +1, C_L = 1.5nF		1	mV
5	Slew rate	SR	125°C	±34V	R_L =500Ω	1.0	10	V/µs
5	Open loop gain	A_{OL}	125°C	±34V	R_L = 500Ω, F = 10Hz	94		dB
5	Common-mode rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	70		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA61 • PA61A

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FEATURES

WIDE SUPPLY RANGE — ±10 to ±45V
HIGH OUTPUT CURRENT — ±10A Peak
LOW COST — Class "C" output stage
LOW QUIESCENT CURRENT — 3mA

APPLICATIONS

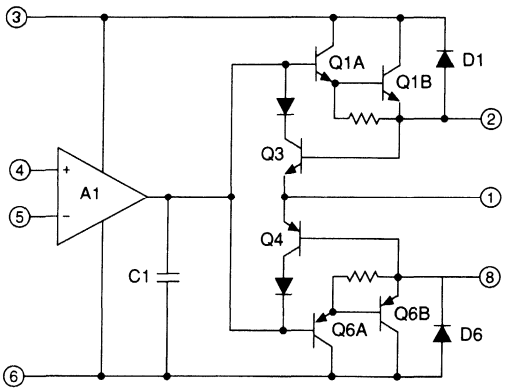
PROGRAMMABLE POWER SUPPLY
MOTOR/SYNCRO DRIVER
VALVE AND ACTUATOR CONTROL
DC OR AC POWER REGULATOR
FIXED FREQUENCY POWER OSCILLATOR

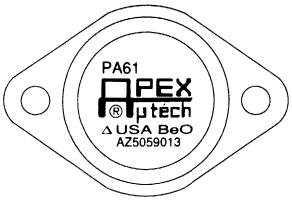
DESCRIPTION

The PA61 and PA61A are high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. Their complementary emitter follower output stage is protected against transient inductive kickback and optimized for low frequency applications where crossover distortion is not critical. These amplifiers are not recommended for audio, transducer or deflection coil drive circuits above 1kHz or when distortion is critical. The safe operating area (SOA) is fully specified and can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, mounting on a heatsink of proper rating is recommended.

This hybrid circuit utilizes thick film conductors, ceramic capacitors, and semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





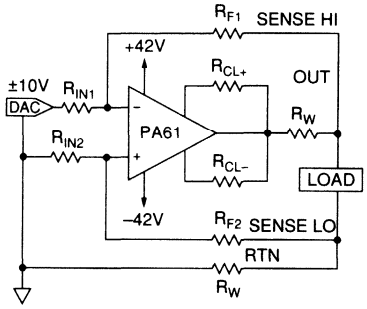


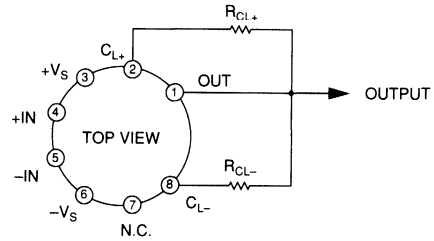
FIGURE 1. PROGRAMMABLE POWER SUPPLY WITH REMOTE SENSING

TYPICAL APPLICATION

Due to its high current drive capability, PA61 applications often utilize remote sensing to compensate IR drops in the wiring. The importance of remote sensing increases as accuracy requirements, output currents, and distance between amplifier and load go up. The circuit above shows wire resistance from the PA61 to the load and back to the local ground via the power return line. Without remote sensing, a 7.5A load current across only 0.05 ohm in each line would produce a 0.75 error at the load.

With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop. Therefore, as long as the Power Op Amp has the voltage drive capability to overcome the IR losses, accuracy remains the same. Application Note 7 presents a general discussion of PPS circuits.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	90V
OUTPUT CURRENT, within SOA	10A
POWER DISSIPATION, internal	97W
INPUT VOLTAGE, differential	$\pm V_S$–3V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder-10s	300°C
TEMPERATURE, junction[1]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

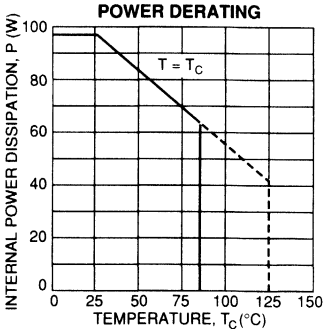
SPECIFICATIONS

		PA61			PA61A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±2	±6		±1	±3	mV
OFFSET VOLTAGE, vs. temperature	Specified temperature range		±10	±65		*	±40	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
OFFSET VOLTAGE, vs. power	T_C = 25°C		±20			*		µV/W
BIAS CURRENT, initial	T_C = 25°C		12	30		10	20	nA
BIAS CURRENT, vs. temperature	Specified temperature range		±50	±400		*	*	pA/°C
BIAS CURRENT, vs. supply	T_C = 25°C		±10			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		±12	±30		±5	±10	nA
OFFSET CURRENT, vs. temperature	Specified temperature range		±50			*		pA/°C
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		MΩ
INPUT CAPACITANCE	T_C = 25°C		3			*		pF
COMMON MODE VOLTAGE RANGE[3]	Specified temperature range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
COMMON MODE REJECTION, DC[3]	Specified temperature range	74	100		*	*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full temp. range, full load	96	108		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	T_C = 25°C, full load		1			*		MHz
POWER BANDWIDTH	T_C = 25°C, I_O = 8A, V_O = $40V_{PP}$	10	16		*	*		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = 10A	$\pm V_S$–7	$\pm V_S$–5		$\pm V_S$–6	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 4A	$\pm V_S$–6	$\pm V_S$–4		*	*		V
VOLTAGE SWING[3]	Full temp. range, I_O = 68mA	$\pm V_S$–5			*			V
CURRENT	T_C = 25°C	±10			*			A
SETTLING TIME to .1%	T_C = 25°C, 2V step		2			*		µs
SLEW RATE	T_C = 25°C, R_L = 6Ω	1.0	2.8		*	*		V/µs
CAPACITIVE LOAD, unit gain	Full temperature range			1.5			*	nF
CAPACITIVE LOAD, gain>4	Full temperature range			SOA			*	
POWER SUPPLY								
VOLTAGE	Full temperature range	±10	±32	±45	*	*	*	V
CURRENT, quiescent	T_C = 25°C		3	10		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	F > 60Hz		1.0	1.2		*	*	°C/W
RESISTANCE, DC, junction to case	F < 60Hz		1.5	1.8		*	*	°C/W
RESISTANCE, junction to air			30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specification	–25	25	+85	*	*	*	°C

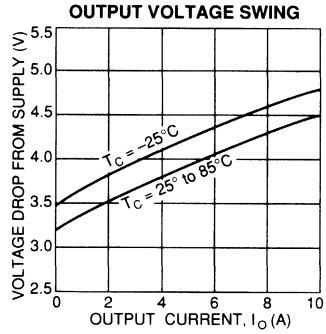
NOTES: * The specification of PA61A is identical to the specification for PA61 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

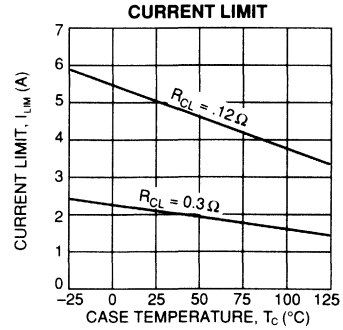
POWER DERATING



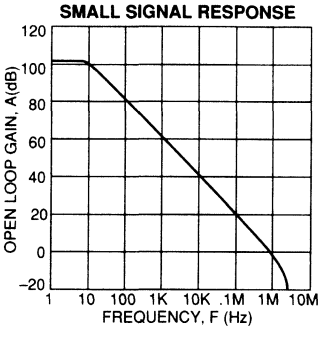
OUTPUT VOLTAGE SWING



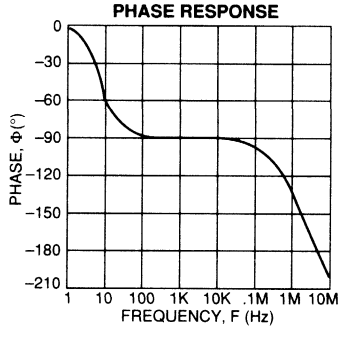
CURRENT LIMIT



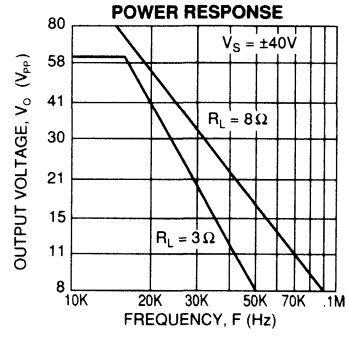
SMALL SIGNAL RESPONSE



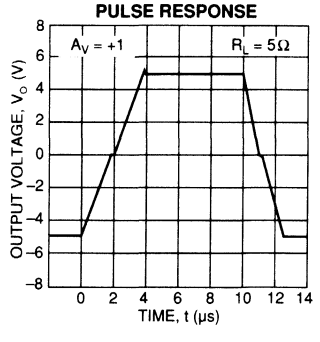
PHASE RESPONSE



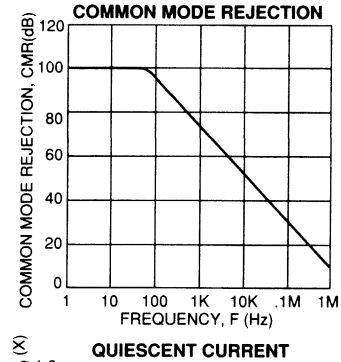
POWER RESPONSE



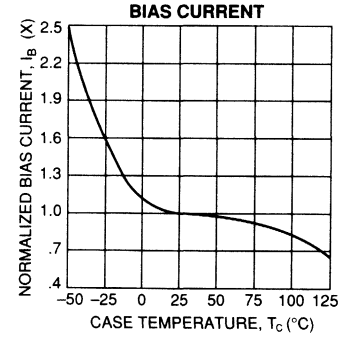
PULSE RESPONSE



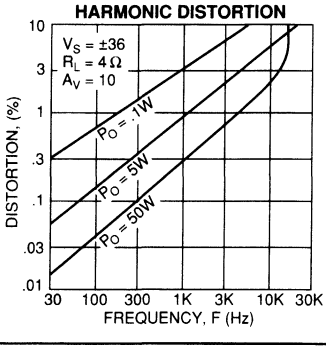
COMMON MODE REJECTION



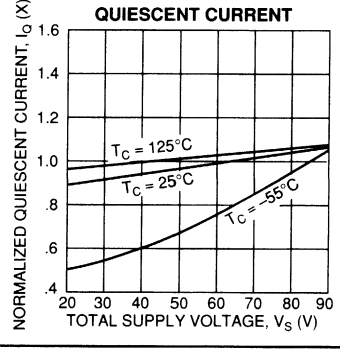
BIAS CURRENT



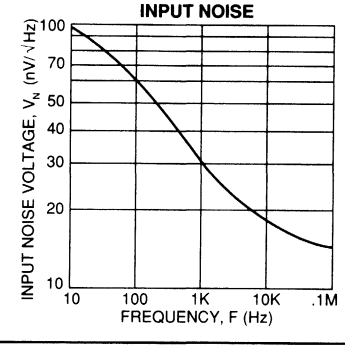
HARMONIC DISTORTION



QUIESCENT CURRENT



INPUT NOISE



GENERAL

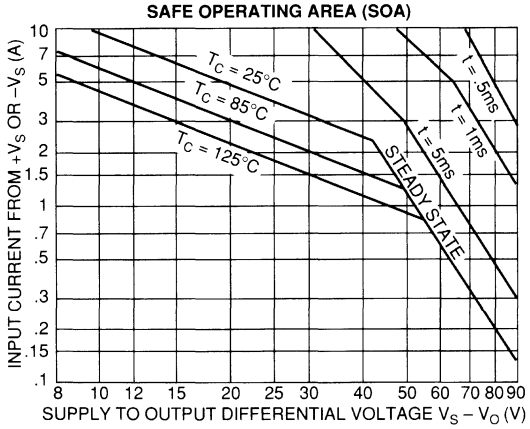
Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has 3 distinct limitations:

1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

SAFE OPERATING AREA (SOA)



The SOA curves combine the effect of all limits for this Power Op Amp. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. The following guidelines may save extensive analytical efforts.

1. Under transient conditions, capacitive and dynamic* inductive loads up to the following maximum are safe:

	CAPACITIVE LOAD		INDUCTIVE LOAD	
V_S	I_{LIM} = 5A	I_{LIM} = 10A	I_{LIM} = 5A	I_{LIM} = 10A
45V	200 F	150 F	8mH	2.8mH
40V	400 F	200 F	11mH	4.3mH
35V	800 F	400 F	20mH	5.0mH
30V	1600 F	800 F	35mH	6.2mH
25V	5.0mF	2.5mF	50mH	15mH
20V	10mF	5.0mF	400mH	20mH
15V	20mF	10mF	**	100mH

* If the inductive load is driven near steady state conditions, allowing the output voltage to drop more than 8V below the supply rail with I_{LIM} = 10A or 15V below the supply rail with I_{LIM} = 5A while the amplifier is current limiting, the inductor should be capacitively coupled or the current limit must be lowered to meet SOA criteria.

** Second breakdown effect imposes no limitation but thermal limitations must still be observed.

2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C=85°C.

$\pm V_S$	SHORT TO $V_S \pm$ C, L, OR EMF LOAD	SHORT TO COMMON
45V	0.1A	1.3A
40V	0.2A	1.5A
35V	0.3A	1.6A
30V	0.5A	2.0A
25V	1.2A	2.4A
20V	1.5A	3.0A
15V	2.0A	4.0A

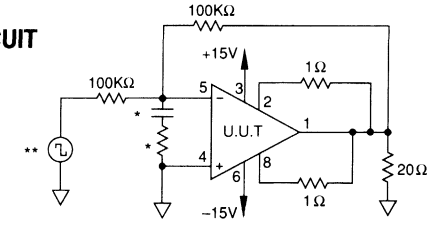
These simplified limits may be exceeded with further analysis using the operating conditions for a specific application.

3. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

TABLE 4 GROUP A INSPECTION
PA61M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±32V	V_{IN} = 0, A_V = 100		10	mA
1	Input Offset Voltage	V_{OS}	25°C	±32V	V_{IN} = 0, A_V = 100		±6	mV
1	Input Offset Voltage	V_{OS}	25°C	±10V	V_{IN} = 0, A_V = 100		±10.4	mV
1	Input Offset Voltage	V_{OS}	25°C	±45V	V_{IN} = 0, A_V = 100		±8.6	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Bias Current, –IN	$-I_B$	25°C	±32V	V_{IN} = 0		±30	nA
1	Input Offset Current	I_{OS}	25°C	±32V	V_{IN} = 0		±30	nA
3	Quiescent Current	I_Q	–55°C	±32V	V_{IN} = 0, A_V = 100		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±32V	V_{IN} = 0, A_V = 100		±11.2	mV
3	Input Offset Voltage	V_{OS}	–55°C	±10V	V_{IN} = 0, A_V = 100		±15.6	mV
3	Input Offset Voltage	V_{OS}	–55°C	±45V	V_{IN} = 0, A_V = 100		±13.8	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±32V	V_{IN} = 0		±115	nA
3	Input Offset Current	I_{OS}	–55°C	±32V	V_{IN} = 0		±115	nA
2	Quiescent Current	I_Q	125°C	±32V	V_{IN} = 0, A_V = 100		15	mA
2	Input Offset Voltage	V_{OS}	125°C	±32V	V_{IN} = 0, A_V = 100		±12.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±10V	V_{IN} = 0, A_V = 100		±16.9	mV
2	Input Offset Voltage	V_{OS}	125°C	±45V	V_{IN} = 0, A_V = 100		±15.1	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±32V	V_{IN} = 0		±70	nA
2	Input Offset Current	I_{OS}	125°C	±32V	V_{IN} = 0		±70	nA
4	Output Voltage, I_O = 10A	V_O	25°C	±17V	R_L = 1Ω	10		V
4	Output Voltage, I_O = 80mA	V_O	25°C	±45V	R_L = 500Ω	40		V
4	Output Voltage, I_O = 4A	V_O	25°C	± 30V	R_L = 6Ω	24		V
4	Current Limits	I_{CL}	25°C	±15V	R_L = 1Ω, R_{CL} = .1Ω	5	7.9	A
4	Stability/Noise	E_N	25°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±32V	R_L = 500Ω	1	10	V/µs
4	Open Loop Gain	A_{OL}	25°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
6	Output Voltage, I_O = 10A	V_O	–55°C	±17V	R_L = 1Ω	10		V
6	Output Voltage, I_O = 80mA	V_O	–55°C	±45V	R_L = 500Ω	40		V
6	Output Voltage, I_O = 4A	V_O	–55°C	±30V	R_L = 6Ω	24		V
6	Stability/Noise	E_N	–55°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±32V	R_L = 500Ω	1	10	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
6	CommonMode Rejection	CMR	–55°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB
5	Output Voltage, I_O = 8A	V_O	125°C	±15V	R_L = 1Ω	8		V
5	Output Voltage, I_O = 80mA	V_O	125°C	±45V	R_L = 500Ω	40		V
5	Output Voltage, I_O = 4A	V_O	125°C	±30V	R_L = 6Ω	24		V
5	Stability/Noise	E_N	125°C	±32V	R_L = 500Ω, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±32V	R_L = 500Ω	1	10	V/µs
5	Open Loop Gain	A_{OL}	125°C	±32V	R_L = 500Ω, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±15V	R_L = 500Ω, F = DC, V_{CM} = ±9V	74		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA81J • PA82J SERIES

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- **HIGH VOLTAGE OPERATION — ±150V (PA82J)**
- **HIGH OUTPUT CURRENT — ±30mA (PA81J)**
- **PROTECTED OUTPUT — Thermal Shutoff**
- **LOW BIAS CURRENT, LOW NOISE — FET Input**
- **SECOND SOURCEABLE — BB3581J, 82J**

APPLICATIONS

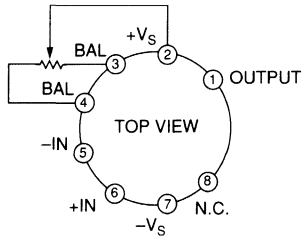
- **HIGH IMPEDANCE BUFFERS UP TO ±140V**
- **ELECTROSTATIC TRANSDUCER & DEFLECTION**
- **PROGRAMMABLE POWER SUPPLIES TO ±145V**
- **BIOCHEMISTRY STIMULATORS**
- **COMPUTER TO VACUUM TUBE INTERFACE**

DESCRIPTION

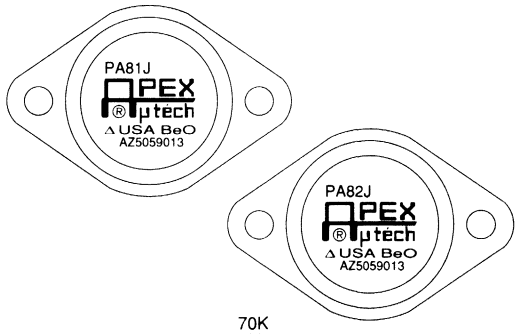
The PA80 series of high voltage operation amplifiers provides an extremely wide range of supply capability with two overlapping products. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode. As a result, these models offer outstanding common mode and power supply rejection. The output stage operates in the class A/B mode for best linearity. Internal phase compensation assures stability at all gain settings without external components. Fixed internal current limits protect these amplifiers against a short circuit to common at most supply voltages. For sustained high energy flyback, external fast recovery diodes should be used. A built-in thermal shutoff circuit prevents destructive overheating under most abnormal operating conditions. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

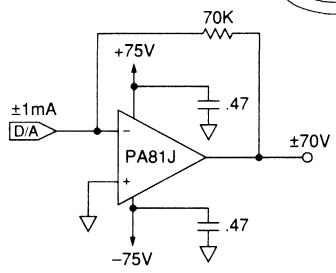
This hybrid circuit utilizes thick film resistors, ceramic capacitors and silicon semiconductors to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. The use of compressible isolation washers may void the warranty.

EXTERNAL CONNECTIONS



NOTE: Input offset trimpot optional.
Recommended value of 100KΩ .



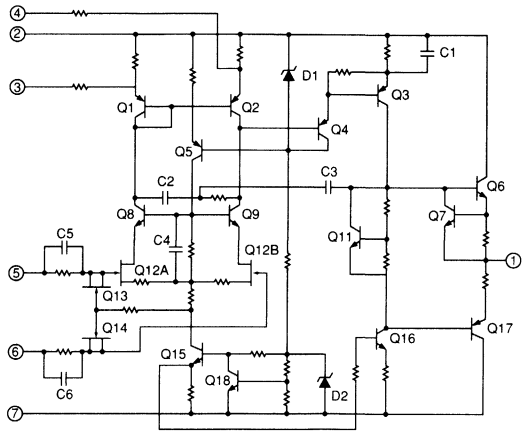


HIGH VOLTAGE PROGRAMMABLE POWER SUPPLY

TYPICAL APPLICATION

The PA81 and 70K ohm resistor form a current to voltage converter, accepting ±1mA from a 12 bit current output digital to analog converter. The power op amp contribution to the error budget is insignificant. At a case temperature of 70°C, the combination of voltage offset and bias errors amounts to less than 31ppm of full scale range. Incorporation of the optional offset trim can further reduce these errors to under 9ppm.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

	PA81J	PA82J
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V	300V
OUTPUT CURRENT, within SOA	Internally Limited	
POWER DISSIPATION, internal	11.5W	11.5W
INPUT VOLTAGE, differential	±150V	±300V
INPUT VOLTAGE, common mode	$\pm V_S$	$\pm V_S$
TEMPERATURE, pin solder - 10 sec	300°C	300°C
TEMPERATURE, junction	150°C	150°C
TEMPERATURE RANGE, storage	–65 to +125°C	–65 to +125°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C	–55 to +125°C

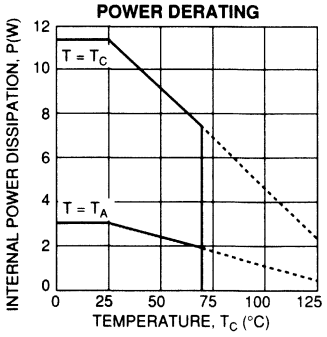
SPECIFICATIONS

		PA81J			PA82J			
PARAMETER	**TEST CONDITIONS**[2]	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		*	*	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	25		*	*	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		20			*		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		75			*		µV/√kh
BIAS CURRENT, initial	T_C = 25°C		5	50		*	*	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.2			*		pA/V
OFFSET CURRENT, initial	T_C = 25°C		2.5	50		*	*	pA
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = 25°C		10			*		pF
COMMON MODE VOLTAGE RANGE[2]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±20V		110			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	Full load	94	116		100	118		dB
UNITY GAIN BANDWIDTH	T_C = 25°C		5			*		MHz
POWER BANDWIDTH	T_C = 25°C, full load		60			30		kHz
PHASE MARGIN	Full temperature range		45			*		°
OUTPUT								
VOLTAGE SWING[2]	T_C = 25°C, I_{PK}	$\pm V_S$–5			*			V
CURRENT, peak	T_C = 25°C	30			15			mA
CURRENT, limit	T_C = 25°C		50			25		mA
SETTLING TIME to .1%	T_C = 25°C, 10V step		12			*		µs
SLEW RATE[4]	T_C = 25°C		20			*		V/µs
CAPACITIVE LOAD	A_V = 1		10			*		nF
POWER SUPPLY								
VOLTAGE	Full temperature range	±32	±75	±75	±70	±150	±150	V
CURRENT, quiescent	T_C = 25°C		6.5	8.5		6.5	8.5	mA
THERMAL								
RESISTANCE, AC, junction to case[3]	F > 60Hz		6			*		°C/W
RESISTANCE, DC, junction to case[3]	F < 60Hz		9	10		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, shutdown			150			*		°C
TEMPERATURE RANGE, case	Meets full range specification	0		70	*		*	°C

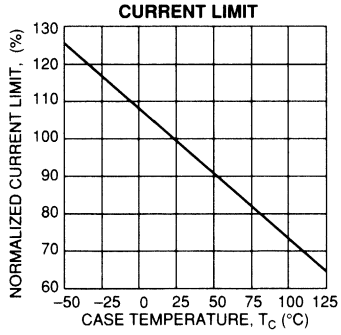
NOTES: * The specification of PA82J is identical to the specification for PA81J in applicable column to the left.
1. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
2. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
4. On the PA81J and PA82J, signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

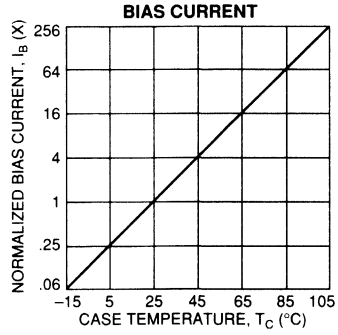
POWER DERATING



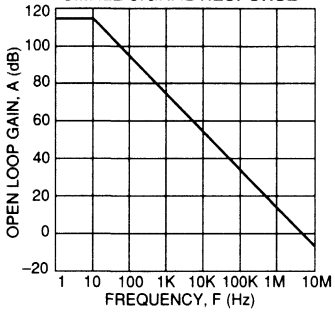
CURRENT LIMIT



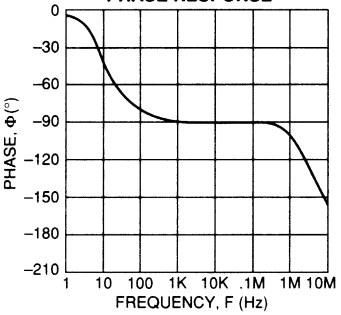
BIAS CURRENT



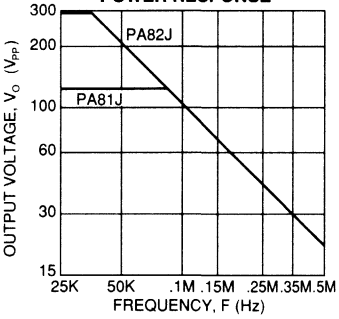
SMALL SIGNAL RESPONSE



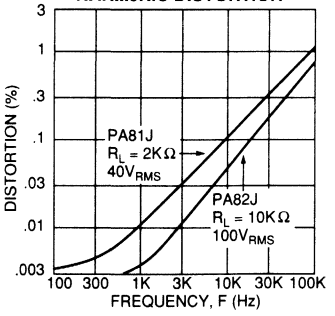
PHASE RESPONSE



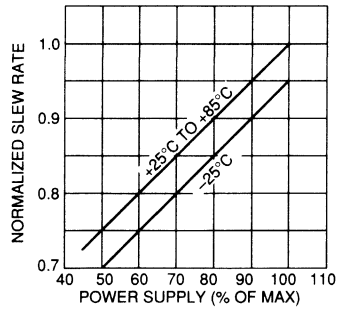
POWER RESPONSE



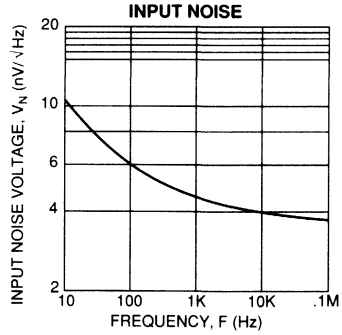
HARMONIC DISTORTION



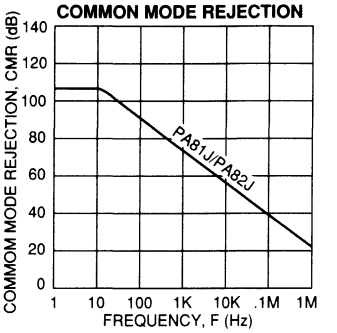
SLEW RATE



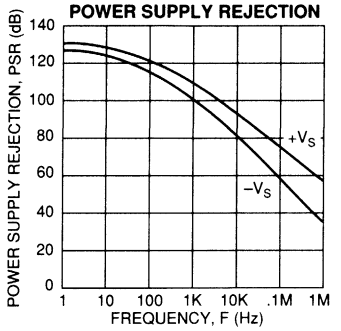
INPUT NOISE



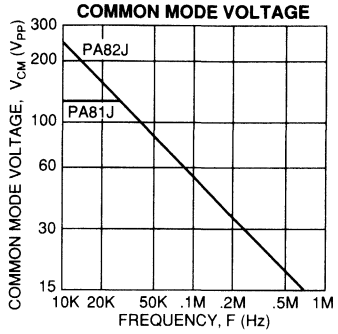
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

For the PA80J and PA81J, the combination of voltage capability and internal current limits mandate that the devices are safe for all combinations of supply voltage and load. On the PA82J, any load combination is safe up to a total supply of 250 volts. When total supply voltage equals 300 volts, the device will be safe if the output current is limited to 10 milliamps or less. This means that the PA82J used on supplies up to 125 volts will sustain a short to common or either supply without danger. When using supplies above ±125 volts, a short to one of the supplies will be potentially destructive. When using single supply above 250 volts, a short to common will be potentially destructive.

Safe supply voltages do not imply disregard for heatsinking. The thermal calculations and the use of a heatsink are required in many applications to maintain the case temperature within the specified operating range of 0 to 70°C. Exceeding this case temperature range can result in an inoperative circuit due to excessive input errors or activation of the thermal shutdown.

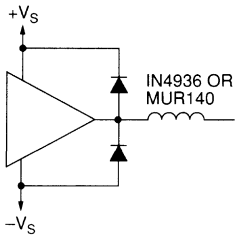


FIGURE 2.
PROTECTION,
INDUCTIVE LOAD

INDUCTIVE LOADS

Two external diodes as shown in Figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltage of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating, or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

THERMAL SHUTDOWN

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside the T_C = 25°C boundary). It is designed to protect against short-term conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy integrity, and reduce the reliability of the device.

SINGLE SUPPLY OPERATION

These amplifiers are suitable for operation from a single supply voltage. The operating requirements do however, impose the limitation that the input voltages do not approach closer than 10 volts to either supply rail. This is due to the operating voltage requirements of the current sources, the half-dynamic loads and the cascode stage. Refer to the simplified schematics.Thus, single supply operation requires the input signals to be biased at least 10 volts from either supply rail. Figure 3 illustrates one bias technique to achieve this.

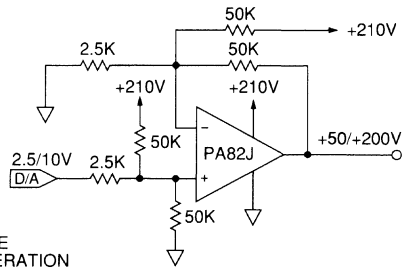


FIGURE 3.
TRUE SINGLE
SUPPLY OPERATION

Figure 4 illustrates a very common deviation from true single supply operation. The availibility of two supplies still allows ground (common) referenced signals, but also maximizes the high voltage capability of the unipolar output. This technique can utilize an existing low voltage system power supply and does not place large current demands on that supply. The 12 volt supply in this case must supply only the quiescent current of the PA81J, which is 8.5mA maximum. If the load is reactive or EMF producing, the low voltage supply must also be able to absorb the reverse currents generated by the load.

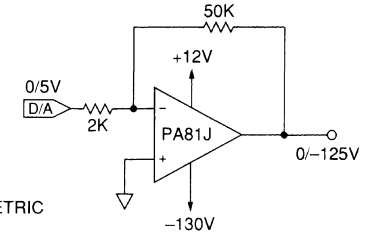


FIGURE 4.
NON-SYMMETRIC
SUPPLIES

POWER OPERATIONAL AMPLIFIERS
PA83 • PA83A

FEATURES

- **LOW BIAS CURRENT, LOW NOISE — FET Input**
- **PROTECTED OUTPUT — Thermal Shutoff**
- **FULLY PROTECTED INPUT — Up to ±150V**
- **WIDE SUPPLY RANGE — ±15V to ±150V**
- **SECOND SOURCEABLE — BB3583AM/JM**

APPLICATIONS

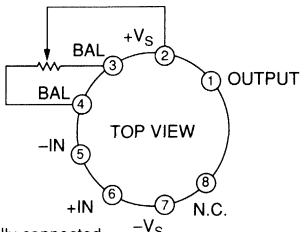
- **HIGH VOLTAGE INSTRUMENTATION**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PROGRAMMABLE POWER SUPPLIES UP TO 290V**
- **ANALOG SIMULATORS**

DESCRIPTION

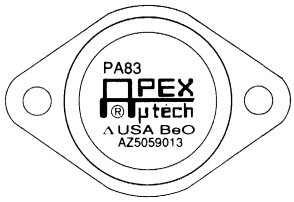
The PA83 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual (±) supply or 290V with a single supply. Its input stage is protected against transient and steady state overvoltages up to and including the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA83 features an unprecedented supply range and excellent supply rejection. The output stage is biased in the class A/B mode for linear operation. Internal phase compensation assures stability at all gain settings without need for external components. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 120V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

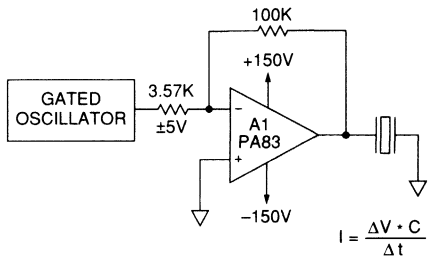
This hybrid circuit utilizes beryllia (BeO) substrates, thick (cermet) film resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible washers may void the warranty.

EXTERNAL CONNECTIONS



NOTES:
1. Pin 8 not internally connected.
2. Input offset trimpot optional. Recommended value 100KΩ.



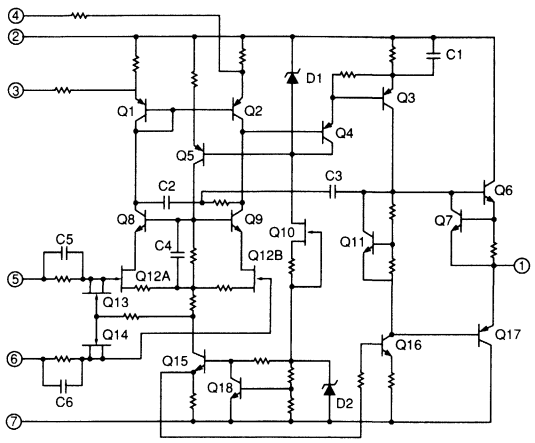


SIMPLE PIEZO ELECTRIC TRANSDUCER DRIVE

TYPICAL APPLICATION

While piezo electric transducers present a complex impedance, they are often primarily capacitive at useful frequencies. Due to this capacitance, the speed limitation for a given transducer/amplifier combination may well stem from limited current drive rather than power bandwidth restrictions. With its drive capability of 75mA, the PA83 can drive transducers having up to 2nF of capacitance at 40kHz at maximum output voltage. In the event the transducer may be subject to shock or vibration, flyback diodes, voltage clamps or other protection networks must be added to protect the amplifier from high voltages which may be generated.

EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[1]	17.5W
INPUT VOLTAGE, differential	±300V
INPUT VOLTAGE, common mode	±300V
TEMPERATURE, pin solder - 10s max (solder)	300°C
TEMPERATURE, junction	150°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

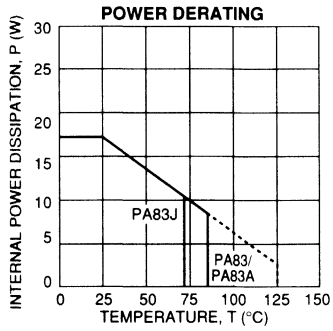
SPECIFICATIONS

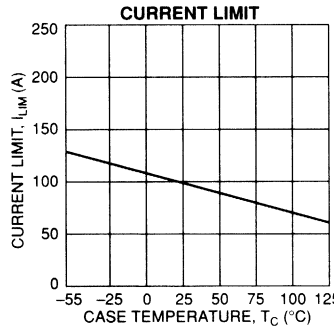
		PA83/PA83J			PA83A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV/√kh
BIAS CURRENT, initial[3]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[3]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	Full temperature range		6			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S$–10			*			V
COMMON MODE REJECTION, DC	Full temperature range		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = 2KΩ	96	116		*	*		dB
UNITY GAIN CROSSOVER FREQ.	T_C = 25°C, R_L = 2KΩ		5		3	*		MHz
POWER BANDWIDTH	T_C = 25°C, R_L = 10KΩ		60		40	*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4], full load	Full temp. range, I_O = 75mA	$\pm V_S$–10	$\pm V_S$–5		*	*		V
VOLTAGE SWING[4]	Full temp. range, I_O = 15mA	$\pm V_S$–5	$\pm V_S$–3		*	*		V
CURRENT, peak	T_C = 25°C	75			*			mA
CURRENT, short circuit	T_C = 25°C		100			*		mA
SLEW RATE[6]	T_C = 25°C, R_L = 2KΩ	20	30		*	*		V/µs
CAPACITIVE LOAD, unity gain	Full temperature range			10			*	nF
CAPACITIVE LOAD, gain > 4	Full temperature range			SOA			*	µF
SETTLING TIME to .1%	T_C = 25°C, R_L = 2KΩ, 10V step		12			*		µs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15	±150	±150	*	*	*	V
CURRENT, quiescent	T_C = 25°C		6	8.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	F > 60Hz		3.8			*		°C/W
RESISTANCE, DC, junction to case	F < 60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air			30			*		°C/W
TEMP. RANGE, case (PA83/PA83A)	Meets full range specification	–25		+85	*		*	°C
TEMP. RANGE, case (PA83J)	Meets full range specification	0		70				°C

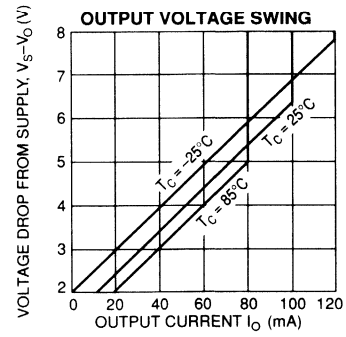
NOTES: * The specification of PA83A is identical to the specification for PA83 in applicable column to the left.

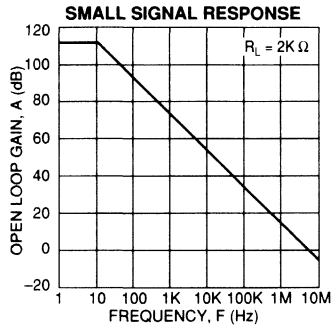
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all tests is the TYP rating, unless otherwise noted as a test condition.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.

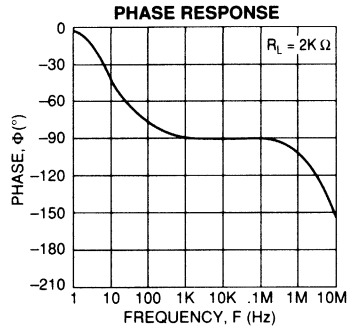
CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

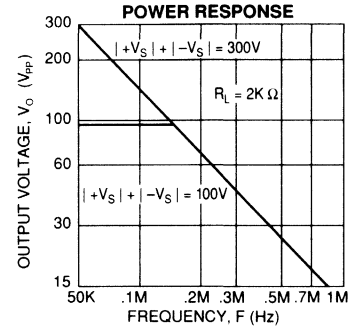

POWER DERATING
INTERNAL POWER DISSIPATION, P (W)
30
25
20
15
10
5
0
PA83J
PA83/
PA83A
0 25 50 75 100 125 150
TEMPERATURE, T (°C)

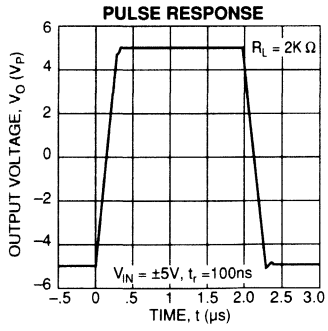

CURRENT LIMIT
CURRENT LIMIT, I_{LIM} (A)
250
200
150
100
50
0
−55 −25 0 25 50 75 100 125
CASE TEMPERATURE, T_C (°C)

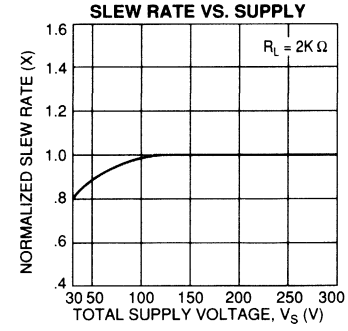

OUTPUT VOLTAGE SWING
VOLTAGE DROP FROM SUPPLY, V_S–V_O (V)
8
7
6
5
4
3
2
T_C = −25°C
T_C = 25°C
T_C = 85°C
0 20 40 60 80 100 120
OUTPUT CURRENT I_O (mA)

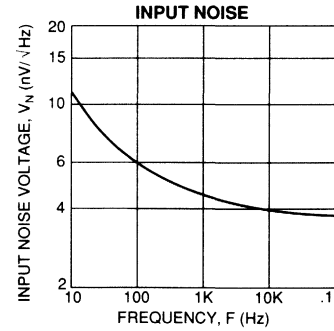

SMALL SIGNAL RESPONSE
OPEN LOOP GAIN, A (dB)
120
100
80
60
40
20
0
−20
R_L = 2K Ω
1 10 100 1K 10K 100K 1M 10M
FREQUENCY, F (Hz)

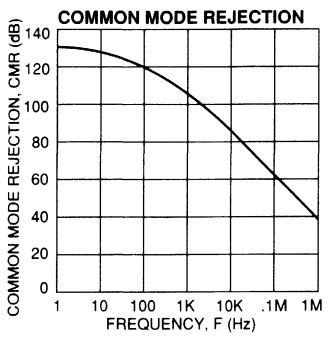

PHASE RESPONSE
PHASE, Φ (°)
0
−30
−60
−90
−120
−150
−180
−210
R_L = 2K Ω
1 10 100 1K 10K .1M 1M 10M
FREQUENCY, F (Hz)

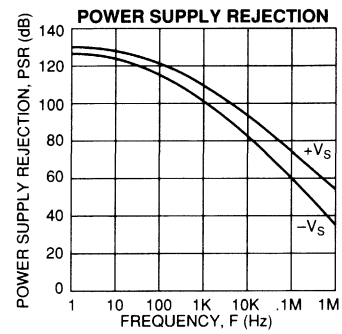

POWER RESPONSE
OUTPUT VOLTAGE, V_O (V_{PP})
300
200
100
60
30
15
| +V_S | + | −V_S | = 300V
R_L = 2K Ω
| +V_S | + | −V_S | = 100V
50K .1M .2M .3M .5M .7M 1M
FREQUENCY, F (Hz)

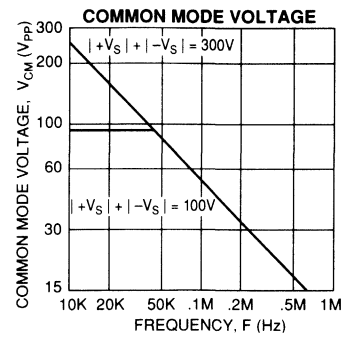

PULSE RESPONSE
OUTPUT VOLTAGE, V_O (V_P)
6
4
2
0
−2
−4
−6
R_L = 2K Ω
V_{IN} = ±5V, t_r = 100ns
−.5 0 .5 1 1.5 2.0 2.5 3.0
TIME, t (µs)


SLEW RATE VS. SUPPLY
NORMALIZED SLEW RATE (X)
1.6
1.4
1.2
1.0
.8
.6
.4
R_L = 2K Ω
30 50 100 150 200 250 300
TOTAL SUPPLY VOLTAGE, V_S (V)


INPUT NOISE
INPUT NOISE VOLTAGE, V_N (nV/√Hz)
20
15
10
6
4
2
10 100 1K 10K .1M
FREQUENCY, F (Hz)


COMMON MODE REJECTION
COMMON MODE REJECTION, CMR (dB)
140
120
100
80
60
40
20
0
1 10 100 1K 10K .1M 1M
FREQUENCY, F (Hz)


POWER SUPPLY REJECTION
POWER SUPPLY REJECTION, PSR (dB)
140
120
100
80
60
40
20
0
+V_S
−V_S
1 10 100 1K 10K .1M 1M
FREQUENCY, F (Hz)


COMMON MODE VOLTAGE
COMMON MODE VOLTAGE, V_{CM} (V_{PP})
300
200
100
60
30
15
| +V_S | + | −V_S | = 300V
| +V_S | + | −V_S | = 100V
10K 20K 50K .1M .2M .5M 1M
FREQUENCY, F (Hz)

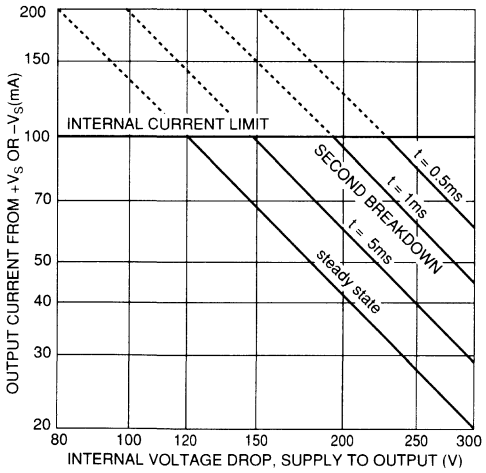
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage amplifier has two distinct limitations.

1. The internal current limit, which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceed specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_S$	C(MAX)	L(MAX)
150V	.7 F	1.5H
125V	2.0µF	2.5H
100V	5.µF	6.0H
75V	60µF	30H
50V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to 120V or single supplies up to 120V.
3. Short circuits to the supply rails are safe with total supply voltages up to 120V, e.g. ±60V.
4. The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperature during temporary fault conditions.

Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, destroy signal integrity, and reduce the reliability of the device.

INDUCTIVE LOADS

Two external diodes as shown in Figure 1, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

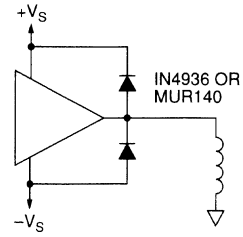


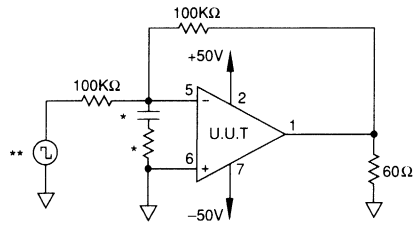
FIGURE 1. PROTECTION, INDUCTIVE LOAD

TABLE 4 GROUP A INSPECTION

PA83M

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		8.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0, A_V = 100		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		10	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V =100		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0, A_V = 100		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		10	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0, A_V = 100		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 75mA	V_O	25°C	±85V	R_L = 1K	75		V
4	Output Voltage, I_O = 29mA	V_O	25°C	±150V	R_L = 5K	145		V
4	Current Limits	I_{CL}	25°C	±30V	R_L = 100Ω	75	125	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K	20	60	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5K, F = 10Hz	96		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 40mA	V_O	–55°C	±45V	R_L = 1K	40		V
6	Output Voltage, I_O = 29mA	V_O	–55°C	±150V	R_L = 5K	145		V
6	Stability/Noise	E_N	–55°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±150V	R_L = 5K	20	60	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	R_L = 5K, F = 10Hz	96		dB
6	Common Mode Rejection	CMR	–55°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 40mA	V_O	125°C	±45V	R_L = 1K	40		V
5	Output Voltage, I_O = 29mA	V_O	125°C	±150V	R_L = 5K	145		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K	20	60	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	96		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5K, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA84 • PA84A • PA84S

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FEATURES

- **HIGH SLEW RATE — 200V/μs**
- **FAST SETTLING TIME — .1% in 1μs (PA84S)**
- **FULLY PROTECTED INPUT — Up to ±150v**
- **LOW BIAS CURRENT, LOW NOISE — FET Input**
- **WIDE SUPPLY RANGE — ±15V to ±150V**
- **SECOND SOURCEABLE — BB3584JM**

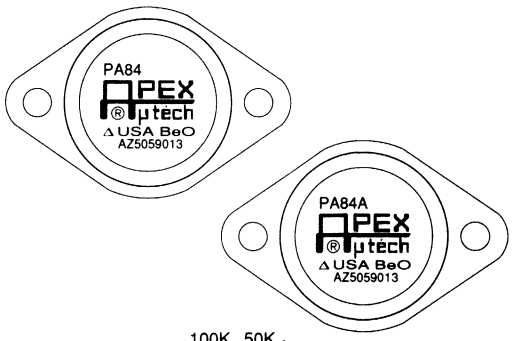
APPLICATIONS

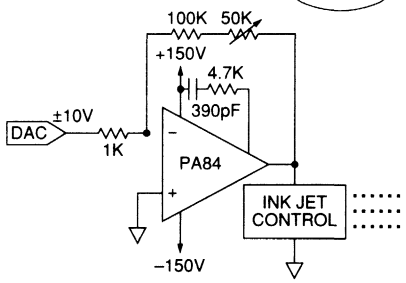
- **HIGH VOLTAGE INSTRUMENTATION**
- **ELECTROSTATIC TRANSDUCERS & DEFLECTION**
- **PROGRAMMABLE POWER SUPPLIES UP TO 290V**
- **ANALOG SIMULATORS**

DESCRIPTION

The PA84 is a high voltage operational amplifier designed for output voltage swings up to ±145V with a dual supply or 290V with a single supply. Two versions are available. The new PA84S, fast settling amplifier can absorb differential input overvoltages up to ±50V while the established PA84 and PA84A can handle differential input overvoltages of up to ±300V. Both versions are protected against common mode transients and overvoltages up to the supply rails. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a zener diode fed by a FET constant current source. As a result, the PA84 features an unprecedented supply range and excellent supply rejection. The output stage is biased-on for linear operation. External phase compensation allows for user flexibility in obtaining the maximum slew rate. Fixed current limits protect these amplifiers against shorts to common at supply voltages up to 150V. For operation into inductive loads, two external flyback pulse protection diodes are recommended. A built-in thermal shutoff circuit prevents destructive overheating. However, a heatsink may be necessary to maintain the proper case temperature under normal operating conditions.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

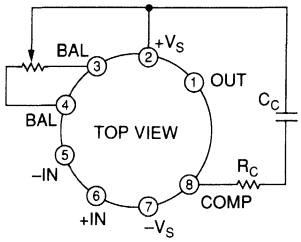




TYPICAL APPLICATION

The PA84 is ideally suited to driving ink jet control units (often a piezo electric device) which require precise pulse shape control to deposit crisp clear date or lot code information on product containers. The external compensation network has been optimized to match the gain setting of the circuit and the complex impedance of the ink jet control unit. The combination of speed and high voltage capabilities of the PA84 form ink droplets of uniform volume at high production rates to enhance the value of the printer.

EXTERNAL CONNECTION

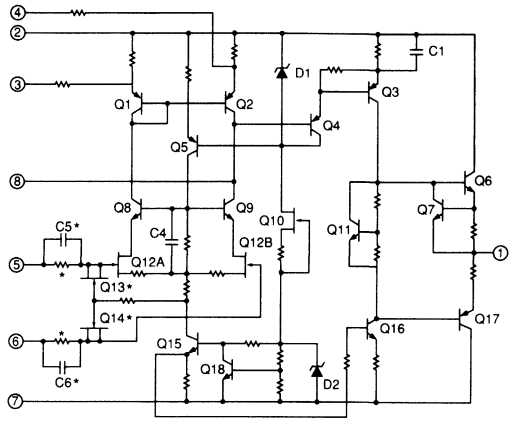


PHASE COMPENSATION

GAIN	C_C	R_C
1	10nF	200Ω
10	500pF	2KΩ
100	50pF	20KΩ
1000	none	none

NOTES:
1. Phase Compensation required for safe operation.
2. Input offset trimpot optional. Recommended value 100KΩ.

EQUIVALENT SCHEMATIC



* NOTE: Not used for PA84S

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	Internally Limited
POWER DISSIPATION, internal at T_C = 25°C[2]	17.5W
INPUT VOLTAGE, differential PA84/PA84A[1]	±300V
INPUT VOLTAGE, differential PA84S	±50V
INPUT VOLTAGE, common mode[1]	$\pm V_S$
TEMPERATURE, pins for 10s max (solder)	300°C
TEMPERATURE, junction[2]	200°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

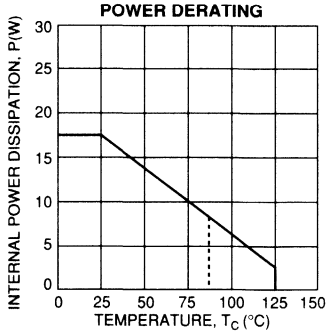
		PA84/PA84S			PA84A			
PARAMETER	**TEST CONDITIONS[3]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial	T_C = 25°C		±1.5	±3		±.5	±1	mV
OFFSET VOLTAGE, vs. temperature	T_C = –25° to +85°C		±10	±25		±5	±10	µV/°C
OFFSET VOLTAGE, vs. supply	T_C = 25°C		±.5			±.2		µV/V
OFFSET VOLTAGE, vs. time	T_C = 25°C		±75			*		µV√kh
BIAS CURRENT, initial[4]	T_C = 25°C		5	50		3	10	pA
BIAS CURRENT, vs. supply	T_C = 25°C		.01			*		pA/V
OFFSET CURRENT, initial[4]	T_C = 25°C		±2.5	±50		±1.5	±10	pA
OFFSET CURRENT, vs. supply	T_C = 25°C		±.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		10^{11}			*		Ω
INPUT CAPACITANCE	T_C = –25° to +85°C		6			*		pF
COMMON MODE VOLTAGE RANGE[5]	T_C = –25° to +85°C	$\pm V_S$–10	$\pm V_S$–8.5		*	*		V
COMMON MODE REJECTION, DC	T_C = –25° to +85°C		130			*		dB
GAIN								
OPEN LOOP GAIN at 10Hz	T_C = 25°C, R_L = ∞		120			*		dB
OPEN LOOP GAIN at 10Hz.	T_C = 25°C, R_L = 3.5KΩ	100	118		*	*		dB
GAIN BANDWIDTH PRODUCT@ 1MHz	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		75			*		MHz
POWER BANDWIDTH, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		250		180	*		kHz
POWER BANDWIDTH, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		120			*		kHz
OUTPUT								
VOLTAGE SWING[5]	T_C = 25°C, I_O = ±40mA	$\pm V_S$–7	$\pm V_S$–3		*	*		V
VOLTAGE SWING[5]	T_C = –25° to +85°C, I_O = ±15mA	$\pm V_S$–5	$\pm V_S$–2		*	*		V
CURRENT, peak	T_C = 25°C	40			*			mA
CURRENT, short circuit	T_C = 25°C		50			*		mA
SLEW RATE, high gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 20KΩ		200		150	*		V/µs
SLEW RATE, low gain	T_C = 25°C, R_L = 3.5KΩ, R_C = 2KΩ		125			*		V/µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84S**		2					µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step **ONLY**		1					µs
SETTLING TIME .01% at gain = 100	T_C = 25°C, R_L = 3.5KΩ **PA84/84A**		20			20		µs
SETTLING TIME .1% at gain = 100	R_C = 20KΩ, V_{IN} = 2V step		12			12		µs
POWER SUPPLY								
VOLTAGE	T_C = –55°C to +125°C	±15		±150	*		*	V
CURRENT, quiescent	T_C = 25°C		5.5	7.5		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[6]	T_C = –55°C to +125°C, F > 60Hz		3.8			*		°C/W
RESISTANCE, DC, junction to case	T_C = –55°C to +125°C, F < 60Hz		6	6.5		*	*	°C/W
RESISTANCE, case to air	T_C = –55°C to +125°C		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA84A is identical to the specification for PA84/PA84S in applicable column to the left.

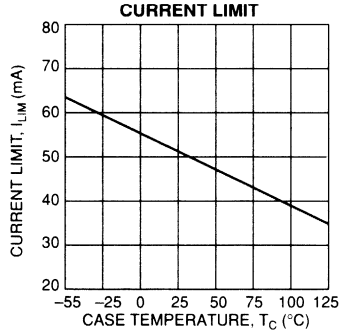
1. Signal slew rates at pins 5 and 6 must be limited to less than 1V/ns to avoid damage. When faster waveforms are unavoidable, resistors in series with those pins, limiting current to 150mA will protect the amplifier from damage.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. The power supply voltage for all tests is ±150V, unless otherwise noted as a test condition.
4. Doubles for every 10°C of temperature increase.
5. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
6. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

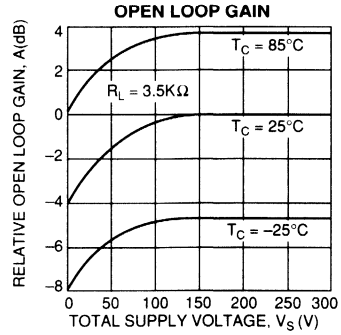
POWER DERATING



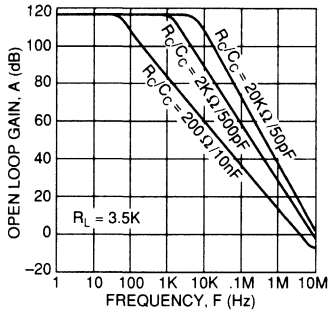
CURRENT LIMIT



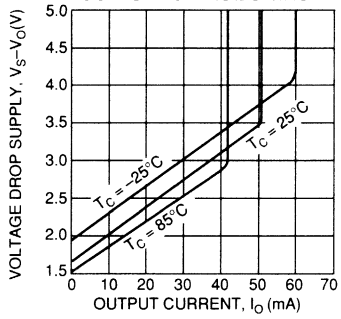
OPEN LOOP GAIN



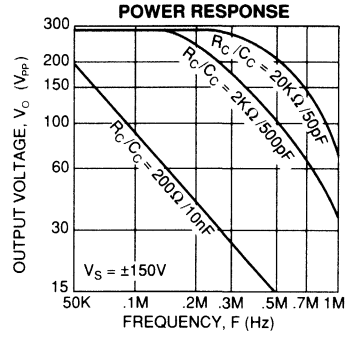
SMALL SIGNAL RESPONSE



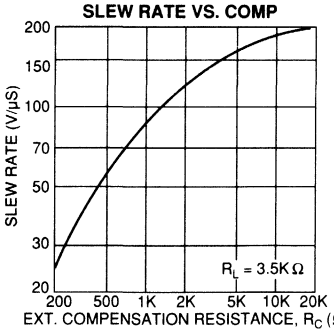
OUTPUT VOLTAGE SWING



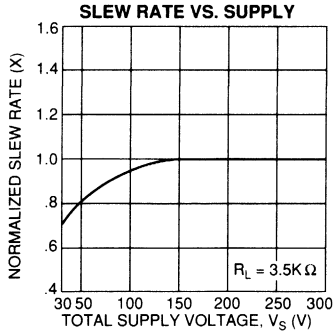
POWER RESPONSE



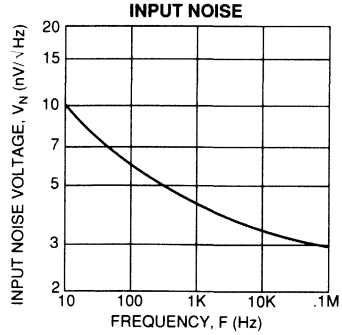
SLEW RATE VS. COMP



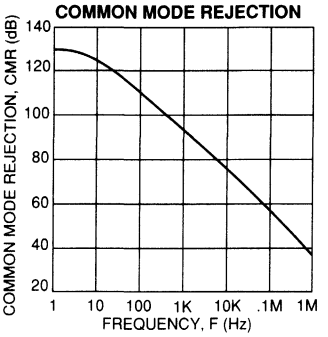
SLEW RATE VS. SUPPLY



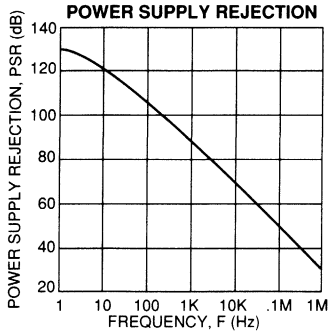
INPUT NOISE



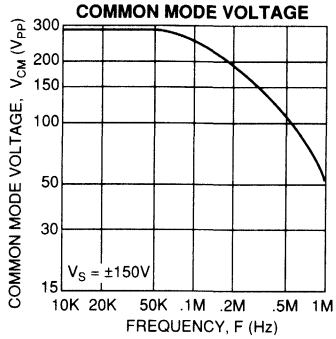
COMMON MODE REJECTION



POWER SUPPLY REJECTION



COMMON MODE VOLTAGE



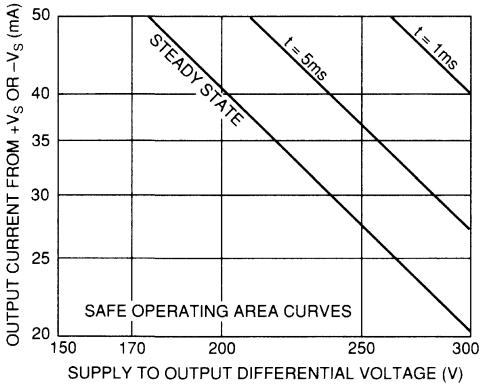
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this high voltage operational amplifier has two output limitations:

1. The internal current limit which limits maximum available output current.
2. The second breakdown effect, which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.



The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads. However, the following guidelines may save extensive analytical efforts:

1. The following capacitive and inductive loads are safe:

$\pm V_S$	C(MAX)	L(MAX)
150V	1.2μF	.7H
125V	6.0μF	25H
100V	12μF	90H
75V	ALL	ALL

2. Short circuits to ground are safe with dual supplies up to ±150V or single supplies up to 150V.
3. Short circuits to the supply rails are safe with total supply voltages up to 150V (i.e. ±75V).

THERMAL SHUTDOWN PROTECTION

The thermal protection circuit shuts off the amplifier when the substrate temperature exceeds approximately 150°C. This allows heatsink selection to be based on normal operating conditions while protecting the amplifier against excessive junction temperatures during temporary fault conditions.

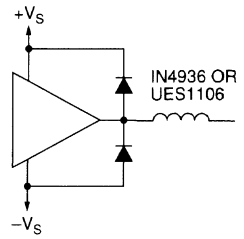
Thermal protection is a fairly slow-acting circuit and therefore does not protect the amplifier against transient SOA violations (areas outside of the T_C = 25°C boundary). It is designed to protect against short-term fault conditions that result in high power dissipation within the amplifier. If the conditions that cause thermal shutdown are not removed, the amplifier will oscillate in and out of shutdown. This will result in high peak power stresses, will destroy signal integrity, and reduce the reliability of the device.

OUTPUT PROTECTION

Two external diodes as shown in Figure 2, are required to protect these amplifiers against flyback (kickback) pulses exceeding the supply voltages of the amplifier when driving inductive loads. For component selection, these external diodes must be very quick, such as ultra fast recovery diodes with no more than 200 nanoseconds of reverse recovery time. The diode will turn on to divert the flyback energy into the supply rails thus protecting the output transistors from destruction due to reverse bias.

A note of caution about the supply. The energy of the flyback pulse must be absorbed by the power supply. As a result, a transient will be superimposed on the supply voltage, the magnitude of the transient being a function of its transient impedance and current sinking capability. If the supply voltage plus transient exceeds the maximum supply rating or if the AC impedance of the supply is unknown, it is best to clamp the output and the supply with a zener diode to absorb the transient.

FIGURE 1. PROTECTIVE, INDUCTIVE LOAD



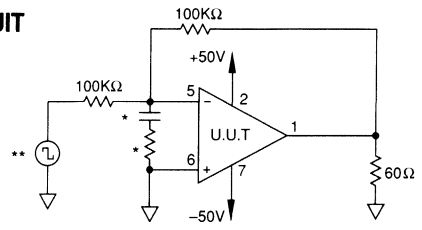
STABILITY

Due to its large bandwidth the PA84 is more likely to oscillate than lower bandwidth Power Operational Amplifiers such as the PA83 or PA08. To prevent oscillations, a reasonable phase margin must be maintained by:

1. Selection of the proper phase compensation capacitor and resistor. Use the values given in the table under external connections and interpolate if necessary. The phase margin can be increased by using a large capacitor and a smaller resistor than the slew rate optimized values listed in the table. The compensation capacitor may be connected to common (in lieu of $+V_S$) if the positive supply is properly bypassed to common. Because the voltage at pin 8 is only a few volts below the positive supply, this ground connection requires the use of a high voltage capacitor.
2. Keeping the external sumpoint stray capacitance to ground at a minimum and the sumpoint load resistance (input and feedback resistors in parallel) below 500Ω. Larger sumpoint load resistance can be used with increased phase compensation (see 1 above).
3. Connecting the amplifier case to a local AC common thus preventing it from acting as an antenna.

SG	PARAMETER	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent Current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		7.5	mA
1	Input Offset Voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		3	mV
1	Input Offset Voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		5.7	mV
1	Input Bias Current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0, A_V = 100		50	pA
1	Input Bias Current, –IN	$-I_B$	25°C	±150V	V_{IN} = 0		50	pA
1	Input Offset Current	I_{OS}	25°C	±150V	V_{IN} = 0		50	pA
3	Quiescent Current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
3	Input Offset Voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		5	mV
3	Input Offset Voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		7.7	mV
3	Input Bias Current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0, A_V = 100		50	pA
3	Input BiasCurrent, –IN	$-I_B$	–55°C	±150V	V_{IN} = 0		50	pA
3	Input Offset Current	I_{OS}	–55°C	±150V	V_{IN} = 0		50	pA
2	Quiescent Current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		9.5	mA
2	Input Offset Voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		5.5	mV
2	Input Offset Voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		8.2	mV
2	Input Bias Current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0, A_V = 100		10	nA
2	Input Bias Current, –IN	$-I_B$	125°C	±150V	V_{IN} = 0		10	nA
2	Input Offset Current	I_{OS}	125°C	±150V	V_{IN} = 0		10	nA
4	Output Voltage, I_O = 40mA	V_O	25°C	±47V	R_L = 1K	40		V
4	Output Voltage, I_O = 28.6mA	V_O	25°C	±150V	R_L = 5K	143		V
4	Output Voltage, I_O = 15mA	V_O	25°C	± 80V	R_L = 5K	75		V
4	Current Limits	I_{CL}	25°C	± 150V	R_L = 100Ω	36	70	mA
4	Stability/Noise	E_N	25°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
4	Slew Rate	SR	25°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
4	Open Loop Gain	A_{OL}	25°C	±150V	R_L = 5k, F = 10Hz	100		dB
4	Common Mode Rejection	CMR	25°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
6	Output Voltage, I_O = 40mA	V_O	–55°C	±47V	R_L = 1K	40		V
6	Output Voltage, I_O = 28.6mA	V_O	–55°C	±50V	R_L = 5K	143		V
6	Output Voltage, I_O = 15mA	V_O	–55°C	±80V	R_L = 5K	75		V
6	Stability/Noise	E_N	–55°C	±150V	R_L = 5K, A_V = 1, C_L = 10nF		1	mV
6	Slew Rate	SR	–55°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
6	Open Loop Gain	A_{OL}	–55°C	±150V	R_L = 5K, F = 10Hz	100		dB
6	Common Mode Rejection	CMR	-55°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB
5	Output Voltage, I_O = 30mA	V_O	125°C	±37V	R_L = 1K	30		V
5	Output Voltage, I_O = 28.6mA	V_O	125°C	±150V	R_L = 5K	143		V
5	Output Voltage, I_O = 15mA	V_O	125°C	±80V	R_L = 5K	75		V
5	Stability/Noise	E_N	125°C	±150V	R_L = 5 , A_V = 1, C_L = 10nF		1	mV
5	Slew Rate	SR	125°C	±150V	R_L = 5K, C_C = 50pF	100	600	V/µs
5	Open Loop Gain	A_{OL}	125°C	±150V	R_L = 5K, F = 10Hz	100		dB
5	Common Mode Rejection	CMR	125°C	±32.5V	R_L = 5k, F = DC, V_{CM} = ±22.5V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

NOTES:

PA85 • PA85A

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FEATURES

- HIGH VOLTAGE — 450V
- HIGH SLEW RATE — 1000V/μS
- HIGH OUTPUT CURRENT — 200mA

APPLICATIONS

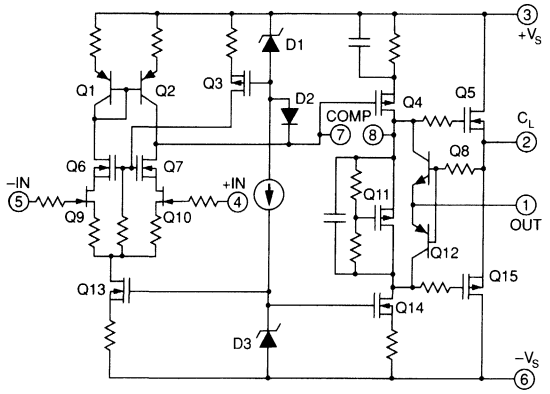
- HIGH VOLTAGE INSTRUMENTATION
- PIEZO TRANSDUCER EXCITATION
- PROGRAMMABLE POWER SUPPLIES UP TO 440V
- ELECTROSTATIC TRANSDUCERS & DEFLECTION

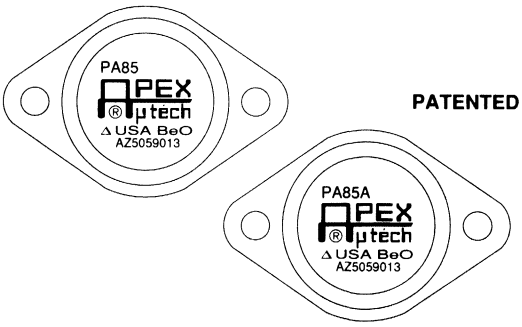
DESCRIPTION

The PA85 is a high voltage, high power bandwidth MOSFET operational amplifier designed for output currents up to 200mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA85 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and silicon semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC

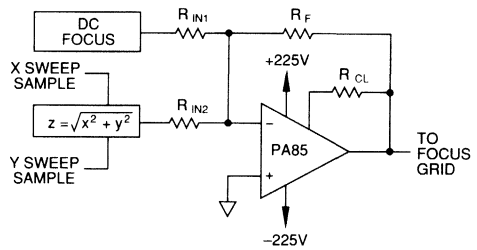




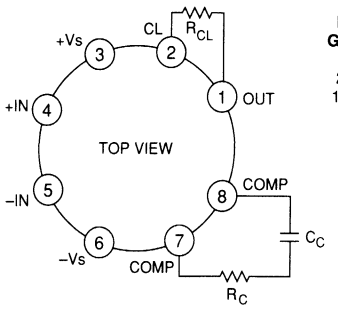
PATENTED

TYPICAL APPLICATION

Dynamic focusing is the active correction of focusing voltage as a beam traverses the face of a CRT. This is necessary in high resolution flat face monitors since the distance between cathode and screen varies as the beam moves from the center of the screen to the edges. PA85 lends itself well to this function since it can be connected as a summing amplifier with inputs from the nominal focus potential and the dynamic correction. The nominal might be derived from a potentiometer, or perhaps automatic focusing circuitry might be used to generate this potential. The dynamic correction is generated from the sweep voltages by calculating the distance of the beam from the center of the display.



EXTERNAL CONNECTIONS



PHASE COMPENSATION

Gain	C_C	R_C
1	68pF	100Ω
20	10pF	330Ω
100	3.3pF	0Ω

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, continuous within SOA	200mA
POWER DISSIPATION, continuous @ T_C = 25°C	40W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

		PA85			PA85A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			3	10		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			10	100		3	30	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S$–12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 10pf		1			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 3.3pf		100			*		MHz
POWER BANDWIDTH	C_C = 10pf		300			*		kHz
	C_C = 3.3pf		500			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = ±200mA	±Vs–10	±Vs–6.5		*	*		V
VOLTAGE SWING[4]	I_O = ±75mA	±V–8.5	±Vs–6.0		*	*		V
VOLTAGE SWING[4]	I_O = ±20mA	±V–7.5	±Vs–5.5		*	*		V
CURRENT, continuous	T_C = 85°C	±200				*		mA
SLEW RATE, A_V = 20	C_C = 10pf		400			*		V/µs
SLEW RATE, A_V = 100	C_C = OPEN		1000		700	*		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			*		*	pf
SETTLING TIME to .1%	C_C = 10pf, 2V step		1			*		µs
RESISTANCE, no load	R_{CL} = 0		50			*		Ω
POWER SUPPLY								
VOLTAGE[6]	Full temperature range	±15	±200	±225	*	*	*	V
CURRENT, quiescent			21	25		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			2.5			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			4.2			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W

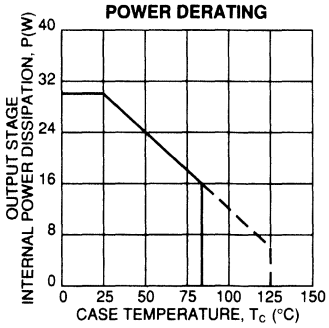
NOTES: * The specification of PA85A is identical to the specification for PA85 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

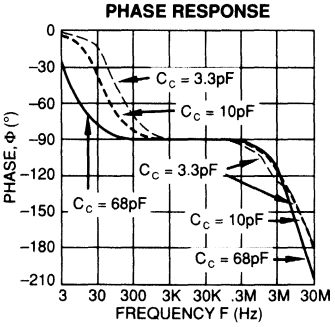
CAUTION The PA85 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

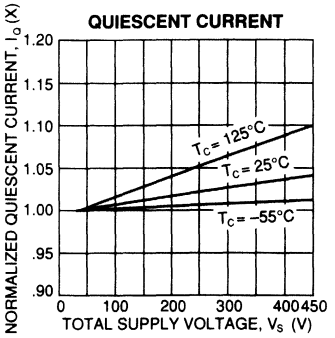
POWER DERATING



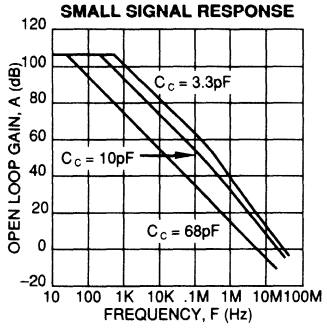
PHASE RESPONSE



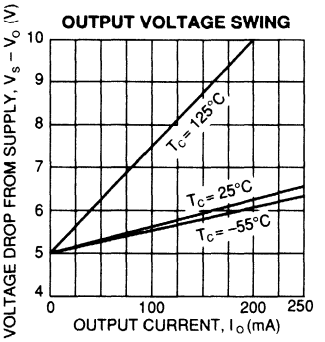
QUIESCENT CURRENT



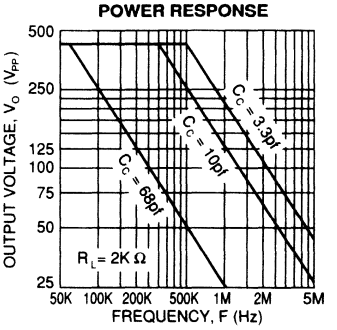
SMALL SIGNAL RESPONSE



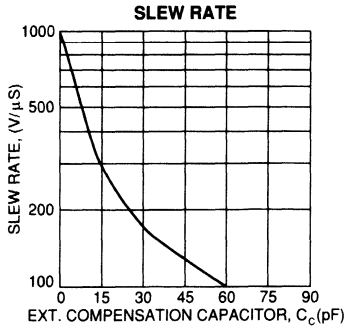
OUTPUT VOLTAGE SWING



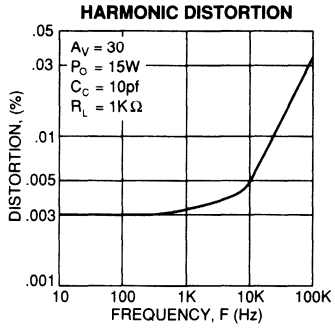
POWER RESPONSE



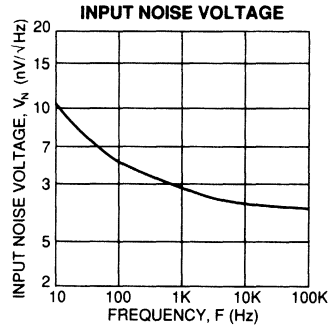
SLEW RATE



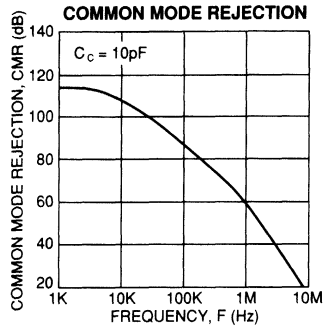
HARMONIC DISTORTION



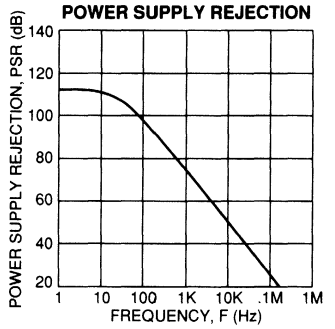
INPUT NOISE VOLTAGE



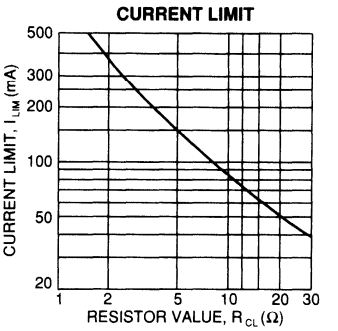
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 1.4 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 30 ohms.

$$R_{CL} = \frac{.7}{I_{LIM} - .016}$$

SAFE OPERATING AREA (SOA)

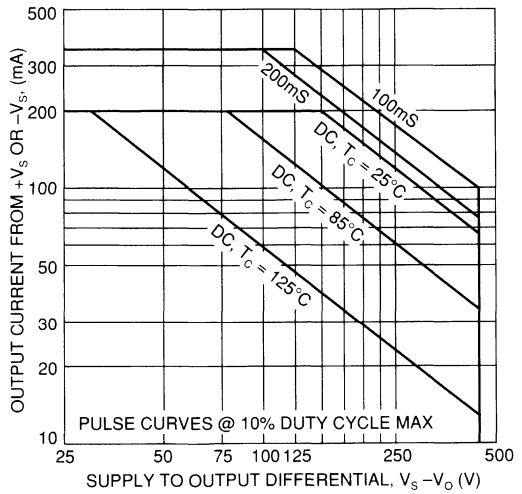
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.



INPUT PROTECTION

Although the PA85 can withstand differential voltages up to ±25V, additional external protection is recommended. Since the PA85 is a high speed amplifier, low leakage, low capacitance JFETs connected as diodes are recommended (e.g. 2N4416, Q1-Q4 in Figure 2). The differential input voltage will be clamped to ±1.4V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

In applications where the PA85 is to be operated with power supply voltages near the absolute maximum rating, unidirectional zener diode transient absorbers such as 1N6448A are recommended as protection on the supply pins (Z1, Z2 in Figure 2). The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to a diode drop from ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

STABILITY

The PA85 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

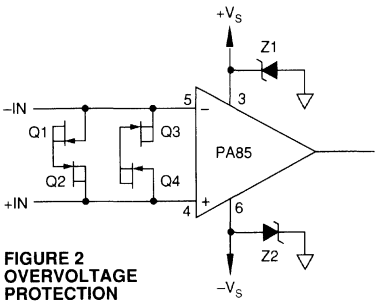
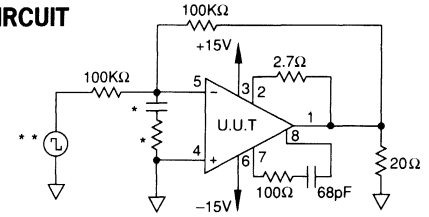


FIGURE 2 OVERVOLTAGE PROTECTION

TABLE 4 GROUP A INSPECTION
PA85M

SG	PARAMETER***	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		25	mA
1	Input offset voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		±4	mV
1	Input offset voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		±2	mV
1	Input bias current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input bias current, –IN	$-I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input offset current	I_{OS}	25°C	±150V	V_{IN} = 0		±100	pA
3	Quiescent current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		28	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		±6.4	mV
3	Input offset voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		±4.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input bias current, –IN	$-I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input offset current	I_{OS}	–55°C	±150V	V_{IN} = 0		±50	pA
2	Quiescent current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		28	mA
2	Input offset voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		±7	mV
2	Input offset voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		±5	mV
2	Input bias current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input bias current, –IN	$-I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input offset current	I_{OS}	125°C	±150V	V_{IN} = 0		±10	nA
4	Output voltage, I_O = 200mA	V_O	25°C	±50V	R_L = 200Ω	40		V
4	Output voltage, I_O = 70mA	V_O	25°C	±150V	R_L = 2KΩ	141		V
4	Output voltage, I_O = 20mA	V_O	25°C	±48V	R_L = 2KΩ	40		V
4	Current limits	I_{CL}	25°C	±50V	R_{CL} = 10Ω, R_L = 200Ω	60	112	mA
4	Stability/noise	E_N	25°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
4	Slew rate	SR	25°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
4	Open loop gain	A_{OL}	25°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
4	Common-mode rejection	CMR	25°C	±150V	F = DC, V_{CM} = ±90V	90		dB
6	Output voltage, I_O = 200mA	V_O	–55°C	±50V	R_L = 200Ω	40		V
6	Output voltage, I_O = 70mA	V_O	–55°C	±150V	R_L = 2KΩ	141		V
6	Output voltage, I_O = 20mA	V_O	–55°C	±48V	R_L = 2KΩ	40		V
6	Stability/noise	E_N	–55°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
6	Slew rate	SR	–55°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
6	Open loop gain	A_{OL}	–55°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
6	Common-mode rejection	CMR	–55°C	±150V	F = DC, V_{CM} = ±90V	90		dB
5	Output voltage, I_O = 150mA	V_O	125°C	±40V	R_L = 200Ω	30		V
5	Output voltage, I_O = 70mA	V_O	125°C	±150V	R_L = 2KΩ	141		V
5	Output voltage, I_O = 20mA	V_O	125°C	±48V	R_L = 2KΩ	40		V
5	Stability/noise	E_N	125°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
5	Slew rate	SR	125°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	400		V/µs
5	Open loop gain	A_{OL}	125°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
5	Common-mode rejection	CMR	125°C	±150V	F = DC, V_{CM} = ±90V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

*** An additional test is performed manually at T_C = 25°C which stresses power supply, common mode range and output swing to ±225V (450V total).

NOTES:

PA88 • PA88A

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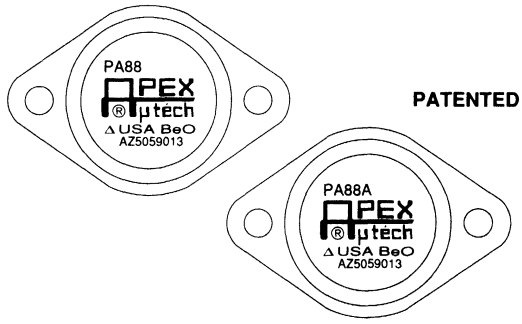
FEATURES

- HIGH VOLTAGE — 450V
- LOW QUIESCENT CURRENT — 2mA
- HIGH OUTPUT CURRENT — 100mA
- PROGRAMMABLE CURRENT LIMIT
- LOW BIAS CURRENT — FET Input

APPLICATIONS

- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC TRANSDUCERS
- PROGRAMMABLE POWER SUPPLIES UP TO 440V



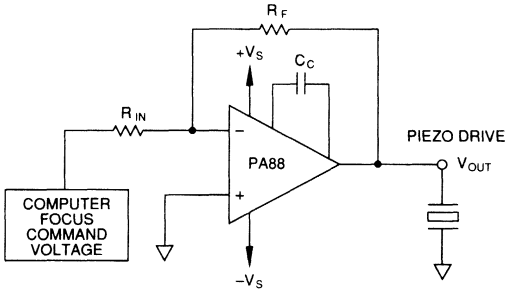
PATENTED

DESCRIPTION

The PA88 is a high voltage, low quiescent current MOSFET operational amplifier designed for output currents up to 100mA. Output voltages can swing up to ±215V with a dual supply and up to +440 volts with a single supply. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration. All internal biasing is referenced to a bootstrapped zener-MOSFET current source. As a result, the PA88 features an unprecedented supply range and excellent supply rejection. The MOSFET output stage is biased on for linear operation. External compensation provides user flexibility.

This hybrid circuit utilizes beryllia (BeO) substrates, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

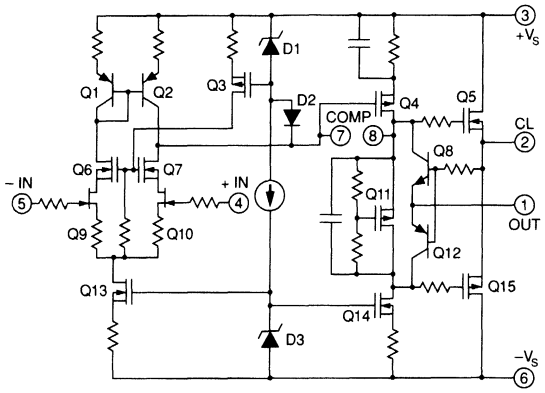
TYPICAL APPLICATION



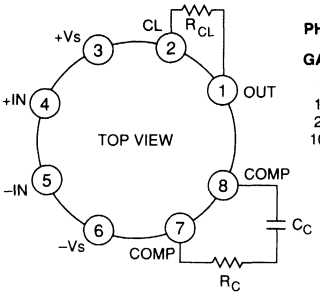
LOW POWER, PIEZOELECTRIC POSITIONING

Piezo positioning may be applied to the focusing of segmented mirror systems. The composite mirror may be composed of hundreds of elements, each requiring focusing under computer control. In such complex systems the PA88's advantage of low quiescent power consumption reduces the costs of power supplies and cooling, while providing the interface between the computer and the high voltage drive to the piezo positioners.

EQUIVALENT SCHEMATIC



EXTERNAL CONNECTIONS



PHASE COMPENSATION

GAIN	C_C	R_C
1	68pf	100 Ω
10	33pf	100 Ω
20	15pf	100 Ω
100	3.3pf	—

$$R_{CL} = \frac{.7}{I_{LIM}}$$

C_C RATED FOR FULL SUPPLY VOLTAGE

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	450V
OUTPUT CURRENT, source, sink	See SOA
POWER DISSIPATION, continuous @ T_C = 25°C	15W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

		PA88			PA88A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			1	5		*	*	µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/√kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT, vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			2.5	100		3	20	pA
INPUT IMPEDANCE, DC			10^{11}			*		Ω
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]		$\pm V_S$–12			*			V
COMMON MODE REJECTION, DC	V_{CM} = ±90V	90	110		*	*		dB
NOISE	100kHz BW, R_S = 1KΩ, C_C = 15pf		2			*		µVrms
GAIN								
OPEN LOOP, @ 15Hz	R_L = 2KΩ, C_C = OPEN	96	111		*	*		dB
GAIN BANDWIDTH PRODUCT at 1MHz	R_L = 2KΩ, C_C = 15pf, R_C = 100Ω		2.1			*		MHz
POWER BANDWIDTH	R_L = 2KΩ, C_C = 15pf, R_C = 100Ω		6			*		kHz
PHASE MARGIN	Full temperature range		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = ±100mA	$\pm V_S$–10	$\pm V_S$–8.8		*	*		V
VOLTAGE SWING[4]	Full temp. range, I_O = ±75mA	$\pm V_S$–8.5	$\pm V_S$–7.5		*	*		V
VOLTAGE SWING[4]	Full temp. range, I_O = ±20mA	$\pm V_S$–7.5	$\pm V_S$–5.2		*	*		V
CURRENT, continuous	T_C = 85°C	±100				*		mA
SLEW RATE, A_V = 20	C_C = 15pf, R_C = 100Ω		8			*		V/µs
SLEW RATE, A_V = 100	C_C = OPEN		30			*		V/µs
CAPACITIVE LOAD, A_V = +1	Full temperature range	470			*			pf
SETTLING TIME to .1%	C_C = 15pf, R_C = 100Ω, 2V step		10			*		µs
RESISTANCE, no load	R_{CL} = 0		100			*		Ω
POWER SUPPLY								
VOLTAGE[6]	See note 6	±15	±200	±225	*	*	*	V
CURRENT, quiescent,			1.7	2		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz			5.0			*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz			8.3			*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W

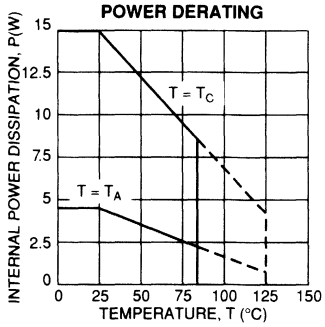
NOTES: * The specification of PA88A is identical to the specification for PA88 in applicable column to the left.

1. Unless otherwise noted: T_C = 25°C, compensation = C_C = 68pF, R_C = 100Ω. DC input specifications are ± value given. Power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative power supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Derate max supply rating .625 V/°C below 25°C case. No derating needed above 25°C case.

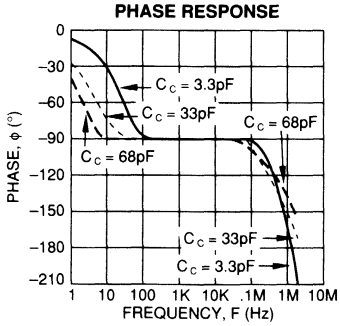
CAUTION The PA88 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

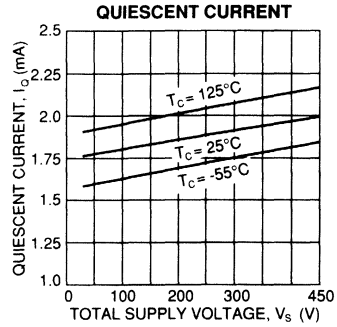
POWER DERATING



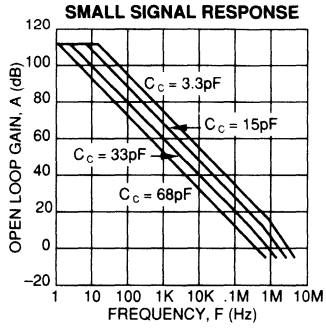
PHASE RESPONSE



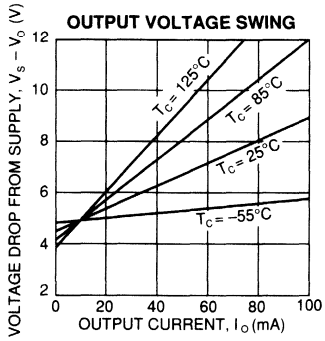
QUIESCENT CURRENT



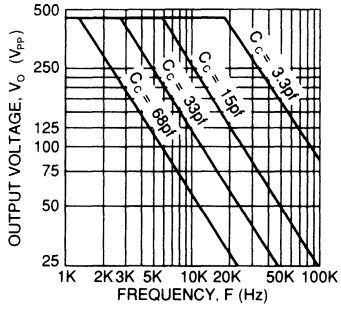
SMALL SIGNAL RESPONSE



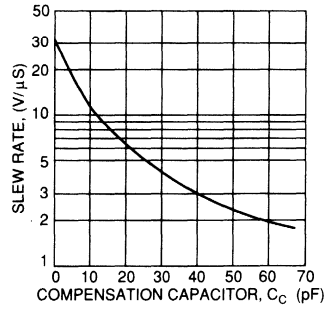
OUTPUT VOLTAGE SWING



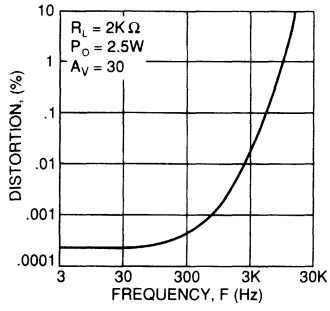
POWER RESPONSE



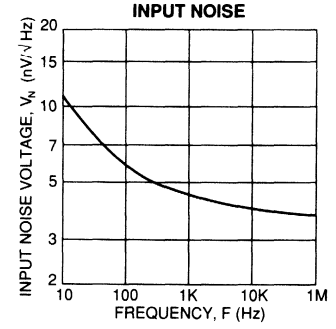
SLEW RATE



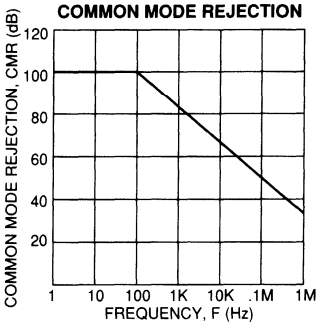
HARMONIC DISTORTION



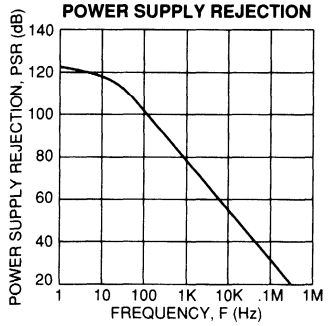
INPUT NOISE



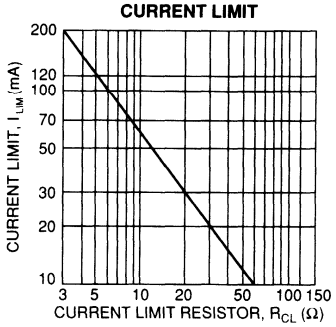
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows; with the maximum practical value of 150 ohms.

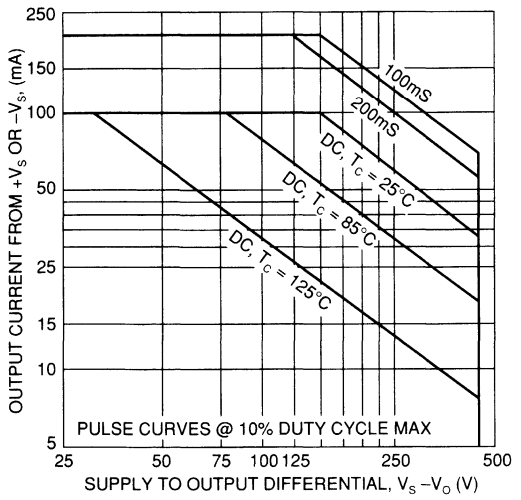
$$R_{CL} = \frac{.7}{I_{LIM}}$$

SAFE OPERATING AREA (SOA)

The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.



INPUT PROTECTION

Although the PA88 can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 or 1N914 signal diodes are sufficient (D1, D2 in Figure 2a). In more demanding applications where low leakage or low capacitance are of concern 2N4416 or 2N5457-2N5459 JFETs connected as diodes will be required (Q1, Q2 in Figure 2b). In either case the input differential voltage will be clamped to ±.7V. This is sufficient overdrive to produce maximum power bandwidth.

POWER SUPPLY PROTECTION

In applications where the PA88 is to be operated with power supply voltages near the absolute maximum rating, unidirectional zener diode transient absorbers such as 1N6448A are recommended as protection on the supply pins (Z1, Z2 in Figure 2). The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to a diode drop from ground. Whether the zeners are used or not, the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversal as well as line regulation.

STABILITY

The PA88 has sufficient phase margin to be stable with most capacitive loads at a gain of 4 or more, using the recommended phase compensation. However, the low pass circuit created by the sumpoint (–in) capacitance and the feedback network may add phase shift and cause instabilities. As a general rule, the sumpoint load resistance (input and feedback resistors in parallel) should be 1K ohm or less at low gain settings (up to 10). Alternatively, use a bypass capacitor across the feedback resistor. The time constant of the feedback resistor and bypass capacitor combination should match the time constant of the sumpoint resistance and sumpoint capacitance.

The PA88 is externally compensated and performance can be tailored to the application. Use the graphs of small signal response and power response as a guide. The compensation capacitor C_C must be rated at 500V working voltage. An NPO capacitor is recommended. The compensation network C_CR_C must be mounted closely to the amplifier pins 7 and 8 to avoid spurious oscillation.

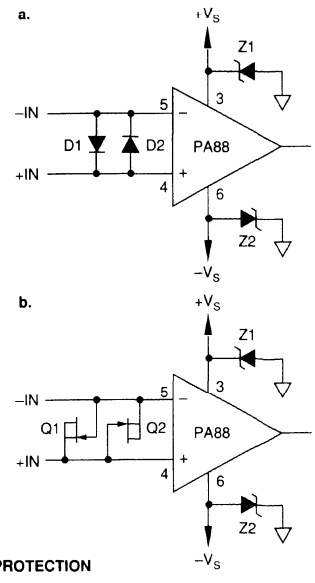
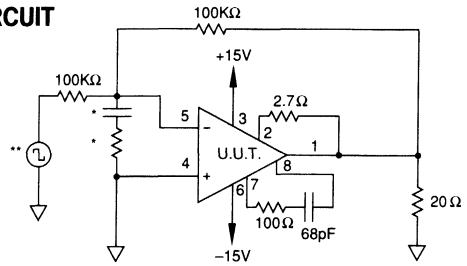


FIGURE 2. OVERVOLTAGE PROTECTION

SG	PARAMETER***	SYMBOL	TEMP.	POWER	TEST CONDITIONS	MIN	MAX	UNITS
1	Quiescent current	I_Q	25°C	±150V	V_{IN} = 0, A_V = 100		2	mA
1	Input offset voltage	V_{OS}	25°C	±15V	V_{IN} = 0, A_V = 100		±4	mV
1	Input offset voltage	V_{OS}	25°C	±150V	V_{IN} = 0, A_V = 100		±2	mV
1	Input bias current, +IN	$+I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input bias current, –IN	$-I_B$	25°C	±150V	V_{IN} = 0		±50	pA
1	Input offset current	I_{OS}	25°C	±150V	V_{IN} = 0		±100	pA
3	Quiescent current	I_Q	–55°C	±150V	V_{IN} = 0, A_V = 100		2.3	mA
3	Input offset voltage	V_{OS}	–55°C	±15V	V_{IN} = 0, A_V = 100		±6.4	mV
3	Input offset voltage	V_{OS}	–55°C	±150V	V_{IN} = 0, A_V = 100		±4.4	mV
3	Input bias current, +IN	$+I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input bias current, –IN	$-I_B$	–55°C	±150V	V_{IN} = 0		±50	pA
3	Input offset current	I_{OS}	–55°C	±150V	V_{IN} = 0		±50	pA
2	Quiescent current	I_Q	125°C	±150V	V_{IN} = 0, A_V = 100		2.3	mA
2	Input offset voltage	V_{OS}	125°C	±15V	V_{IN} = 0, A_V = 100		±7	mV
2	Input offset voltage	V_{OS}	125°C	±150V	V_{IN} = 0, A_V = 100		±5	mV
2	Input bias current, +IN	$+I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input bias current, –IN	$-I_B$	125°C	±150V	V_{IN} = 0		±10	nA
2	Input offset current	I_{OS}	125°C	±150V	V_{IN} = 0		±10	nA
4	Output voltage, I_O = 100mA	V_O	25°C	±30V	R_L = 200Ω	20		V
4	Output voltage, I_O = 70mA	V_O	25°C	±150V	R_L = 2KΩ	141		V
4	Output voltage, I_O = 20mA	V_O	25°C	±48V	R_L = 2KΩ	40		V
4	Current limits	I_{CL}	25°C	±50V	R_{CL} = 10Ω, R_L = 200Ω	50	84	mA
4	Stability/noise	E_N	25°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
4	Slew rate	SR	25°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	15		V/µs
4	Open loop gain	A_{OL}	25°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
4	Common-mode rejection	CMR	25°C	±150V	F = DC, V_{CM} = ±90V	90		dB
6	Output voltage, I_O = 100mA	V_O	–55°C	±30V	R_L = 200Ω	20		V
6	Output voltage, I_O = 70mA	V_O	–55°C	±150V	R_L = 2KΩ	141		V
6	Output voltage, I_O = 20mA	V_O	–55°C	±48V	R_L = 2KΩ	40		V
6	Stability/noise	E_N	–55°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
6	Slew rate	SR	–55°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	15		V/µs
6	Open loop gain	A_{OL}	–55°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
6	Common-mode rejection	CMR	–55°C	±150V	F = DC, V_{CM} = ±90V	90		dB
5	Output voltage, I_O = 75mA	V_O	125°C	±25V	R_L = 200Ω	13		V
5	Output voltage, I_O = 37mA	V_O	125°C	±83V	R_L = 2KΩ	74		V
5	Output voltage, I_O = 10mA	V_O	125°C	±28V	R_L = 2KΩ	20		V
5	Stability/noise	E_N	125°C	±150V	C_C = 68pF, R_C = 100Ω, A_V = +1, C_L = 470pF		1	mV
5	Slew rate	SR	125°C	±150V	R_L = 2KΩ, A_V = 100, C_C = OPEN	15		V/µs
5	Open loop gain	A_{OL}	125°C	±150V	R_L = 2KΩ, F = 15Hz, C_C = OPEN	96		dB
5	Common-mode rejection	CMR	125°C	±150V	F = DC, V_{CM} = ±90V	90		dB

BURN IN CIRCUIT



* These components are used to stabilize device due to poor high frequency characteristics of burn in board.

** Input signals are calculated to result in internal power dissipation of approximately 2.1W at case temperature = 125°C.

*** An additional test is performed manually at T_C = 25°C which stresses power supply, common mode range and output swing to ±225V (450V total).

NOTES:

POWER OPERATIONAL AMPLIFIERS
PA89 • PA89A

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- 1000V P-P SIGNAL OUTPUT
- WIDE SUPPLY RANGE — ±75V to ±600V
- PROGRAMMABLE CURRENT LIMIT
- 75 mA CONTINUOUS OUTPUT CURRENT
- HERMETICITY 100% TESTED
- INPUT PROTECTION

APPLICATIONS

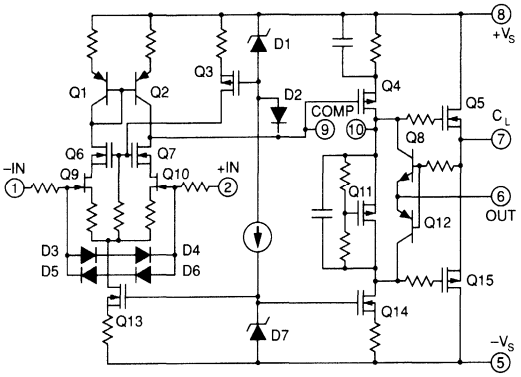
- PIEZOELECTRIC POSITIONING
- HIGH VOLTAGE INSTRUMENTATION
- ELECTROSTATIC DEFLECTION
- SEMICONDUCTOR TESTING

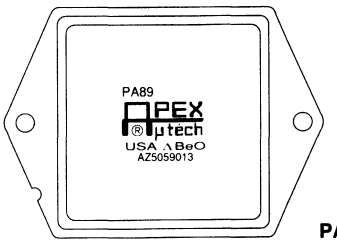
DESCRIPTION

The PA89 is an ultra high voltage, MOSFET operational amplifier designed for output currents up to 75 mA. Output voltages can swing over 1000V p-p. The safe operating area (SOA) has no second breakdown limitations and can be observed with all types of loads by choosing an appropriate current limiting resistor. High accuracy is achieved with a cascode input circuit configuration and 120dB open loop gain. All internal biasing is referenced to a bootstrapped zener-MOSFET current source, giving the PA89 a wide supply range and excellent supply rejection. The MOSFET output stage is biased for class A/B linear operation. External compensation provides user flexibility. The PA89 is 100% fine and gross leak tested to military standards for long term reliability.

This hybrid integrated circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The MO-127 High Voltage, Power Dip™ package is hermetically sealed and electrically isolated.

SIMPLIFIED SCHEMATIC

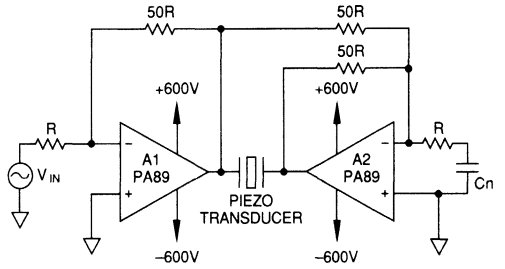




PATENTED

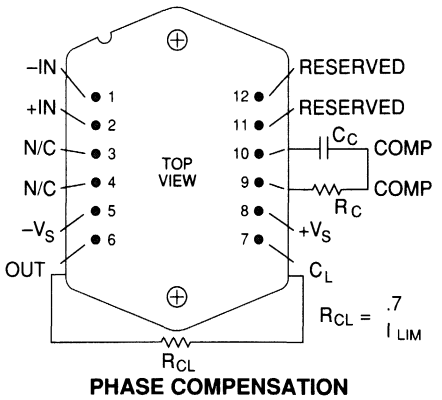
TYPICAL APPLICATION

Ultra-high voltage capability combined with the bridge amplifier configuration makes it possible to develop +/–1000 volt peak swings across a piezo element. A high gain of –50 for A1 insures stability with the capacitive load, while "noise-gain" compensation Rn and Cn on A2 insure the stability of A2 by operating in a noise gain of 50.



SINGLE AXIS MICRO-POSITIONING

EXTERNAL CONNECTIONS*



PHASE COMPENSATION

Gain	C_c	R_c
1	470pF	470Ω
10	68pF	220Ω
15	33pF	220Ω
100	15pF	220Ω

Note: C_c must be rated for full supply voltage –Vs to +Vs.

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	1200V
OUTPUT CURRENT, within SOA	100mA
POWER DISSIPATION, internal at T_C = 25°C	40W
INPUT VOLTAGE, differential	±25V
INPUT VOLTAGE, common mode	$\pm V_S \mp 25V$
TEMPERATURE, pin solder - 10s max	300°C
TEMPERATURE, junction[2]	150°C
TEMPERATURE, storage	–65 to 125°C
OPERATING TEMPERATURE RANGE, case	–55 to 125°C

SPECIFICATIONS

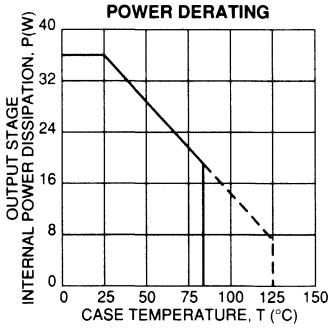
		PA89			PA89A			
PARAMETER	**TEST CONDITIONS[1]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			.5	2		.25	.5	mV
OFFSET VOLTAGE, vs. temperature	Full temperature range		10	30		5	10	µV/°C
OFFSET VOLTAGE, vs. supply			7			*		µV/V
OFFSET VOLTAGE, vs. time			75			*		µV/kh
BIAS CURRENT, initial[3]			5	50		3	10	pA
BIAS CURRENT,vs. supply			.01			*		pA/V
OFFSET CURRENT, initial[3]			5	50		3	20	pA
INPUT IMPEDANCE, DC			10^5			*		MΩ
INPUT CAPACITANCE			4			*		pF
COMMON MODE VOLTAGE RANGE[4]	Full temperature range	$\pm V_S \mp 50$			*			V
COMMON MODE REJECTION, DC	Full temperature range, V_{CM} = ±90V	96	110		*	*		dB
INPUT NOISE	10kHz BW, R_S = 10K, C_C = 15pF		4					µV RMS
GAIN								
OPEN LOOP GAIN at 10Hz	R_L = 10k, C_C = 15pF	108	120		*	*		dB
GAIN BANDWIDTH PRODUCT	R_L = 10k, C_C = 15pF, A_V = 100		10			*		MHz
POWER BANDWIDTH	R_L = 10k, C_C = 15pF, V_O = 500V p-p		5			*		kHz
PHASE MARGIN	Full temperature range, A_V = 10		60			*		°
OUTPUT								
VOLTAGE SWING[4]	I_O = 75mA	$\pm V_S \mp 30$	$\pm V_S \mp 15$		*	*		V
VOLTAGE SWING[4]	Full temperature range, I_O = 20mA	$\pm V_S \mp 20$	$\pm V_S \mp 12$		*	*		V
CURRENT, continuous	Full temperature range	75			*			mA
SLEW RATE	C_C = 15pF, A_V = 100	12	16		*	*		V/µs
CAPACITIVE LOAD, Av = 10	Full temperature range			1			*	nF
CAPACITIVE LOAD, Av>10	Full temperature range			SOA			*	
SETTLING TIME to .1%	R_L = 10KΩ, 10V step, Av = 10		2			*		µs
POWER SUPPLY								
VOLTAGE, V_S[4]	Full temperature range	±75	±500	±600	*	*	*	V
CURRENT, quiescent			4.8	6.0		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[5]	Full temperature range, F > 60Hz		2.1	2.3		*	*	°C/W
RESISTANCE, DC, junction to case	Full temperature range, F < 60Hz		3.3	3.5		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		20			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of PA89A is identical to the specification for PA89 in applicable column to the left.
1. Unless otherwise noted: T_C = 25°C, C_C = 68pF, R_C = 220Ω, and V_S = ±500V. Input parameters for bias currents and offset voltage are ± values given.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
3. Doubles for every 10°C of temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
5. Rating applies only if the output current alternates between both output transistors at a rate faster than 60Hz.

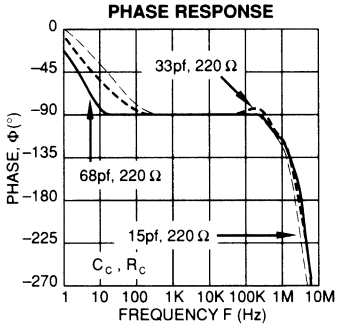
CAUTION The PA89 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

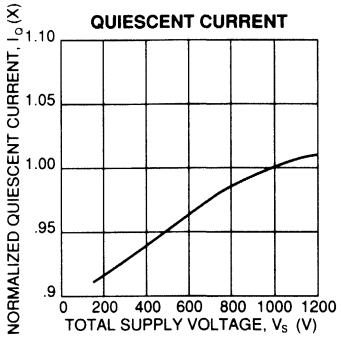
POWER DERATING



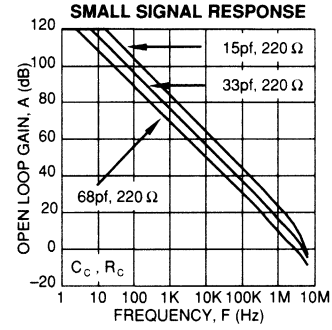
PHASE RESPONSE



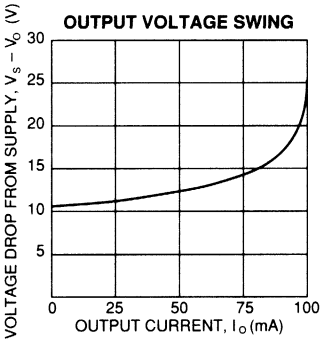
QUIESCENT CURRENT



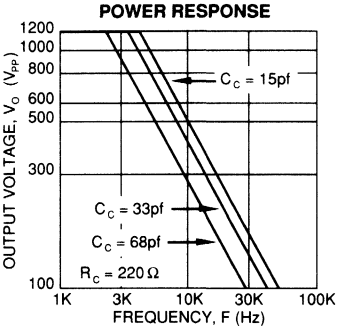
SMALL SIGNAL RESPONSE



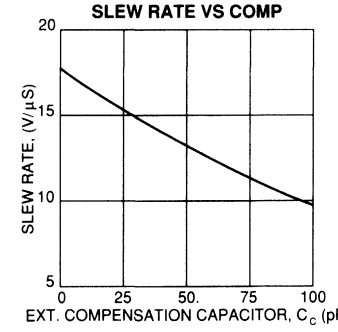
OUTPUT VOLTAGE SWING



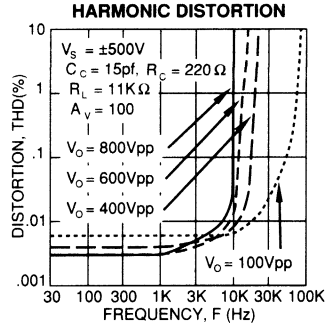
POWER RESPONSE



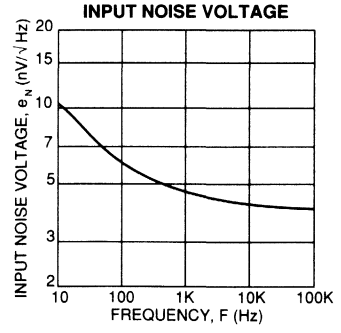
SLEW RATE VS COMP



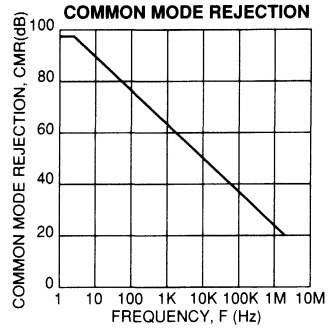
HARMONIC DISTORTION



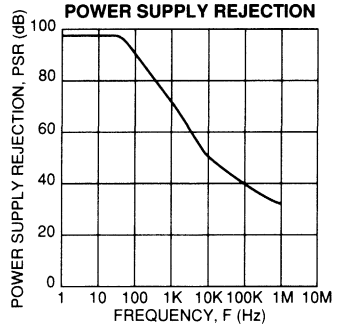
INPUT NOISE VOLTAGE



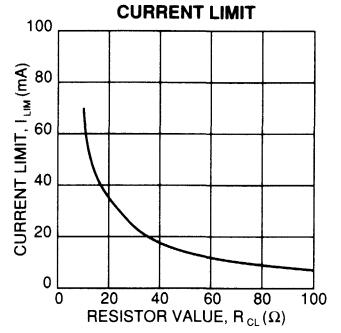
COMMON MODE REJECTION



POWER SUPPLY REJECTION



CURRENT LIMIT



GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

STABILITY

Although the PA89 can be operated at unity gain, maximum slew rate and bandwidth performance was designed to be obtained at gains of 10 or more. Use the small signal response and phase response graphs as a guide. In applications where gains of less than 10 are required, use noise gain compensation to increase the phase margin of the application circuit as illustrated in the typical application drawing.

SAFE OPERATING AREA (SOA)

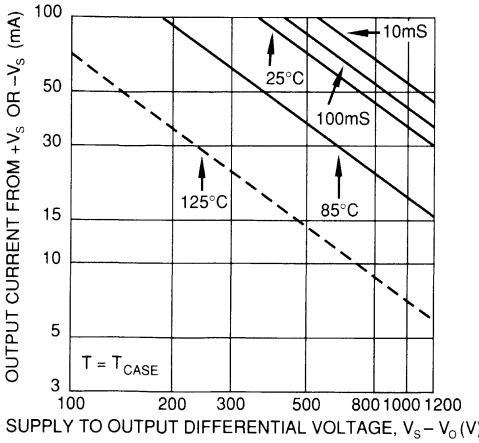
The MOSFET output stage of this power operational amplifier has two distinct limitations:

1. The current handling capability of the MOSFET geometry and the wire bonds.
2. The junction temperature of the output MOSFETs.

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

SAFE OPERATING CURVES

The safe operating area curves define the maximum additional internal power dissipation the amplifier can tolerate when it produces the necessary output to drive an external load. This is not the same as the absolute maximum internal power dissipation listed elsewhere in the specification since the quiescent power dissipation is significant compared to the total.



EXTERNAL COMPONENTS

The very high operating voltages of the PA89 demand consideration of two component specifications rarely of concern in building op amp circuits: voltage rating and voltage coefficient.

The compensation capacitance C_C must be rated for the full supply voltage range. For example, with supply voltages of ±500V the possible voltage swing across C_C is 1000V. In addition, a voltage coefficient less than 100PPM is recommended to maintain the capacitance variation to less than 5% for this example.

Of equal importance are the voltage rating and voltage coefficient of the gain setting resistances. Typical voltage ratings of low wattage resistors are 150 to 250V. In the above example 1000V could appear across the feedback resistor. This would require several resistors in series to obtain the proper voltage rating. Low voltage coefficient resistors will insure good gain linearity. The wattage rating of the feedback resistor is also of concern. A 1 megohm feedback resistor could easily develop 1 watt of power dissipation.

Though high voltage rated resistors can be obtained, a 1 megohm feedback resistor comprised of five 200Kohm, 1/4 watt metal film resistors in series will produce the proper voltage rating, voltage coefficient and wattage rating.

CURRENT LIMIT

For proper operation the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 3.5 ohm, however for optimum reliability the resistor value should be set as high as possible. The value is calculated as follows with the maximum practical value of 150 ohms.

$$R_{CL} = \frac{.7}{I_{LIM}}$$

When setting the value for R_{CL} allow for the load current as well as the current in the feedback resistor. Also allow for the temperature coefficient of the current limit which is approximately -0.3% /°C of case temperature rise.

CAUTIONS

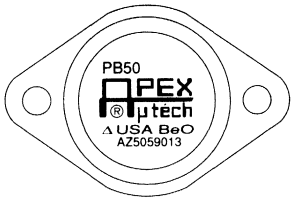
The operating voltages of the PA89 are potentially lethal. During circuit design, develop a functioning circuit at the lowest possible voltages. Clip test leads should be used for "hands off" measurements while troubleshooting.

POWER BOOSTER AMPLIFIER
PB50

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

FEATURES

- **WIDE SUPPLY RANGE — ±30V to ±100V**
- **HIGH OUTPUT CURRENT — Up to 2A Continuous**
- **VOLTAGE AND CURRENT GAIN**
- **HIGH SLEW RATE — 50V/μs Minimum**
- **PROGRAMMABLE OUTPUT CURRENT LIMIT**
- **HIGH POWER BANDWIDTH — 160 kHz Minimum**
- **LOW QUIESCENT CURRENT — 12mA Typical**



APPLICATIONS

- **HIGH VOLTAGE INSTRUMENTATION**
- **Electrostatic TRANSDUCERS & DEFLECTION**
- **Programmable Power Supplies Up to 180V p-p**

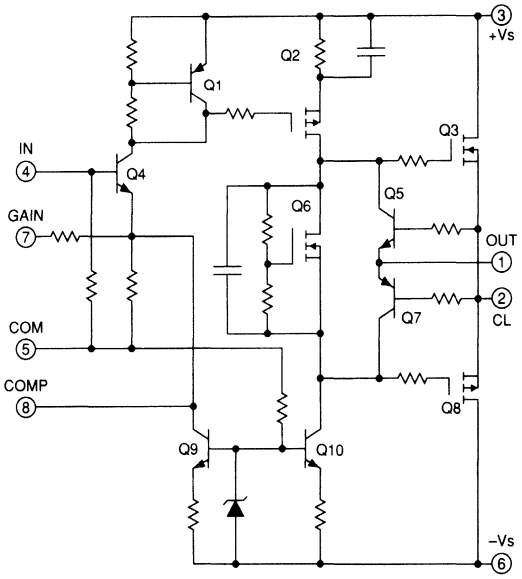
DESCRIPTION

The PB50 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB50 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Junction Transistors. Internal feedback and gainset resistors are provided for a pin-strappable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Although the booster can be configured quite simply, enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATION

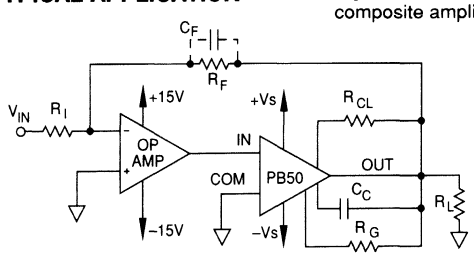
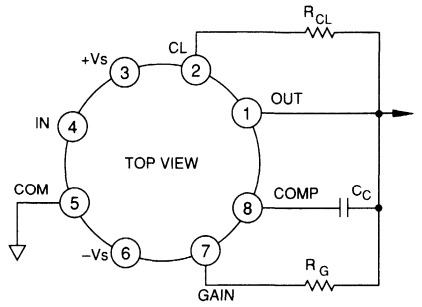


Figure 1. Inverting composite amplifier.

EXTERNAL CONNECTIONS



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	200V
OUTPUT CURRENT, within SOA	2A
POWER DISSIPATION, internal at T_C = 25°C[1]	35W
INPUT VOLTAGE, referred to common	±15V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	150°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

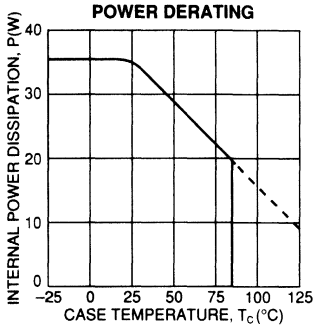
PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			±75	±1.75	V
OFFSET VOLTAGE, vs. temperature	Full temperature range		–4.5	–7	mV/°C
INPUT IMPEDANCE, DC		25	50		kΩ
INPUT CAPACITANCE			3		pF
INPUT VOLTAGE RANGE	Referred to common			±15	V
CLOSED LOOP GAIN RANGE		3	10	25	V/V
GAIN ACCURACY, internal Rg, Rf	A_V = 3		±10	±15	%
GAIN ACCURACY, external Rf	A_V = 10		±15	±25	%
PHASE SHIFT	F = 10kHz, AV_{CL} = 10, C_C = 22pF		10		°
	F = 200kHz, AV_{CL} = 10, C_C = 22pF		60		°
OUTPUT					
VOLTAGE SWING	Io = 2A	V_S–11	V_S –9		V
VOLTAGE SWING	Io = 1A	V_S–10	V_S –7		V
VOLTAGE SWING	Io = .1A	V_S–8	V_S –5		V
CURRENT, continuous		2			A
SLEW RATE	Full temperature range	50	100		V/µs
CAPACITIVE LOAD	Full temperature range		2200		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2		µs
POWER BANDWIDTH	V_C = 100Vpp	160	320		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 25, Vcc = ±100		100		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 3, Vcc = ±30		1		MHz
POWER SUPPLY					
VOLTAGE, $\pm V_S$[3]	Full temperature range	±30[5]	±60	±100	V
CURRENT, quiescent	V_S = ±30		9	12	mA
	V_S = ±60		12	18	mA
	V_S = ±100		17	25	mA
THERMAL					
RESISTANCE, AC junction to case[4]	Full temp. range, F > 60Hz		1.8	2.0	°C/W
RESISTANCE, DC junction to case	Full temp. range, F < 60Hz		3.2	3.5	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	°C

NOTES: 1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
5. –Vs must be at least 30V below COM.

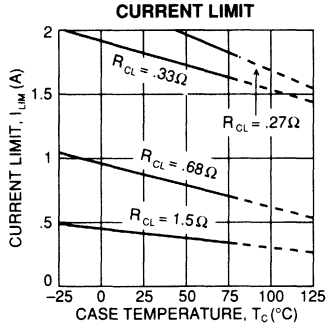
CAUTION The PB50 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

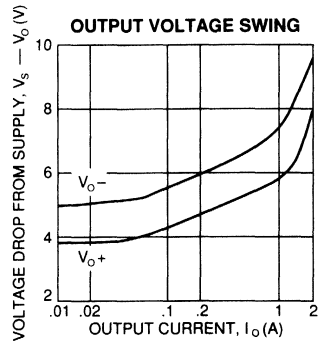
POWER DERATING



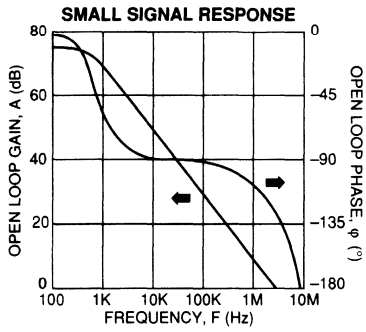
CURRENT LIMIT



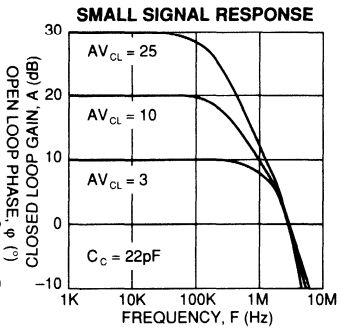
OUTPUT VOLTAGE SWING



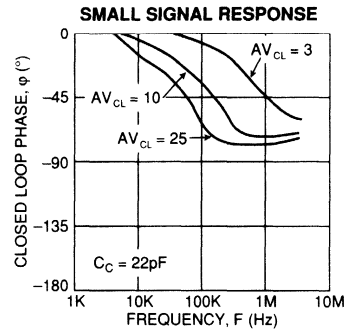
SMALL SIGNAL RESPONSE



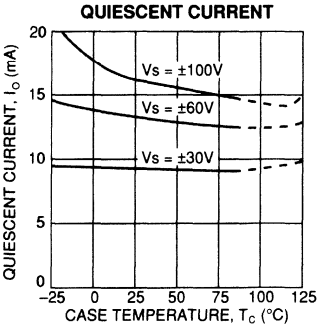
SMALL SIGNAL RESPONSE



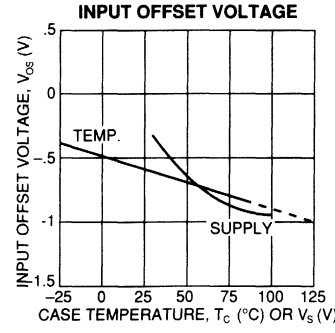
SMALL SIGNAL RESPONSE



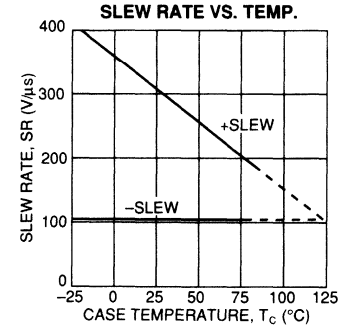
QUIESCENT CURRENT



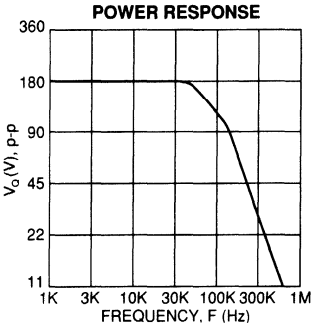
INPUT OFFSET VOLTAGE



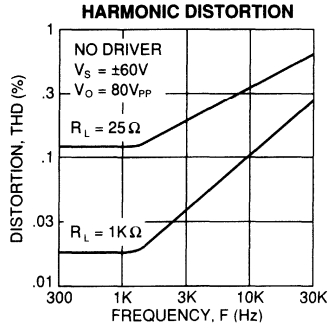
SLEW RATE VS. TEMP.



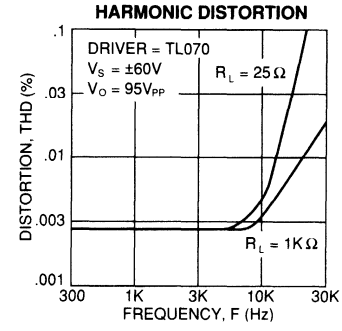
POWER RESPONSE



HARMONIC DISTORTION



HARMONIC DISTORTION



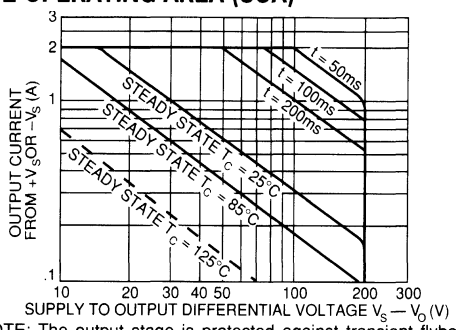
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.27Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.2K) + 1 = 3

Av (composite) = 60K/2K = - 30

Av (driver) = - 30/3 = -10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60
For: R_F = 33K, R_I = 3.3K, R_G = 22K					

Table 1: Typical values for case where op amp effective gain = 1.

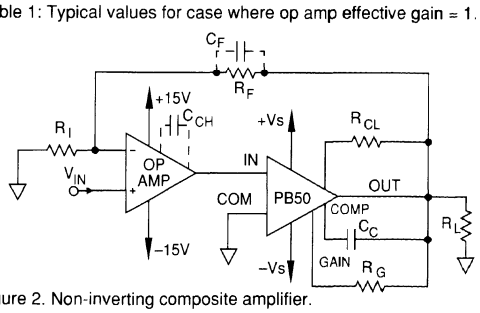


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

FEATURES

- **WIDE SUPPLY RANGE — ±15V to ±150V**
- **HIGH OUTPUT CURRENT —**
  - **1.5A Continuous (PB58)**
  - **2.0A Continuous (PB58A)**
- **VOLTAGE AND CURRENT GAIN**
- **HIGH SLEW — 50V/µs Minimum (PB58)**
  75V/µs Minimum (PB58A)
- **PROGRAMMABLE OUTPUT CURRENT LIMIT**
- **HIGH POWER BANDWIDTH — 320 kHz Minimum**
- **LOW QUIESCENT CURRENT — 12mA Typical**

APPLICATIONS

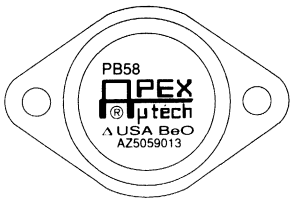
- **HIGH VOLTAGE INSTRUMENTATION**
- **Electrostatic TRANSDUCERS & DEFLECTION**
- **Programmable Power Supplies Up to 280V p-p**

DESCRIPTION

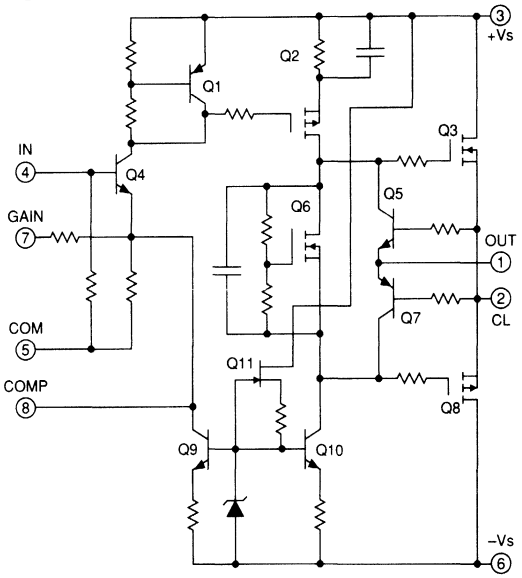
The PB58 is a high voltage, high current amplifier designed to provide voltage and current gain for a small signal, general purpose op amp. Including the power booster within the feedback loop of the driver amplifier results in a composite amplifier with the accuracy of the driver and the extended output voltage range and current capability of the booster. The PB58 can also be used without a driver in some applications, requiring only an external current limit resistor to function properly.

The output stage utilizes complementary MOSFETs, providing symmetrical output impedance and eliminating secondary breakdown limitations imposed by Bipolar Transistors. Internal feedback and gainset resistors are provided for a pin-strapable gain of 3. Additional gain can be achieved with a single external resistor. Compensation is not required for most driver/gain configurations, but can be accomplished with a single external capacitor. Enormous flexibility is provided through the choice of driver amplifier, current limit, supply voltage, voltage gain, and compensation.

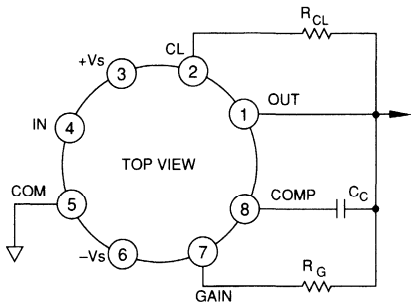
This hybrid circuit utilizes a beryllia (BeO) substrate, thick film resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is electrically isolated and hermetically sealed using one-shot resistance welding. The use of compressible isolation washers may void the warranty.



EQUIVALENT SCHEMATIC

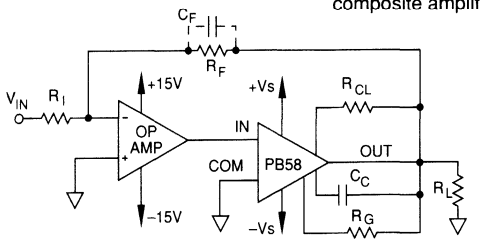


EXTERNAL CONNECTIONS



TYPICAL APPLICATION

Figure 1. Inverting composite amplifier.



ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	300V
OUTPUT CURRENT, within SOA	2.0A
POWER DISSIPATION, internal at T_C = 25°C[1]	83W
INPUT VOLTAGE, referred to common	±15V
INPUT VOLTAGE, referred to $+V_S$	$+V_S$ –6.5V
TEMPERATURE, pin solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–55 to +125°C

SPECIFICATIONS

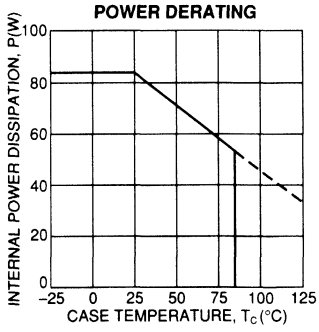
		PB58			PB58A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, initial			±75	±1.75		*	±1.0	V
OFFSET VOLTAGE, vs. temperature	Full temperature range[3]		–4.5	–7		*	*	mV/°C
INPUT IMPEDANCE, DC		25	50		*	*		kΩ
INPUT CAPACITANCE			3			*		pF
INPUT VOLTAGE RANGE	Referred to common			±15			*	V
CLOSED LOOP GAIN RANGE		3	10	25	*	*	*	V/V
GAIN ACCURACY, internal Rg, Rf	A_V = 3		±10	±15		*	*	%
GAIN ACCURACY, external Rf	A_V = 10		±15	±25		*	*	%
PHASE SHIFT	f = 10kHz, AV_{CL} = 10, C_C = 22pF		10			*		°
	f = 200kHz, AV_{CL} = 10, C_C = 22pF		60			*		°
OUTPUT								
VOLTAGE SWING	Io = 1.5A (PB58), 2A (PB58A)	Vs–11	Vs –8		Vs–12	Vs–9		V
VOLTAGE SWING	Io = 1A	Vs–10	Vs –7		*	*		V
VOLTAGE SWING	Io = .1A	Vs–8	Vs –5		*	*		V
CURRENT, continuous		1.5			2.0			A
SLEW RATE	Full temperature range	50	100		75	*		V/µs
CAPACITIVE LOAD	Full temperature range		2200			*		pF
SETTLING TIME to .1%	R_L = 100Ω, 2V step		2			*		µs
POWER BANDWIDTH	V_C = 100 Vpp	160	320		240	*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 25, Vcc = ±100		100			*		kHz
SMALL SIGNAL BANDWIDTH	C_C = 22pF, A_V = 3, Vcc = ±30		1			*		MHz
POWER SUPPLY								
VOLTAGE, ±Vs[4]	Full temperature range	±15[6]	±60	±150	*	*	*	V
CURRENT, quiescent	Vs = ±15		11			*		mA
	Vs = ±60		12			*		mA
	Vs = ±150		14	18		*	*	mA
THERMAL								
RESISTANCE, AC junction to case[5]	Full temp. range, f > 60Hz		1.2	1.3		*	*	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		1.6	1.8		*	*	°C/W
RESISTANCE, junction to air	Full temperature range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	*	*	*	°C

NOTES: * The specification of PB58A is identical to the specification for PB58 in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF (Mean Time to Failure).
2. The power supply voltage specified under typical (TYP) applies, T_C = 25°C unless otherwise noted.
3. Guaranteed by design but not tested.
4. +Vs and –Vs denote the positive and negative supply rail respectively.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. $-V_S$ must be at least 30V below common.

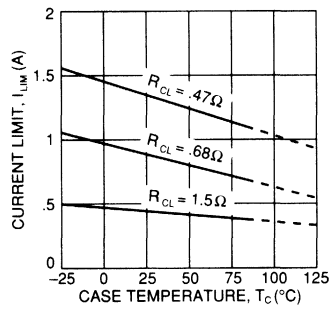
CAUTION The PB58 is constructed from MOSFET transistors. ESD handling procedures must be observed.

The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

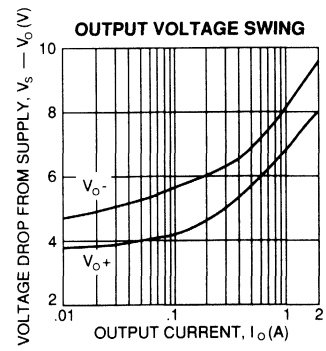
POWER DERATING



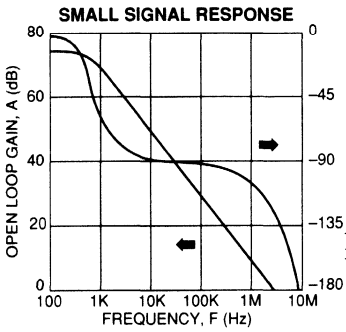
CURRENT LIMIT



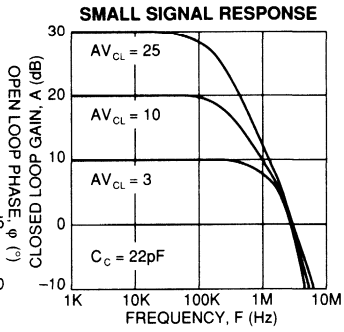
OUTPUT VOLTAGE SWING



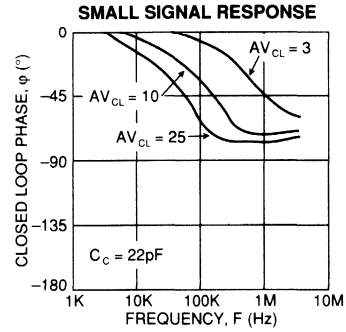
SMALL SIGNAL RESPONSE



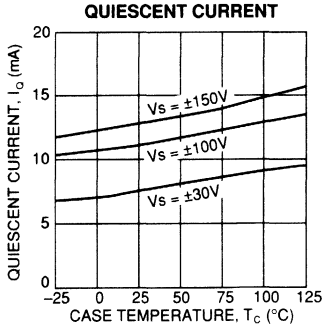
SMALL SIGNAL RESPONSE



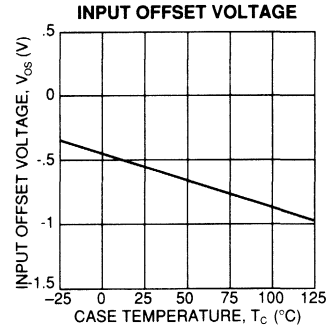
SMALL SIGNAL RESPONSE



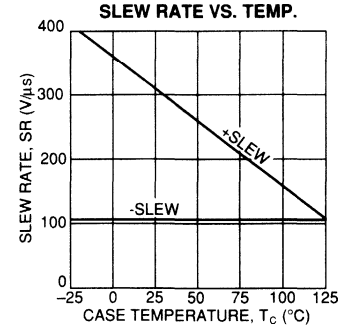
QUIESCENT CURRENT



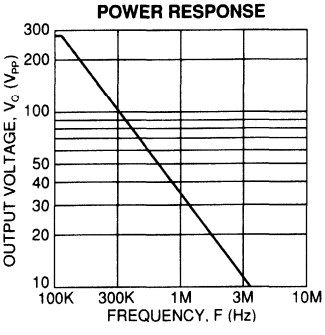
INPUT OFFSET VOLTAGE



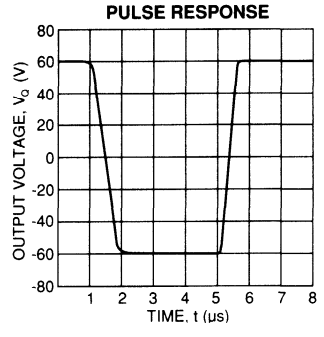
SLEW RATE VS. TEMP.



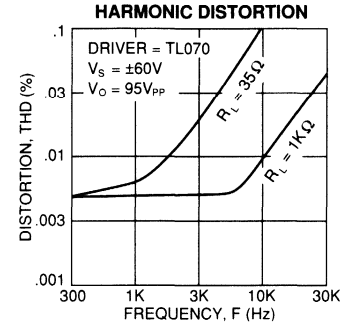
POWER RESPONSE



PULSE RESPONSE



HARMONIC DISTORTION



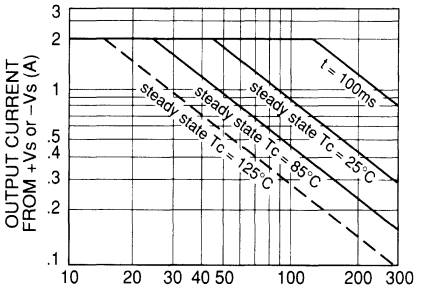
GENERAL

Please read the "General Operating Considerations" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

CURRENT LIMIT

For proper operation, the current limit resistor (R_{CL}) must be connected as shown in the external connection diagram. The minimum value is 0.33Ω with a maximum practical value of 47Ω. For optimum reliability the resistor value should be set as high as possible. The value is calculated as follows: $+I_L = .65/R_{CL} + .010$, $-I_L = .65/R_{CL}$.

SAFE OPERATING AREA (SOA)



SUPPLY TO OUTPUT DIFFERENTIAL VOLTAGE, Vs –Vo (V)

NOTE: The output stage is protected against transient flyback. However, for protection against sustained, high energy flyback, external fast-recovery diodes should be used.

COMPOSITE AMPLIFIER CONSIDERATIONS

Cascading two amplifiers within a feedback loop has many advantages, but also requires careful consideration of several amplifier and system parameters. The most important of these are gain, stability, slew rate, and output swing of the driver. Operating the booster amplifier in higher gains results in a higher slew rate and lower output swing requirement for the driver, but makes stability more difficult to achieve.

GAIN SET

$$R_G = [(Av-1) * 3.1K] - 6.2K$$

$$Av = \frac{R_G + 6.2K}{3.1K} + 1$$

The booster's closed-loop gain is given by the equation above. The composite amplifier's closed loop gain is determined by the feedback network, that is: –Rf/Ri (inverting) or 1+Rf/Ri (non-inverting). The driver amplifier's "effective gain" is equal to the composite gain divided by the booster gain.

Example: Inverting configuration (figure 1) with

R i = 2K, R f = 60K, R g = 0 :

Av (booster) = (6.2K/3.2K) + 1 = 3

Av (composite) = 60K/2K = – 30

Av (driver) = – 30/3 = –10

STABILITY

Stability can be maximized by observing the following guidelines:

1. Operate the booster in the lowest practical gain.
2. Operate the driver amplifier in the highest practical effective gain.
3. Keep gain-bandwidth product of the driver lower than the closed loop bandwidth of the booster.
4. Minimize phase shift within the loop.

A good compromise for (1) and (2) is to set booster gain from 3 to 10 with total (composite) gain at least a factor of 3 times booster gain. Guideline (3) implies compensating the driver as required in low composite gain configurations. Phase shift within the loop (4) is minimized through use of booster and loop compensation capacitors Cc and Cf when required. Typical values are 5pF to 33pF.

Stability is the most difficult to achieve in a configuration where driver effective gain is unity (ie; total gain = booster gain). For this situation, Table 1 gives compensation values for optimum square wave response with the op amp drivers listed.

DRIVER	C_{CH}	C_F	C_C	FPBW	SR
OP07	-	22p	22p	4kHz	1.5
741	-	18p	10p	20kHz	7
LF155	-	4.7p	10p	60kHz	>60
LF156	-	4.7p	10p	80kHz	>60
TL070	22p	15p	10p	80kHz	>60

For: R_F = 33K, R_I = 3.3K, R_G = 22K

Table 1: Typical values for case where op amp effective gain = 1.

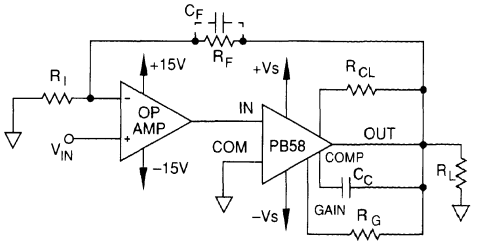


Figure 2. Non-inverting composite amplifier.

SLEW RATE

The slew rate of the composite amplifier is equal to the slew rate of the driver times the booster gain, with a maximum value equal to the booster slew rate.

OUTPUT SWING

The maximum output voltage swing required from the driver op amp is equal to the maximum output swing from the booster divided by the booster gain. The Vos of the booster must also be supplied by the driver, and should be subtracted from the available swing range of the driver. Note also that effects of Vos drift and booster gain accuracy should be considered when calculating maximum available driver swing.

WIDEBAND AMPLIFIER
WA01 • WA01A

FEATURES

- SUPER SLEW — 5000V/µsec
- HIGH BANDWIDTH — 100MHz
- OUTPUT CURRENT TO 400mA
- PIN COMPATIBILITY WITH 3554
- HIGH DC ACCURACY — ±5mV Vos
- LOW DISTORTION — 70dB at 100kHz

APPLICATIONS

- LINE DRIVERS
- DATA ACQUISITION SYSTEMS
- SAMPLE AND HOLD CIRCUITS
- VIDEO PROCESSING
- FUNCTION GENERATIONS
- ATE PIN DRIVER

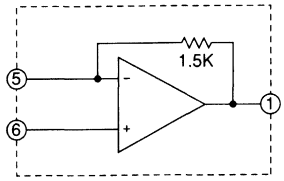
DESCRIPTION

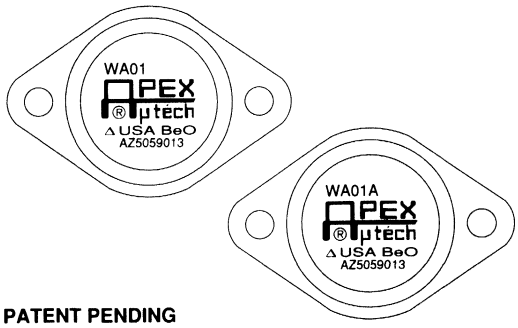
The WA01 uses low impedance push-pull circuits to achieve high speed amplification. The output node of each amplifier stage consists of two transistors, with the first transistor driving the signal in one direction and the second in the other direction. As a result, speed is enhanced, and a lower, much more linear output impedance, is obtained. This technique also exhibits low input impedance which is more compatible with high speed signal processing.

Unlike conventional op amps, the feedback resistor is included in the package. At 1.5K ohms, it provides a transimpedance function of 1.5V/1mA. Standard inverting and non-inverting op amp configurations may be implemented using fewer external components than would otherwise be required. The resultant feedback path is much shorter than when using a conventional external feedback element. As a result, summing node capacitance to ground is lower, and, thus, high frequency characteristics are very stable. To enhance the input characteristics of this wideband amplifier, sophisticated bias current cancellation and voltage offset trim networks have been added to the input stage.

This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability, minimize size, and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

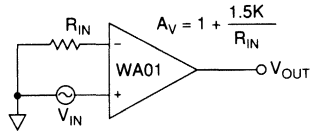
EQUIVALENT SCHEMATIC



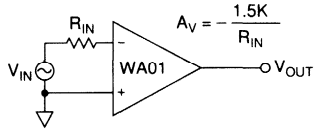


PATENT PENDING

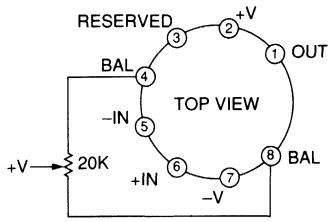
NONINVERTING GAIN



INVERTING GAIN



EXTERNAL CONNECTIONS



OFFSET POTENTIOMETER (OPTIONAL)

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$	32V
OUTPUT CURRENT, within SOA	400mA
POWER DISSIPATION, internal	10.5W
INPUT VOLTAGE, differential	±6V
INPUT VOLTAGE, common mode	$\pm V_S$
TEMPERATURE, pin solder - 10s	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE RANGE, storage	–65 to +150°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

SPECIFICATIONS

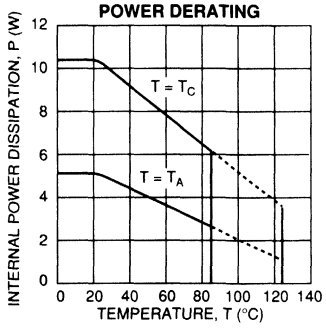
		WA01			WA01A			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
INPUT								
OFFSET VOLTAGE, Initial	T_C = 25°C		±4	±10		±.2	5	mV
OFFSET VOLTAGE, vs. Temperature	Full temperature range		15	50		10	25	µV/°C
OFFSET VOLTAGE, vs. Supply	T_C = 25°C		5	10		*	*	mV/V
OFFSET VOLTAGE, vs. Power	Full temperature range		20			10		µV/W
BIAS CURRENT, initial, +IN	T_C = 25°C		5	20		3	10	µA
BIAS CURRENT, vs. Supply	T_C = 25°C		.01			*		pA/V
INPUT IMPEDANCE, DC	T_C = 25°C		200			*		KΩ
INPUT CAPACITANCE	T_C = 25°C		6			*		pF
COMMON MODE VOLTAGE RANGE[3]	Full temperature range		$\pm V_S$–7.5		*	*		V
COMMON MODE REJECTION, DC[3]	Full temp. range, V_{CM} = ±5V	48	54		*	*		dB
POWER SUPPLY REJECTION, DC[3]	Full temp. range, V_S = 24 to 30	60	75					dB
GAIN								
ACCURACY	T_C = 25°C, F = DC		2	5		1	2	%
POWER BANDWIDTH	T_C = 25°C, I_O = .4A, V_O = $20V_{PP}$		40			*		MHz
	T_C = 25°C, I_O = .05A, V_O = $4V_{PP}$		80			*		MHz
GAIN FLATNESS	DC to 75MHz, A_V = –10		1			*		dB
OUTPUT								
VOLTAGE SWING[3]	T_C = 25°C, I_O = .4A	$\pm V_S$–4.5			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = .2A	$\pm V_S$–4			*			V
VOLTAGE SWING[3]	Full temp. range, I_O = .1A	$\pm V_S$–3.5			*			V
CURRENT, limit	T_C = 25°C		.6			*		A
SETTLING TIME to .1%	T_C = 25°C, 10V step		20			*		ns
SLEW RATE	T_C = 25°C		5000			*		V/µs
CAPACITIVE LOAD	Full temperature range, A_V = 1	22			*			pF
CAPACITIVE LOAD	Full temperature range, A_V = 30	47			*			pF
PROPAGATION DELAY	T_C = 25°C, A_V = 1		2.9			*		nS
POWER SUPPLY								
VOLTAGE	Full temperature range	±12	±15	±16		*	*	V
CURRENT, quiescent	T_C = 25°C		28	30		*	*	mA
THERMAL								
RESISTANCE, AC, junction to case[4]	Full temp. range, F > 60Hz		9	10		*	*	°C/W
RESISTANCE, DC, junction to case	Full temp. range, F < 60Hz		12	14		*	*	°C/W
RESISTANCE, junction to air	Full temp range		30			*		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25		+85	*		*	°C

NOTES: * The specification of WA01A is identical to the specification for WA01 in same category column to the left.

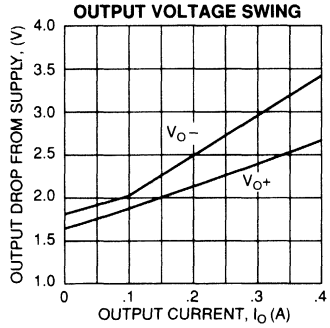
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. The power supply voltage for all specifications is the TYP rating unless noted as a test condition.
3. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.
4. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

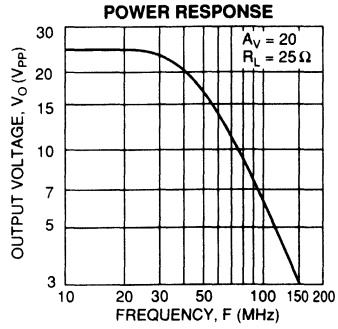
POWER DERATING



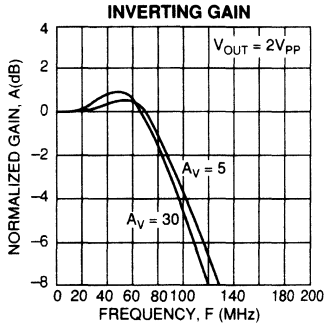
OUTPUT VOLTAGE SWING



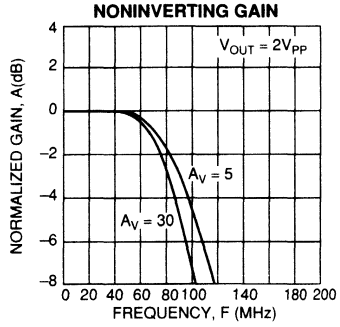
POWER RESPONSE



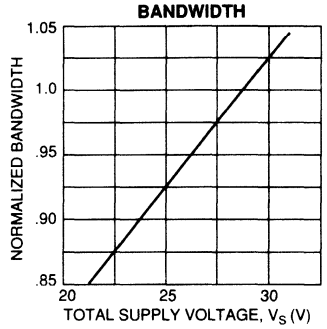
INVERTING GAIN



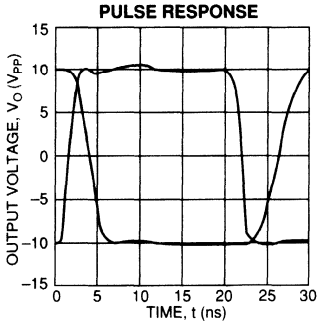
NONINVERTING GAIN



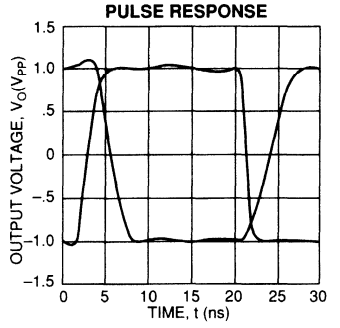
BANDWIDTH



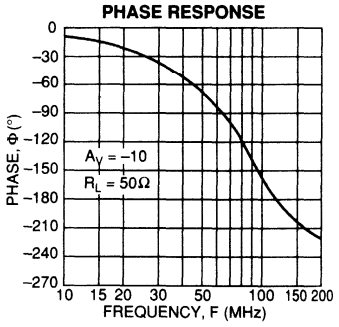
PULSE RESPONSE



PULSE RESPONSE



PHASE RESPONSE



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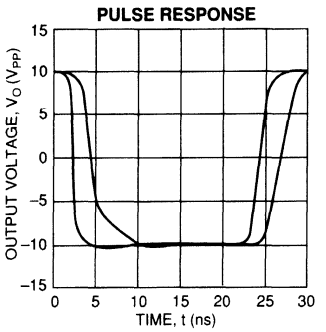
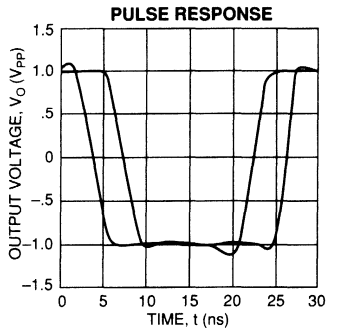
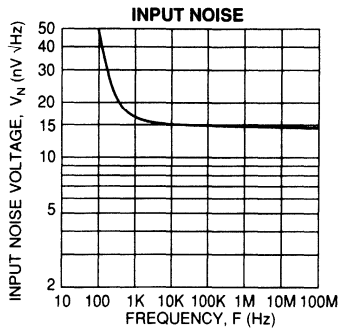


PULSE RESPONSE



INPUT NOISE



GENERAL

Please read the "General Operating Considerartions" section, which covers stability, supplies, heatsinking, mounting, current limit, SOA interpretation, and specification interpretation. Additional information can be found in the application notes. For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

BYPASSING OF SUPPLIES

Each rail must be bypassed to common with a tantalum capacitor in parallel with a ceramic capacitor directly connected from the power supply pins to the ground plane. The ceramic bypass capacitor should have leads as short as possible, be mounted as close to the supply pin as possible, and have a series resonant frequency above 200MHz, including lead inductance. A typical range would be 2.2 to 10μF for the tantalum and 500pF to 3000pF for the ceramic.

LEADS

Keep the output, supply, and bypass leads as short as possible. In the video frequency range, even a few inches of wire has significant inductance, raising the interconnection inpedance and limiting the output current slew rate. Furthermore, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz wire is recommended for high frequency use with low losses.

GROUNDING

Single point grounding of the input resistors and input signal to a common ground plane will prevent undesired current feedback which can cause errors and/or instabilities. Also, the case is electrically isolated (floating) with respect to the internal circuit. It is recommended that the case be connected to the same common ground plane as the inputs.

SAFE OPERATING AREA (SOA)

The bipolar output stage of this wideband amplifier has two distinct limitations:

1. The internal current limit limits maximum available output current.
2. The junction temperature of the output devices.

Compliance within the power derating curve guarantees maximum junction temperature is met.

CURRENT LIMIT

Internal current limit is set using a 1.2Ω ±20% resistor and one transistor VBE drop. Nominal current limit at T_C = 25°C is:

$$I_{LIM} = V_{BE}/R_{CL}; .54A = .65V/1.2\Omega.$$

Temperature variance of the current limit is dominated by the VBE temperature coefficient of –2mV/°C. For a case temperature of +85°C, the nominal current limit is:

$$.442A = [.65 - (60°C)(2mV/°C)]/[1.2\Omega].$$

GAIN SETTING

Unlike other APEX amplifiers, the WA01's feedback resistor is inside the package. This reduces external part count as well as increases performance. To determine the value of the resistor required to achieve the desired gain, the following formulas are necessary:

NONINVERTING	$R_{IN} = 1.5K/(A_V-1)$
INVERTING	$R_{IN} = 1.5K/A_V$

BALANCE CONTROL

The voltage offset of the WA01 is laser trimmed at the factory. To externally zero residual errors in applications where offset is critical, a 20K ohm potentiometer may be installed between pins 4 and 8, and the wiper arm connected to the positive supply. If the optional adjust provision is not used, and setting time is important, tie pin 8 to AC ground with 100–150pF.

STABILITY

The use of an internal feedback resistor of low impedance insures ease of use and stability of the WA01. Additionally, the architecture provides for a constant bandwidth at different gain settings without the need for external compensation. Although the WA01 is stable and well behaved at high frequency, a good PC layout is essential for optimum performance. A layout that keeps inductances, capacitances, and trace lengths to a minimum will prevent oscilliations. To avoid peaking at high frequency when driving a capacitive load, a small resistor (1 to 22 ohms) may be placed between the output and the load to lower the Q of any parasitic resonant circuit that might occur.

FEATURES

- HIGH OUTPUT CURRENT — A DC, 1.5A PEAK
- WIDE SUPPLY VOLTAGE RANGE — ±5 TO ±15V
- SEPARATE FRONT-END AND OUTPUT SUPPLIES
- LOW SATURATION VOLTAGE — 3.5V
- HIGH SLEW RATE — 10,000 V/µs @ 1A
  15,000 V/µs @ 0.5A
- LOW QUIESCENT CURRENT — 30mA
- SLEEP MODE CONTROL — 2.5mA
- HIGH FULL POWER BANDWIDTH — 70MHz

APPLICATIONS

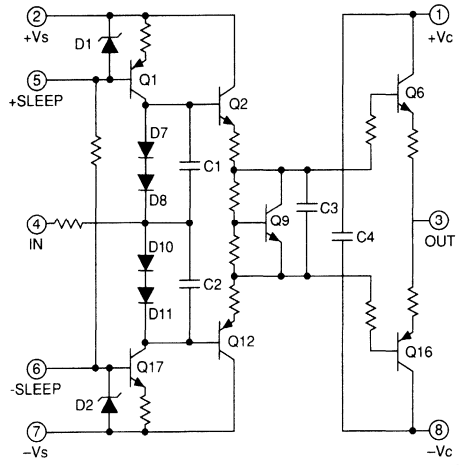
- LASER DIODE DRIVE
- GATE DRIVE FOR LARGE FETS
- SEMICONDUCTOR TESTING

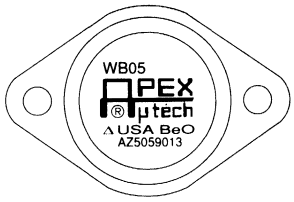
DESCRIPTION

The WB05 is a high slew rate, high current, wideband buffer capable of internal power dissipation of up to 15 watts. It provides high output currents of 1A continuous, and 1.5A peaks, under pulsed conditions. Typical circuit configuration using the WB05 will be a composite amplifier arrangement. Therefore, input capacitance has been minimized to reduce the drive requirements from the driver amplifier. A sleep mode feature has been incorporated to lower quiescent current during standby modes for battery powered applications.

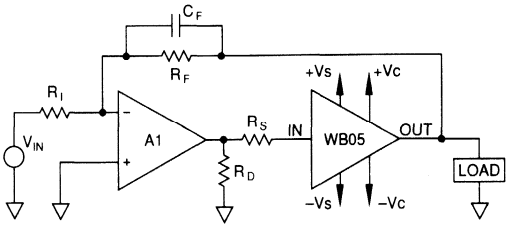
This hybrid circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers may void the warranty.

EQUIVALENT SCHEMATIC





TYPICAL APPLICATION

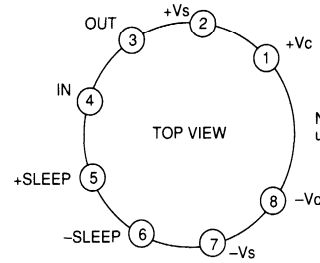


COMPOSITE AMPLIFIER CONFIGURATION

In this composite amplifier configuration, R_F and R_I should be kept as low as possible consistent with input impedance and gain requirements. Using low value resistors prevents high impedance nodes from acting as antennas, which could cause output signals to be picked up as positive feedback and result in oscillations. Low values also keep input and stray capacitance time constants low, for high speed and improved settling time. C_F is used to optimize settling time by compensating for input and stray capacitances. R_D (typically 500Ω) reduces the ouput impedance of A1 while R_S (typically 5-30Ω) provides damping for strays. The driver op amp must be capable of supplying adequate phase margin for itself and the WB05 at the closed loop gain used.

The driver amplifier also must be capable of providing enough current to drive R_D as well as charge the WB05's input and any other stray capacitances, at the intended slew rate. The phase shift introduced by the WB05 will increase the minimum required gain of the driver amplifier to guarantee stability. If the driver amplifier is a transimpedance amplifier, the inverting configuration shown will typically exhibit better slew rate and rise time than a noninverting configuration. This effect is due to the nature of the front end of most transimpedance amplifiers and the current available for turning on the output stage in the two different configurations. The case of the WB05 should be grounded if possible.

EXTERNAL CONNECTIONS



NOTE: If SLEEP pins are unused, leave open

ABSOLUTE MAXIMUM RATINGS

SUPPLY VOLTAGE, $+V_S$ to $-V_S$, $+V_C$ to $-V_C$	30V
OUTPUT CURRENT, within SOA	1.5A
POWER DISSIPATION, internal at T_C = 25°C	15W
INPUT VOLTAGE RANGE	$\pm V_S$
TEMPERATURE, pins solder—10 sec max	300°C
TEMPERATURE, junction[1]	175°C
TEMPERATURE, storage	–65 to 175°C
OPERATING TEMPERATURE RANGE, case	–25 to +85°C

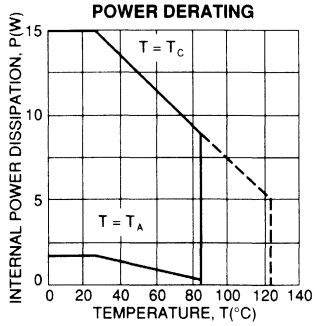
SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE, initial			30	100	mV
OFFSET VOLTAGE, vs. temperature			100	500	µV/°C
BIAS CURRENT	V_{IN} = 0V		150	700	µA
INPUT CAPACITANCE			4		pF
INPUT VOLTAGE RANGE	I_{IN} < 1mA	$\pm V_S \mp 2$	$\pm V_S \mp 1.7$		V
INPUT OVERDRIVE CURRENT	$V_{IN} = +V_S$ or $V_{IN} = -V_S$		5	7	mA
PHASE SHIFT	f = 40MHz, R_L = 10Ω		8		°
	f = 150MHz, R_L = 10Ω		25		°
OUTPUT					
SATURATION VOLTAGE, (V_C-V_O)	I_O = 0.5A, $V_C = V_S - 3$	2.2	1.8		V
	I_O = 1A, $V_C = V_S - 3$	3.5	2.7		V
	I_O = 1A, $V_C = V_S$	6.5	6		V
OUTPUT CURRENT, continuous				1	A
OUTPUT CURRENT, pulsed	50% duty cycle, 10 ms pulse			1.5	A
SLEW RATE	R_L = 10Ω, V_{IN} = 15V/ns	8	10		V/ns
POWER BANDWIDTH	$V_C = V_S = \pm 15$, R_L = 20Ω	50	70		MHz
POWER BANDWIDTH	$V_C = V_S = \pm 5$, R_L = 20Ω		10		MHz
SETTLING TIME	8V step, R_L = 8Ω, to 0.1%		60		ns
	2V step, R_L = 10Ω, to 0.1%		22		ns
SMALL SIGNAL BANDWIDTH	$V_C = V_S = \pm 15$		250		MHz
OUTPUT IMPEDANCE	$V_C = V_S = \pm 15$, f = 1MHz		2		Ω
SMALL SIGNAL RISETIME	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		1.7		ns
SMALL SIGNAL PROP. DELAY	1V step, R_L = 10, $\pm V_S = \pm V_C$ = 15V		0.8		ns
DC GAIN	R_L = 10Ω, $\pm V_S = \pm V_C$ = 15V	0.82	0.87	0.93	V/V
POWER SUPPLY					
VOLTAGE (V_C, V_S)	Full temperature range	±5	±15	±15	V
QUIESCENT CURRENT			30	35	mA
	Sleep mode		2.5	3.5	mA
THERMAL					
RESISTANCE, AC junction to case[3]	Full temp. range, f > 60Hz		6	7.2	°C/W
RESISTANCE, DC junction to case	Full temp. range, f < 60Hz		8.3	10	°C/W
RESISTANCE, junction to air	Full temperature range		30		°C/W
TEMPERATURE RANGE, case	Meets full range specifications	–25	25	85	°C

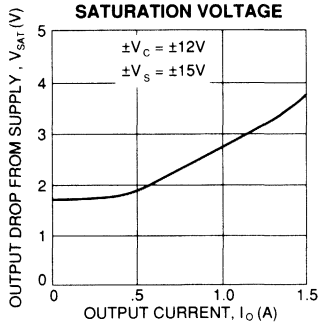
NOTES: 1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.
2. Case temperature is 25°C and the power supply voltage for all specifications is the TYP rating otherwise noted as a test condition. Case is grounded for all specifications.
3. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

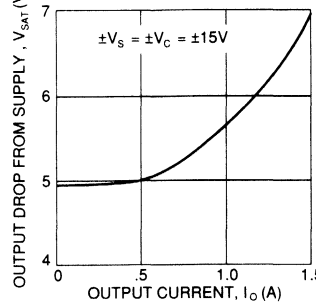
POWER DERATING



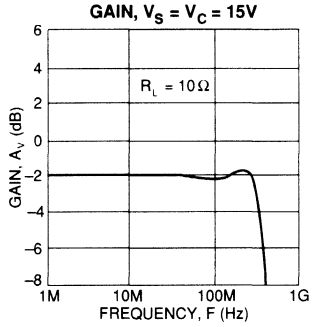
SATURATION VOLTAGE



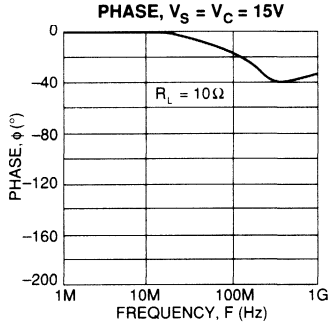
SATURATION VOLTAGE



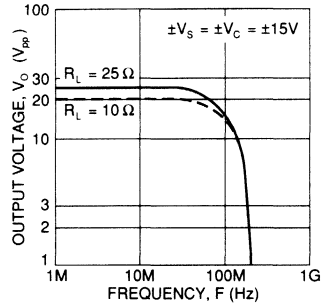
GAIN, $V_S = V_C = 15V$



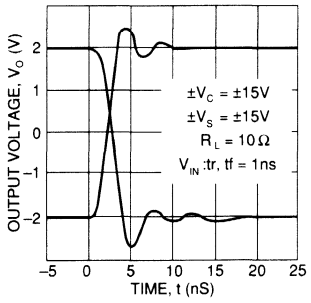
PHASE, $V_S = V_C = 15V$



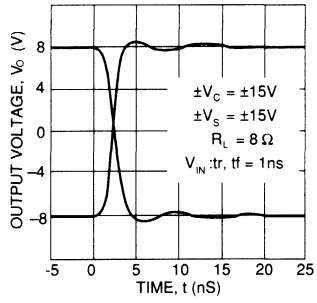
POWER RESPONSE



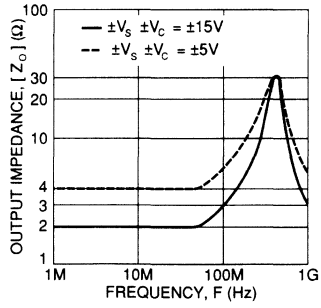
SMALL SIGNAL PULSE RESPONSE



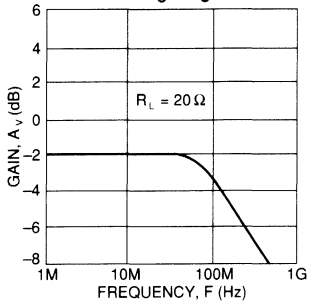
LARGE SIGNAL PULSE RESPONSE



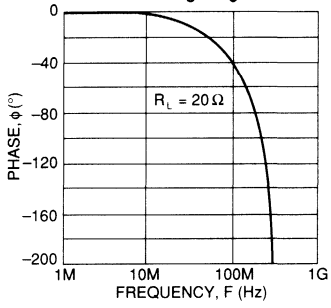
OUTPUT IMPEDANCE



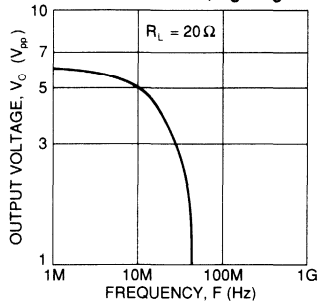
GAIN, $V_S = V_C = 5V$



PHASE, $V_S = V_C = 5V$



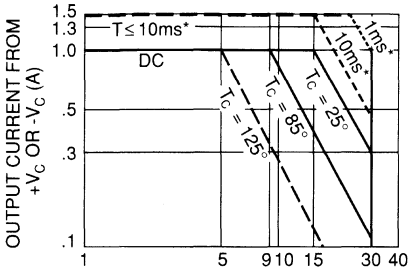
POWER RESPONSE, $V_S = V_C = 5V$



GENERAL

Please read the "General Operating Considerations" section. Additional information can be found in AN #15, "Applying the Ultra-fast WB05." For information on the package outline, heatsinks, and mounting hardware, consult the "Accessory and Package Mechanical Data" section of the handbook.

SAFE OPERATING AREA (SOA)



INTERNAL VOLTAGE PROP SUPPLY TO OUTPUT V_C -V_O (V)
*Pulsed operation: duty cycle less than or equal to 50%.

USE OF SUPPLY PINS FOR BOOST

The output stage supply voltage can be reduced or have series resistors installed to reduce power dissipation in the buffer if required. Output stage supply pins should be bypassed on the buffer side of the series resistors if they are used. Reduced output supplies (or increased input supplies) will also improve output voltage swing to the rail (V_{SAT}).

HIGH Z_L AND/OR C_L

The WB05 has been optimized for high current/low impedance loads. With large load impedances (Z_L > 100Ω) or high capacitive loading (C_L > 150pF), the buffer may show peaking in the small signal response. If required, a series R-C network of 22Ω and 68 pF can be connected from the output to ground to flatten the response.

CURRENT LIMIT

The scheme shown in Figure 1 is rather slow but is cost effective if the WB05 must be operated in a system where available supply voltages exceed ±15V or when it is desired to reduced power dissipation in the WB05 by running the output stage power supplies (±V_C) at a lower voltage. This circuit provides both regulated voltage and output current limit.

The circuit shown in Figure 2 takes advantage of the WB05 sleep pins. With Figure 2 there is a 10µs delay until the current is limited.

SLEEP MODE

The WB05 quiescent current will drop from ≈30mA to ≈2.5mA when both sleep pins are pulled within 100mV of their respective supply pins. A typical circuit for implememtation is shown in Figure 3.

COMPOSITE AMPLIFIER CONSIDERATIONS

When the WB05 is used as shown in the "TYPICAL APPLICATION" figure, the phase shift of the WB05 is inside the feedback loop for A1 and must be considered for stability calculations. See AN #15.

SLEW RATE

The WB05 output can slew no faster than its input is driven. To achieve high input slew rates, keep driving impedances as low as practical. Note that any strays from layout will add to the input capacitance of the buffer and may form a pole with driving network resistance or driver output impedance.

LAYOUT AND BYPASS

The WB05 requires good VHF/UHF lead dress and layout due to its 250MHz small signal bandwidth. Output currents of up to 1.5A and high dV/dt at the output can cause unwanted inductive and capacitive coupling, respectively, in your layout. Recommended power supply bypassing is as follows:

Vc = Vs: On each supply rail, V+ and V-, place in parallel the following capacitors:
C1, C4 = 330 to 1000 pF ceramic capacitor
C2, C5 = 0.01 to 0.033 µF ceramic capacitor
C3, C6 = 2.2 to 6.8 µF low ESR tantalum electrolytic

Vc ≠ Vs: On each Vc supply rail, +Vc and -Vc, place in parallel the following capacitors:
C1, C6 = 330 to 1000 pF ceramic capacitor
C2, C7 = 0.01 to 0.033 µF ceramic capacitor
C3, C8 = 2.2 to 6.8 µF low ESR tantalum electrolytic

On each Vs supply rail, +Vs and -Vs, place in parallel the following capacitors:
C4, C9 = 0.01 to 0.033 µF ceramic capacitor
C5, C10 = 330 to 1,000pF ceramic capacitor

All capacitors must be as close to the buffer supply pins as possible, with short leads (1/8" to 1/4") and/or short, wide PCB traces to minimize stray inductances.

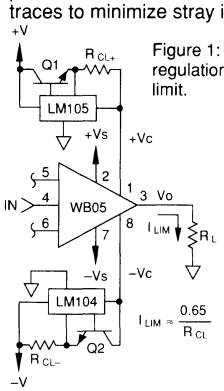


Figure 1: Output voltage regulation and current limit.

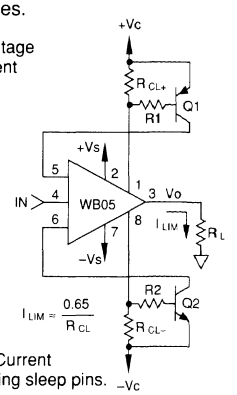


Figure 2: Current limiting using sleep pins.

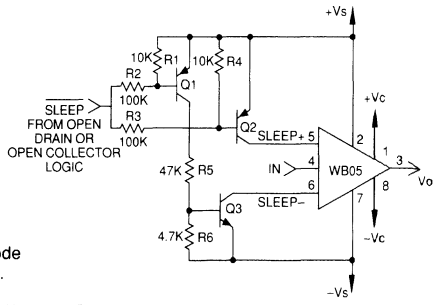


Figure 3: Sleep mode interface.

DC/DC CONVERTERS

This section provides product specifications for Apex's new line of DC/DC Converters as of September 1991. As this product line expands, new product data sheets will become available.

For Up-to-Date
Product Information
Call the
Apex Product Literature Hotline
(800) 448-1025
Toll Free

NOTES:

20 WATT DC-DC CONVERTER

DB2805S • DB2805SA

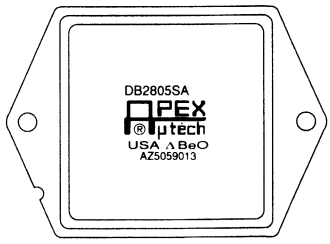
APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

HI-REL DESIGN

- **WELDED HERMETIC PACKAGE**
- **LOW INTERNAL TEMPERATURE GRADIENTS**
- **LOW COMPONENT COUNT**
- **ALL CERAMIC CAPACITORS**
- **WAVE SOLDERABLE PACKAGE**

OTHER FEATURES

- **NO DERATING — -55 to +85°C and -55 to +125°C**
- **WIDE SUPPLY RANGE — 15 to 50V**
- **HIGH POWER DENSITY — 20W/IN³**
- **HIGH ISOLATION — 500V**



PATENT PENDING

DESCRIPTION

The DB2805S(A) has been created to provide a reliable DC/DC Converter specified over the military temperature range. This has been achieved using a new package, rather than pushing the envelope on existing DC/DC Converter packages. A 12-pin MO-127 High Profile Power Dip™, pioneered by Apex for Power Amplifiers up to 500W, provides very low thermal gradients, rugged hermeticity and high voltage isolation.

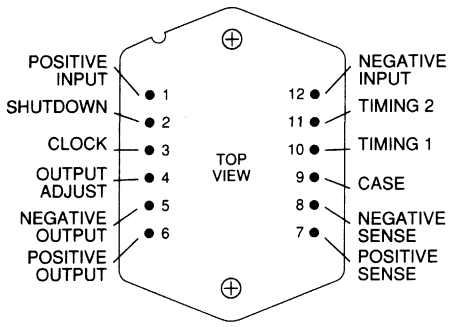
To further enhance reliability, the internal component count has been kept low. What is more, no tantalum or electrolytic capacitors are used in this design, a major cause of low MTBF in DC/DC Converters.

The sophisticated DB 2805S(A) features remote shutdown, kelvin sense, slaveability, and indefinite short circuit protection. It uses a push-pull topology operated in the feed forward, current mode. The typical switching frequency is 500 kHz. A π type input filter is included in order to reduce the peak to peak input ripple current.

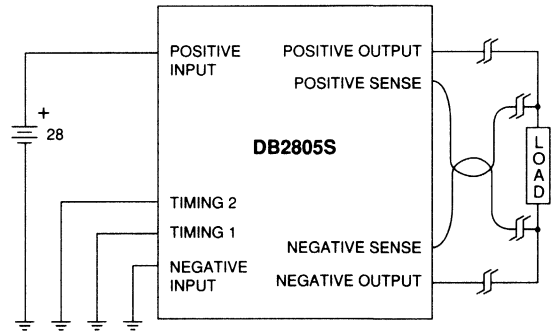
This hybrid converter utilizes thick film (cermet) resistors, ceramic capacitors, miniature magnetics and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures.

The 12-pin MO-127 High Profile Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Do not use thermally conductive electrical insulators between package and heatsink.

EXTERNAL CONNECTIONS

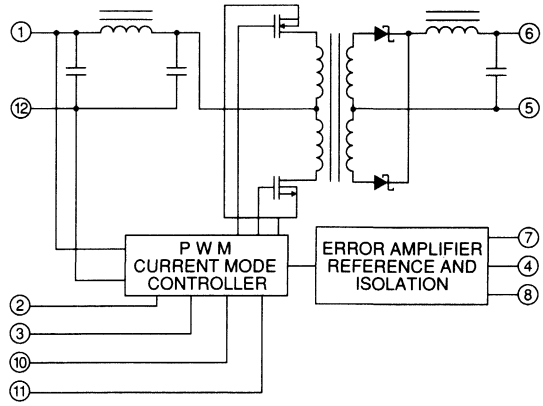


TYPICAL APPLICATION



The above diagram shows the remote sense feature which reduces V_O errors due to resistive drops in long power supply lines. This diagram also shows the connection for non-synchronized operation.

BLOCK DIAGRAM

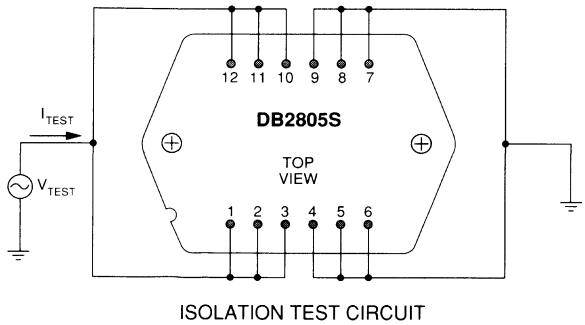


ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE RANGE	0 – 50V
OUTPUT CURRENT	4A
POWER DISSIPATION	15W
TEMPERATURE, Storage	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	DB2805S MIN	DB2805S TYP	DB2805S MAX	DB2805SA MIN	DB2805SA TYP	DB2805SA MAX	UNITS
STEADY STATE CHARACTERISTICS								
OUTPUT VOLTAGE	V_{IN}; 16 - 40 Vdc	5.00	5.05	5.10	*	*	*	Vdc
OUTPUT CURRENT		0.40		4	*		*	Amps
EFFICIENCY	V_{IN}; 16-40, I_{OUT} = 4 Amps	64	72	76	66	72	76	%
RIPPLE VOLTAGE	Bandwidth DC → 1MHz	20	60	70	20	50	60	mV
OUTPUT POWER			20	20.8		*	*	Watts
LINE REGULATION	V_{IN}; 16 to 40 Volts		±0.2	±1.0		±0.1	±0.5	%
LOAD REGULATION	I_{OUT}; 400mA to 4 Amps		±2.0	±3.0		±1.0	±2.0	%
INPUT VOLTAGE RANGE	I_{OUT} = 4 Amps	17	28	40	16	28	40	Vdc
INPUT CURRENT	V_{IN}; 16 to 40 Volts	1.78	0.95	0.75	*	*	*	Amps
INPUT RIPPLE CURRENT	V_{IN}; 16 to 40 Volts	20	60	70	*	*	*	mA p-p
JUNCTION TEMPERATURE RISE			10	22		*	*	°C
TEMPERATURE RANGE, case	I_{OUT} = 4.0 Amps	–55	25	85	–55	25	125	°C
QUIESCENT CURRENT	V_{IN}; 16 to 40 Volts; V_{PIN2}; 5V		60	100		*	*	mA
ISOLATION CHARACTERISTICS								
LEAKAGE RESISTANCE	(See Figure 1 DC)	100			*			MΩ
LEAKAGE CAPACITANCE	(See Figure 1, F = 10kHz	20	35		*	*		pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE	V_{IN} Slew Rate = .1V/µs							
OUTPUT VOLTAGE	V_{IN}; 17 → 40 Volts		+700			*		mVpk
RECOVERY TIME	V_{IN}; 17 → 40 Volts		800			*		µsec
OUTPUT VOLTAGE	V_{IN}; 40 → 17 Volts		–800			*		mVpk
RECOVERY TIME	V_{IN}; 40 → 17 Volts		800			*		µsec
LOAD STEP RESPONSE	I_{OUT} Slew Rate = 1.5A/µs							
OUTPUT VOLTAGE	I_O; 2 → 4 Amps		–700			*		mVpk
RECOVERY TIME	I_O; 2 → 4 Amps		200			*		µsec
OUTPUT VOLTAGE	I_O; 4 → 2 Amps		+800			*		mVpk
RECOVERY TIME	I_O; 4 → 2 Amps		200			*		µsec
START-UP OVERSHOOT	V_{IN} ; 0 → 28 Volts		0.25			*		Vdc
SHUTDOWN DELAY	V_{PIN2} ; 0 → 5 Volts		40			*		µsec
SHUTDOWN RECOVERY	V_{PIN2} ; 5 → 0 Volts		10			*		msec

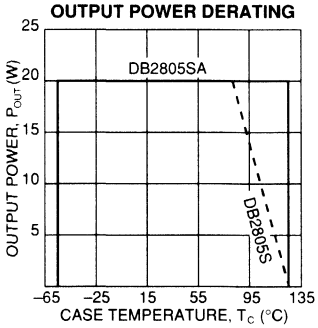


ISOLATION TEST CIRCUIT

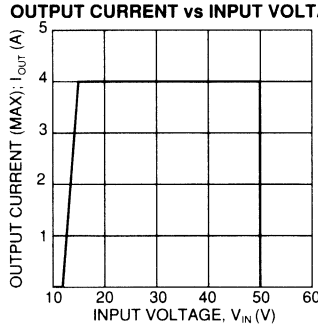
NOTES:
* The specification of DB2805SA is identical to the specification for DB2805S in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF. For guidance, refer to the heatsink data sheet.
2. Unless otherwise stated T_C = 25°, $V_{IN} = V_{PIN12} - V_{PIN1}$ = 28V, I_{OUT} = 4 Amps.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

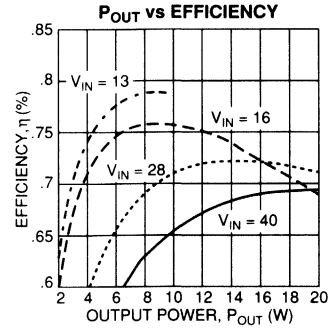
OUTPUT POWER DERATING



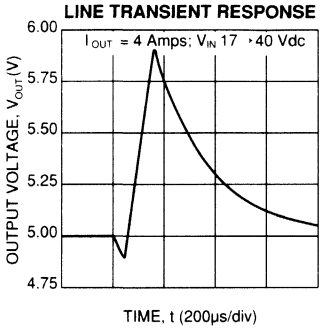
OUTPUT CURRENT vs INPUT VOLTAGE



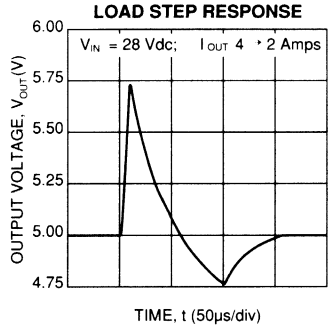
P_{OUT} vs EFFICIENCY



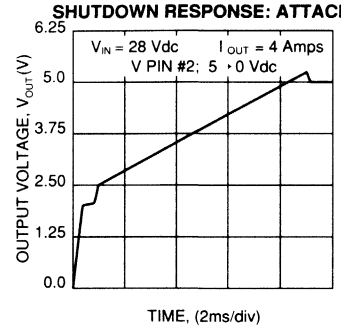
LINE TRANSIENT RESPONSE



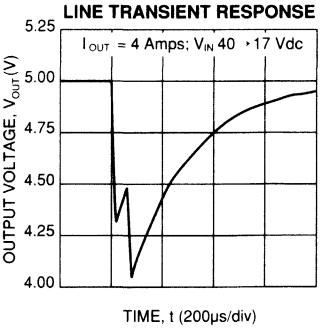
LOAD STEP RESPONSE



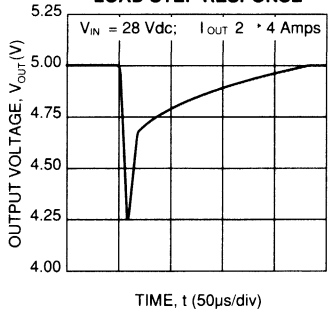
SHUTDOWN RESPONSE: ATTACK



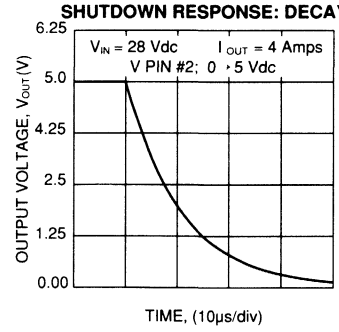
LINE TRANSIENT RESPONSE



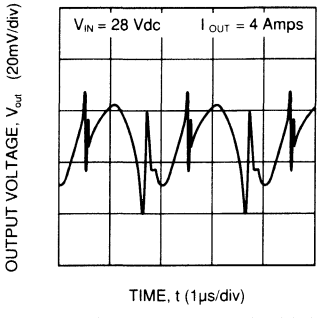
LOAD STEP RESPONSE



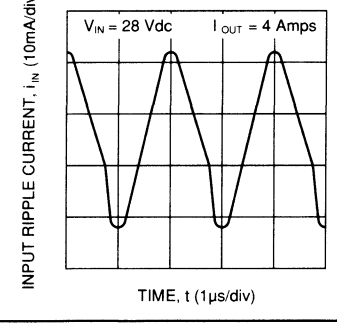
SHUTDOWN RESPONSE: DECAY



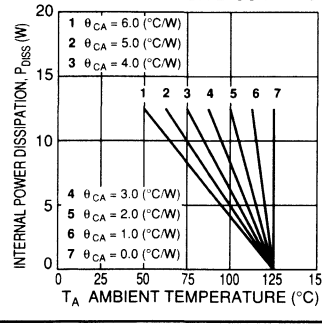
OUTPUT VOLTAGE RIPPLE



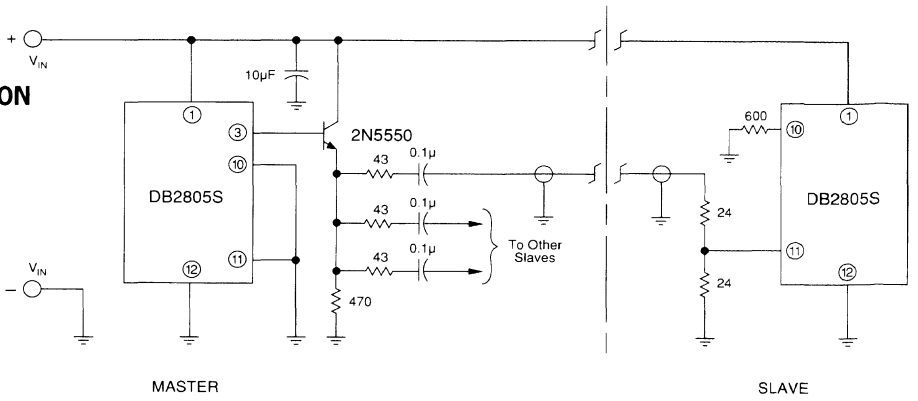
INPUT CURRENT RIPPLE



INTERNAL POWER DISSIPATION



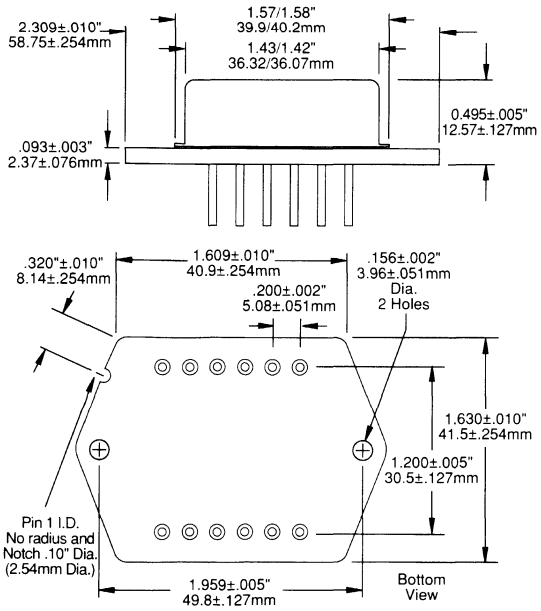
MULTIPLE CONVERTER SYNCHRONIZATION



Operating two or more DB2805S converters as shown at right will synchronize the units to a common switching frequency. This type of operation will help to eliminate the possibility of additional harmonics being generated as a result of different switching frequencies from multiple converters.

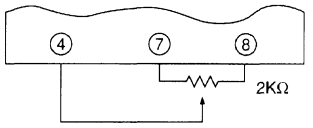
As with all high frequency control systems, great care should be taken in the layout of this circuit. A separate path to ground should be used for the power ground(s) pin 12 and for signal grounds pins 10 and 11. The transistor used to buffer the clock output pin 4 should be mounted as close as possible to the master circuit. The 10µF capacitor should be a good high frequency type and should be mounted as close as possible to the transistor. Shielded cable must be used to distribute the clock information to the slave units to prevent other noise from being coupled into pin 11.

PACKAGE OUTLINE DIMENSIONS MO-127 HIGH PROFILE

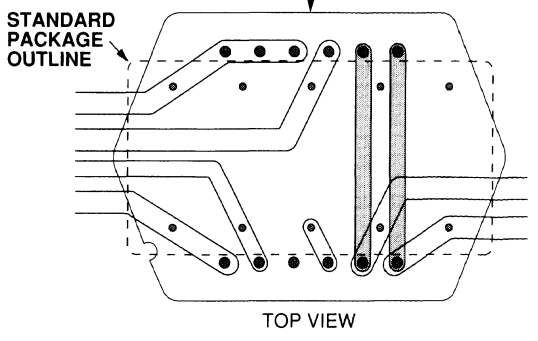


V_{ADJUST}

A 2kΩ potentiometer connected as shown below gives the ability to trim the output voltage between 4.5 and 5.5 volts. The nominal input impedance is 50Ωs measured between pins 4 and 7. An external reference and error amplifier can also provide input to this pin if an even higher degree of output voltage accuracy is desired.



DB2805S PACKAGE OUTLINE



The above diagram shows the form and function adaptability of the DB2805S with the industry standard pinout. The connections shown denote the use of the DB2805S without the synchronization or remote sense features, which are unique to the Apex product.

22.5 WATT DC-DC CONVERTER

DB2812S • DB2812SA

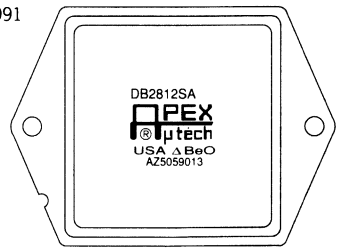
APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

PRELIMINARY

PRODUCT AVAILABLE SEPT. 1, 1991

HI-REL DESIGN

- **WELDED HERMETIC PACKAGE**
- **LOW INTERNAL TEMPERATURE GRADIENTS**
- **LOW COMPONENT COUNT**
- **ALL CERAMIC CAPACITORS**
- **WAVE SOLDERABLE PACKAGE**



PATENT PENDING

OTHER FEATURES

- **NO DERATING — -55 to +85°C and -55 to +125°C**
- **WIDE SUPPLY RANGE — 12 to 50V**
- **HIGH POWER DENSITY — 22.5W/IN³**
- **HIGH ISOLATION — 500V**

DESCRIPTION

The DB2812S(A) has been created to provide a reliable DC/DC Converter specified over the military temperature range. This has been achieved using a new package, rather than pushing the envelope on existing DC/DC Converter packages. A 12-pin MO-127 High Profile Power Dip™, pioneered by Apex for Power Amplifiers up to 500W, provides very low thermal gradients, rugged hermeticity and high voltage isolation.

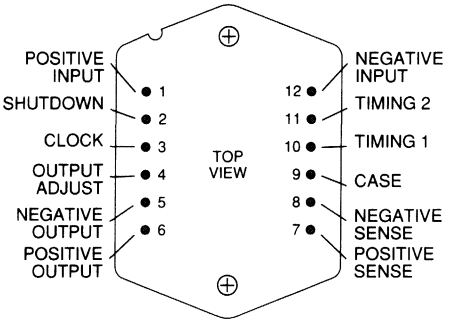
To further enhance reliability, the internal component count has been kept low. What is more, no tantalum or electrolytic capacitors are used in this design, a major cause of low MTBF in DC/DC Converters.

The sophisticated DB 2812S(A) features remote shutdown, kelvin sense, slaveability, and indefinite short circuit protection. It uses a push-pull topology operated in the feed forward, current mode. The typical switching frequency is 500 kHz. A π type input filter is included in order to reduce the peak to peak input ripple current.

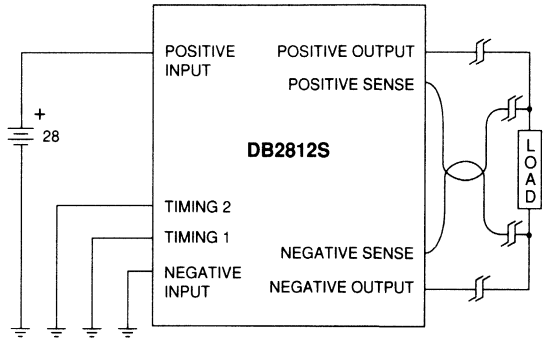
This hybrid converter utilizes thick film (cermet) resistors, ceramic capacitors, miniature magnetics and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures.

The 12-pin MO-127 High Profile Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Do not use thermally conductive electrical insulators between package and heatsink.

EXTERNAL CONNECTIONS

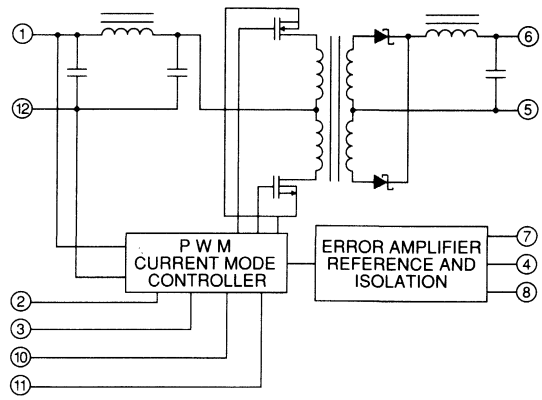


TYPICAL APPLICATION



The above diagram shows the remote sense feature which reduces V_O errors due to resistive drops in long power supply lines. This diagram also shows the connection for non-synchronized operation.

BLOCK DIAGRAM

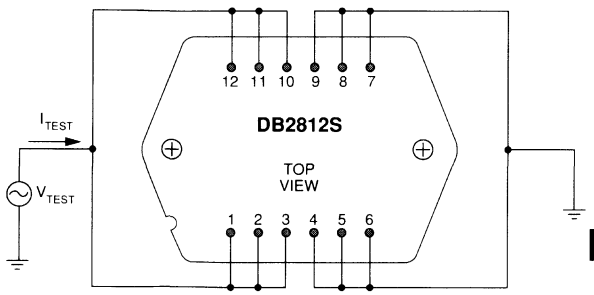


ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE RANGE	0 – 50V
OUTPUT CURRENT	1.88A
POWER DISSIPATION	15W
TEMPERATURE, Storage	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C

SPECIFICATIONS

PARAMETER	TEST CONDITIONS[2]	DB2812S MIN	DB2812S TYP	DB2812S MAX	DB2812SA MIN	DB2812SA TYP	DB2812SA MAX	UNITS
STEADY STATE CHARACTERISTICS								
OUTPUT VOLTAGE	V_{IN}; 16 - 40 Vdc	12.00	12.05	12.10	*	*	*	Vdc
OUTPUT CURRENT		0.18		1.88	*		*	Amps
EFFICIENCY	V_{IN}; 17-40, I_{OUT} = 1.88 Amps	66	73	78	68	74	79	%
RIPPLE VOLTAGE	Bandwidth DC → 1MHz	50	80	100	*	*	*	mV
OUTPUT POWER			22.5	22.7		*	*	Watts
LINE REGULATION	V_{IN}; 17 to 40 Volts		±0.2	±1.0		±0.1	±0.5	%
LOAD REGULATION	I_{OUT}; 180mA to 1.88 Amps		±1.0	±2.0		±0.1	±0.5	%
INPUT VOLTAGE RANGE	I_{OUT} = 1.88 Amps	15	28	40	15	28	50	Vdc
INPUT CURRENT		0.77	1.10	2.05	0.61	1.09	2.05	Amps
INPUT RIPPLE CURRENT		20	60	70	*	*	*	mA p-p
JUNCTION TEMPERATURE RISE			10	22		*	*	°C
TEMPERATURE RANGE, case	I_{OUT} = 1.88 Amps	–55	25	85	–55	25	125	°C
QUIESCENT CURRENT	V_{IN}; 16 to 40 Volts; V_{PIN2}; 5V		60	100		*	*	mA
ISOLATION CHARACTERISTICS								
LEAKAGE RESISTANCE	(See Figure 1 DC)	100			*			MΩ
LEAKAGE CAPACITANCE	(See Figure 1, F = 10kHz	20	35		*	*		pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE	V_{IN} Slew Rate = .1V/µs							
OUTPUT VOLTAGE	V_{IN}; 17 → 40 Volts		+1300			*		mVpk
RECOVERY TIME	V_{IN}; 17 → 40 Volts		800			*		µsec
OUTPUT VOLTAGE	V_{IN}; 40 → 17 Volts		–500			*		mVpk
RECOVERY TIME	V_{IN}; 40 → 17 Volts		600			*		µsec
LOAD STEP RESPONSE	I_{OUT} Slew Rate = 0.7A/µs							
OUTPUT VOLTAGE	I_O; .94 → 1.88 Amps		–1500			*		mVpk
RECOVERY TIME	I_O; .94 → 1.88 Amps		150			*		µsec
OUTPUT VOLTAGE	I_O; 1.88 → 0.94 Amps		+1700			*		mVpk
RECOVERY TIME	I_O; 1.88 → 0.94 Amps		300			*		µsec
START-UP OVERSHOOT	V_{IN} ; 0 → 28 Volts		0.25			*		Vdc
SHUTDOWN DELAY	V_{PIN2} ; 0 → 5 Volts		40			*		µsec
SHUTDOWN RECOVERY	V_{PIN2} ; 5 → 0 Volts		10			*		msec

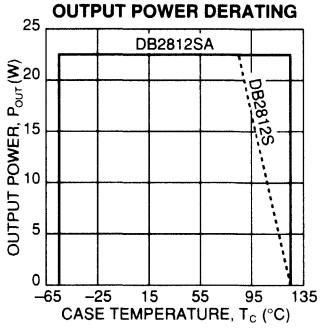


ISOLATION TEST CIRCUIT

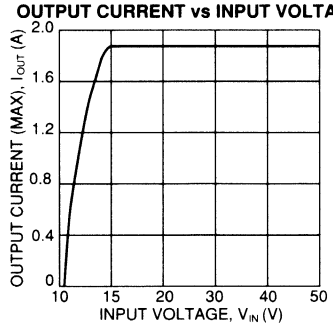
NOTES:
* The specification of DB2812SA is identical to the specification for DB2812S in applicable column to the left.
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF. For guidance, refer to the heatsink data sheet.
2. Unless otherwise stated T_C = 25°, $V_{IN} = V_{PIN12} - V_{PIN1}$ = 28V, I_{OUT} = 1.875 Amps.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

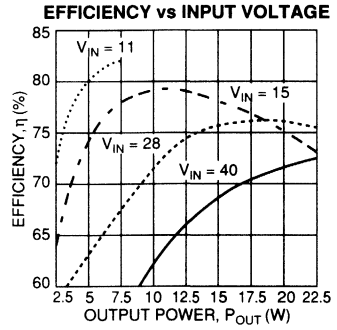
OUTPUT POWER DERATING



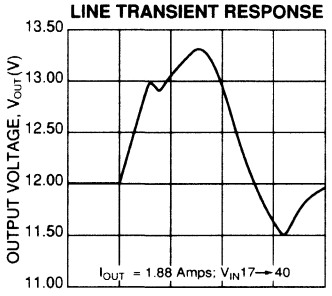
OUTPUT CURRENT vs INPUT VOLTAGE



EFFICIENCY vs INPUT VOLTAGE

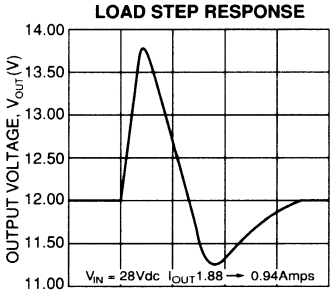


LINE TRANSIENT RESPONSE



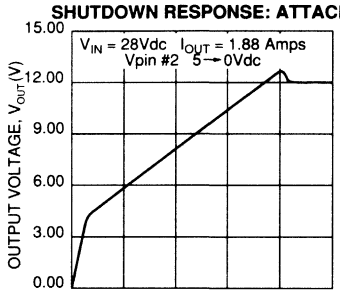
TIME, t (200µs/div)

LOAD STEP RESPONSE



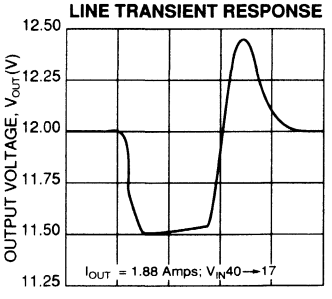
TIME, t (50µs/div)

SHUTDOWN RESPONSE: ATTACK



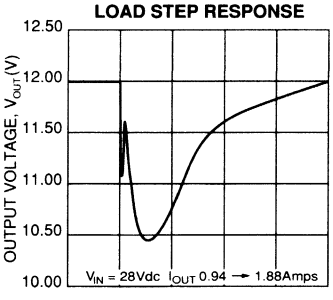
TIME, t (5ms/div)

LINE TRANSIENT RESPONSE



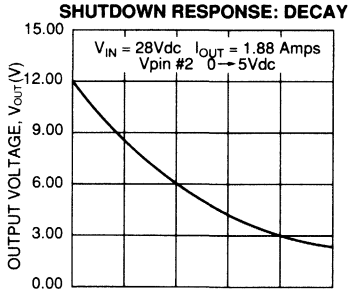
TIME, t (200µs/div)

LOAD STEP RESPONSE



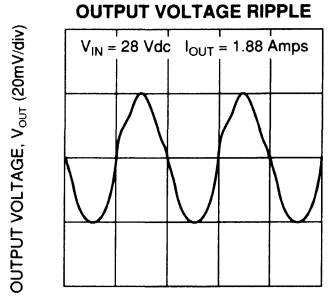
TIME, t (100µs/div)

SHUTDOWN RESPONSE: DECAY



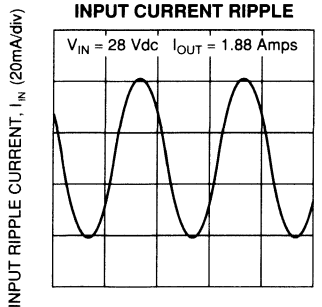
TIME, t (20µs/div)

OUTPUT VOLTAGE RIPPLE



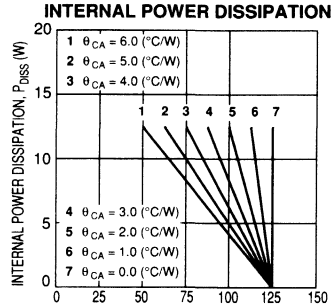
TIME, t (1µs/div)

INPUT CURRENT RIPPLE



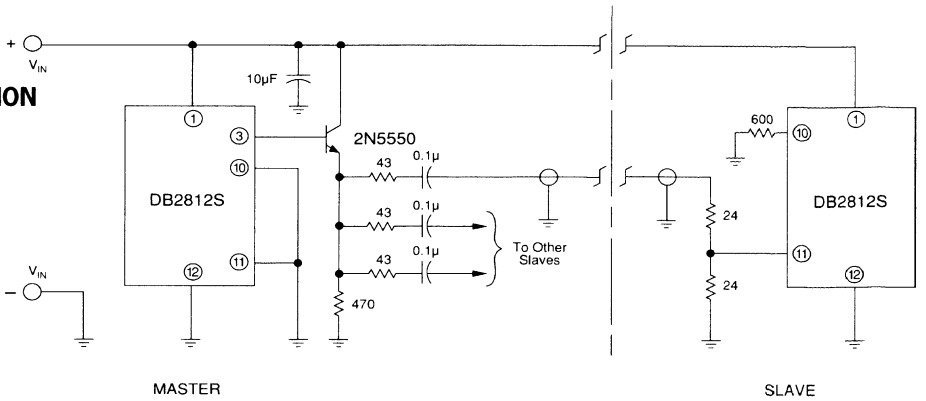
TIME, t (1µs/div)

INTERNAL POWER DISSIPATION



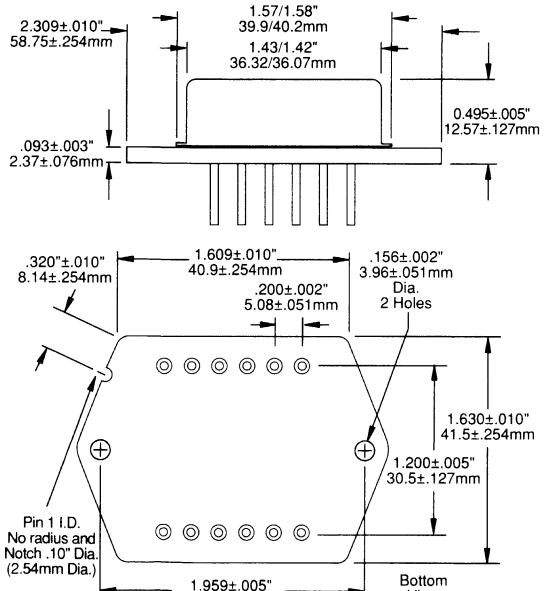
MULTIPLE CONVERTER SYNCHRONIZATION

Operating two or more DB2812S converters as shown at right will synchronize the units to a common switching frequency. This type of operation will help to eliminate the possibility of additional harmonics being generated as a result of different switching frequencies from multiple converters.



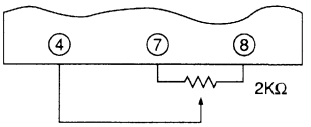
As with all high frequency control systems, great care should be taken in the layout of this circuit. A separate path to ground should be used for the power ground(s) pin 12 and for signal grounds pins 10 and 11. The transistor used to buffer the clock output pin 4 should be mounted as close as possible to the master circuit. The 10µF capacitor should be a good high frequency type and should be mounted as close as possible to the transistor. Shielded cable must be used to distribute the clock information to the slave units to prevent other noise from being coupled into pin 11.

PACKAGE OUTLINE DIMENSIONS MO-127 HIGH PROFILE



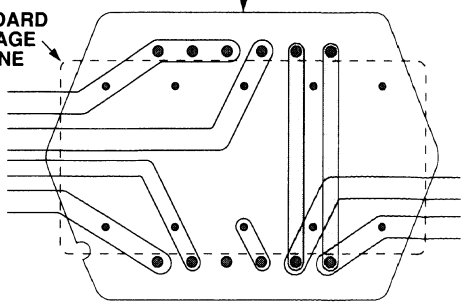
V_{ADJUST}

A 2kΩ potentiometer connected as shown below gives the ability to trim the output voltage between 11.5 and 12.5 volts. The nominal input impedance is 50Ωs measured between pins 4 and 7. An external reference and error amplifier can also provide input to this pin if an even higher degree of output voltage accuracy is desired.



DB2812S PACKAGE OUTLINE

STANDARD PACKAGE OUTLINE



TOP VIEW

□ Denotes second layer of multilayer printed circuit board.

The above diagram shows the form and function adaptability of the DB2812S with the industry standard pinout. The connections shown denote the use of the DB2812S without the synchronization or remote sense features, which are unique to the Apex product.

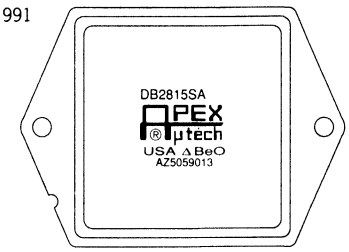
22.5 WATT DC-DC CONVERTER
DB2815S • DB2815SA

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

PRELIMINARY
PRODUCT AVAILABLE SEPT. 1, 1991

HI-REL DESIGN

- **WELDED HERMETIC PACKAGE**
- **LOW INTERNAL TEMPERATURE GRADIENTS**
- **LOW COMPONENT COUNT**
- **ALL CERAMIC CAPACITORS**
- **WAVE SOLDERABLE PACKAGE**



PATENT PENDING

OTHER FEATURES

- **NO DERATING — -55 to +85°C and -55 to +125°C**
- **WIDE SUPPLY RANGE — 12 to 50V**
- **HIGH POWER DENSITY — 22.5W/IN³**
- **HIGH ISOLATION — 500V**

DESCRIPTION

The DB2815S(A) has been created to provide a reliable DC/DC Converter specified over the military temperature range. This has been achieved using a new package, rather than pushing the envelope on existing DC/DC Converter packages. A 12 pin MO-127 High Profile Power Dip™, pioneered by Apex for Power Amplifiers up to 500W, provides very low thermal gradients, rugged hermeticity and high voltage isolation.

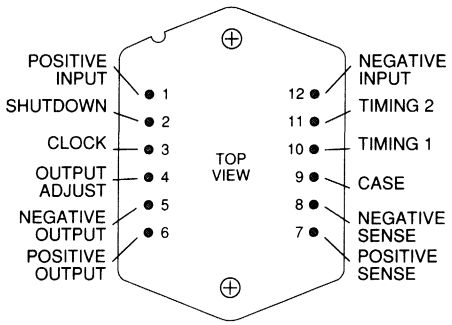
To further enhance reliability, the internal component count has been kept low. What is more, no tantalum or electrolytic capacitors are used in this design, a major cause of low MTBF in DC/DC Converters.

The sophisticated DB 2815S(A) features remote shutdown, kelvin sense, slaveability, and indefinite short circuit protection. It uses a push-pull topology operated in the feed forward, current mode. The typical switching frequency is 500 KHz. A π type input filter is included in order to reduce the peak to peak input ripple current.

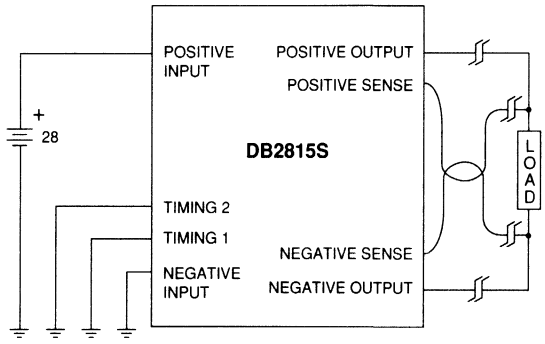
This hybrid converter utilizes thick film (cermet) resistors, ceramic capacitors, miniature magnetics and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures.

The 12-pin MO-127 High Profile Power Dip™ package (see Package Outlines) is hermetically sealed and isolated from the internal circuits. Do not use thermally conductive electrically insulators between package and heatsink.

EXTERNAL CONNECTIONS

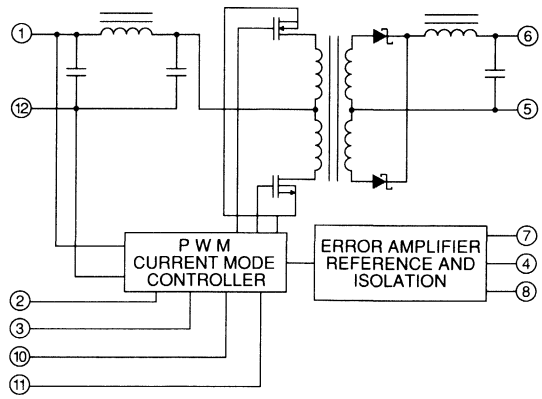


TYPICAL APPLICATION



The above diagram shows the remote sense feature which reduces V_O errors due to resistive drops in long power supply lines. This diagram also shows the connection for non-synchronized operation.

BLOCK DIAGRAM



DB2815S • DB2815SA

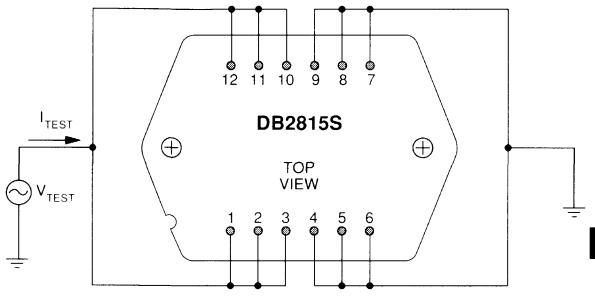
ABSOLUTE MAXIMUM RATINGS
SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

INPUT VOLTAGE RANGE	0 - 50V
OUTPUT CURRENT	1.5A
POWER DISSIPATION	15W
TEMPERATURE, Storage	–65°C, 150°C
TEMPERATURE, Pin Soldering 10s	300°C

SPECIFICATIONS

		DB2815S			DB2815SA			
PARAMETER	**TEST CONDITIONS[2]**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
STEADY STATE CHARACTERISTICS								
OUTPUT VOLTAGE	V_{IN}: 16 - 40 Vdc	15.00	15.05	15.10	*	*	*	Vdc
OUTPUT CURRENT		0.15		1.5	*		*	Amps
EFFICIENCY	V_{IN}: 17-40, I_{OUT} = 1.5 Amps	68	74	79	70	75	80	%
RIPPLE VOLTAGE	Bandwidth DC → 1MHz	20	40	60	20	40	50	mV
OUTPUT POWER			22.5	22.65		*	*	Watts
LINE REGULATION	V_{IN}: 17 to 40 Volts		±0.2	±1.0		±0.1	±0.5	%
LOAD REGULATION	I_{OUT}: 150mA to 1.5 Amps		±1.0	±2.0		±0.1	±0.5	%
INPUT VOLTAGE RANGE	I_{OUT} = 1.5 Amps	15	28	40	15	28	50	Vdc
INPUT CURRENT	V_{IN}: 15 to 40 Volts	0.72	1.09	2.21	0.70	1.07	2.14	Amps
INPUT RIPPLE CURRENT	V_{IN}: 15 to 40 Volts	20	60	70	*	*	*	mA p-p
JUNCTION TEMPERATURE RISE			10	22		*	*	°C
TEMPERATURE RANGE, case	I_{OUT} = 1.5 Amps	–55	25	85	–55	25	125	°C
QUIESCENT CURRENT	V_{IN}: 15 to 40 Volts; V_{PIN2}: 5V		60	100		*	*	mA
ISOLATION CHARACTERISTICS								
LEAKAGE RESISTANCE	(See Figure 1 DC)	100			*			MΩ
LEAKAGE CAPACITANCE	(See Figure 1, f = 10KHz	20	35		*	*		pF
DYNAMIC CHARACTERISTICS								
LINE STEP RESPONSE	V_{IN} Slew Rate = .1V/µs							
OUTPUT VOLTAGE	V_{IN}: 17 → 40 Volts		+2500			*		mVpk
RECOVERY TIME	V_{IN}: 17 → 40 Volts		700			*		µsec
OUTPUT VOLTAGE	V_{IN}: 40 → 7 Volts		–2500			*		mVpk
RECOVERY TIME	V_{IN}: 40 → 17 Volts		600			*		µsec
LOAD STEP RESPONSE	I_{OUT} Slew Rate = 0.5A/µs							
OUTPUT VOLTAGE	I_{OUT}: .75 → 1.5 Amps		–1300			*		mVpk
RECOVERY TIME	I_{OUT}: .75 → 1.5 Amps		400			*		µsec
OUTPUT VOLTAGE	I_{OUT}: 1.5 → 0.75 Amps		+1700			*		mVpk
RECOVERY TIME	I_{OUT}: 1.5 → 0.75 Amps		400			*		µsec
START-UP OVERSHOOT	V_{IN} : 0 → 28V		0.25			*		Vdc
SHUTDOWN DELAY	V_{PIN2} : 0 → 5 Volts		400			*		µsec
SHUTDOWN RECOVERY	V_{PIN2} : 5 → 0 Volts		30			*		msec



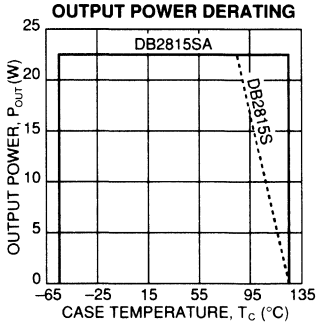
ISOLATION TEST CIRCUIT

NOTES: * The specification of DB2815SA is identical to the specification for DB2815S in applicable column to the left.

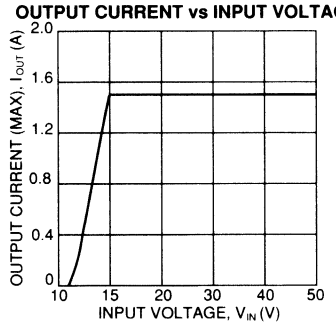
1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF. For guidance, refer to the heatsink data sheet.
2. Unless otherwise stated T_C = 25°, $V_{IN} = V_{PIN12} - V_{PIN1}$ = 28V, I_{OUT} = 1.5 Amps.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

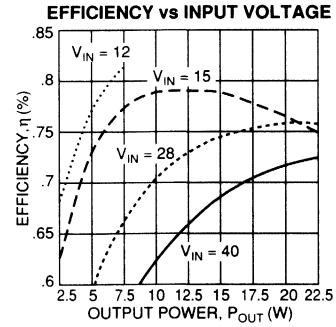
OUTPUT POWER DERATING



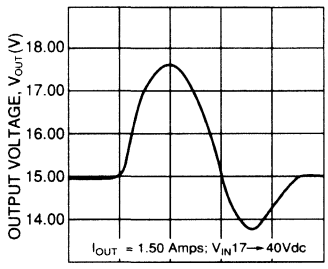
OUTPUT CURRENT vs INPUT VOLTAGE



EFFICIENCY vs INPUT VOLTAGE

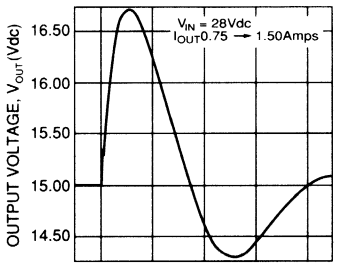


LINE TRANSIENT RESPONSE



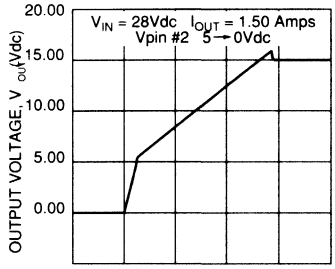
TIME, t (200µs/div)

LOAD STEP RESPONSE



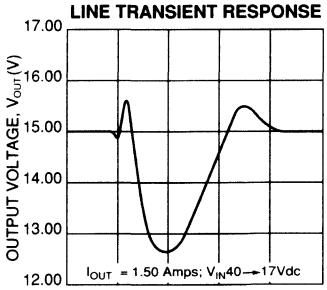
TIME, t (100µs/div)

SHUTDOWN RESPONSE: ATTACK



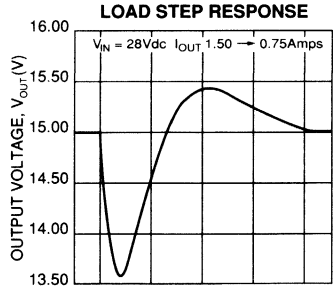
TIME, t (5ms/div)

LINE TRANSIENT RESPONSE



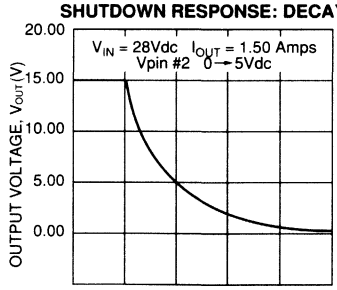
TIME, t (200µs/div)

LOAD STEP RESPONSE



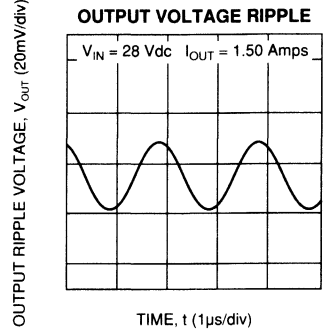
TIME, t (100µs/div)

SHUTDOWN RESPONSE: DECAY



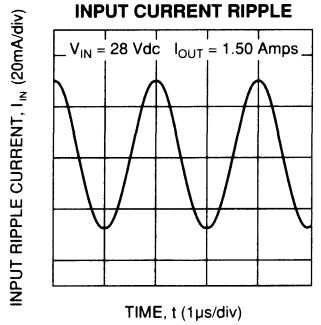
TIME, t (100µs/div)

OUTPUT VOLTAGE RIPPLE



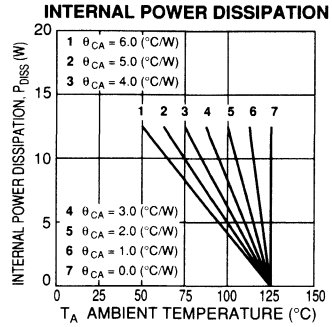
TIME, t (1µs/div)

INPUT CURRENT RIPPLE



TIME, t (1µs/div)

INTERNAL POWER DISSIPATION



MULTIPLE CONVERTER SYNCHRONIZATION

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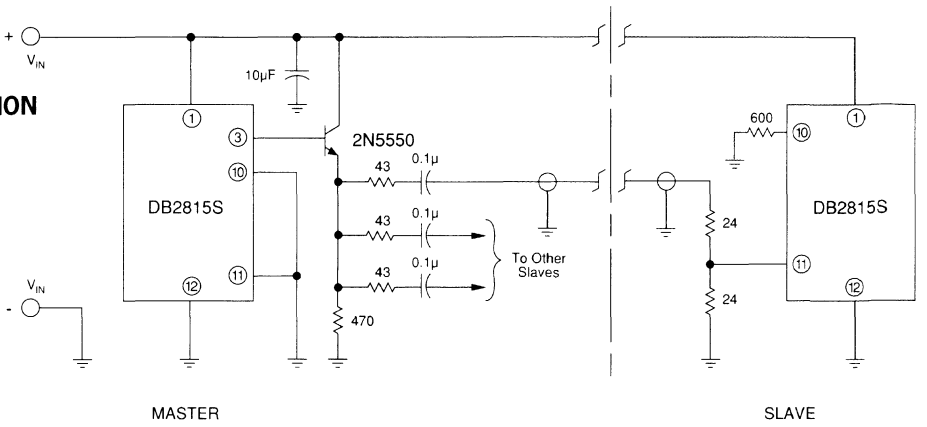
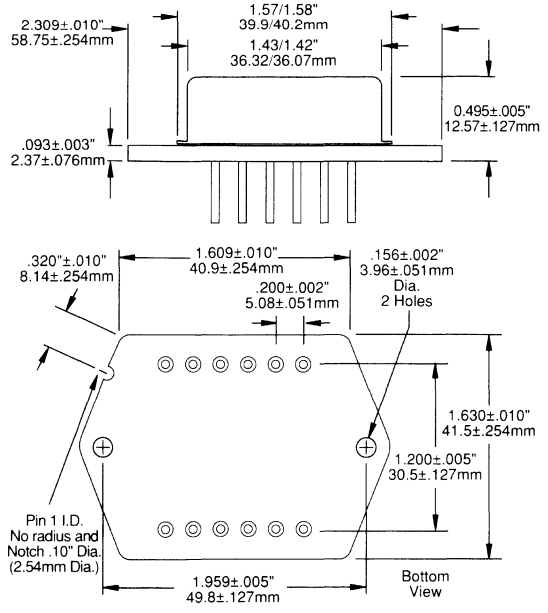


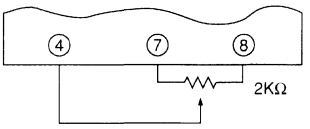
As with all high frequency control systems, great care should be taken in the layout of this circuit. A separate path to ground should be used for the power ground(s) pin 12 and for signal grounds pins 10 and 11. The transistor used to buffer the clock output pin 4 should be mounted as close as possible to the master circuit. The 10µF capacitor should be a good high frequency type and should be mounted as close as possible to the transistor. Shielded cable must be used to distribute the clock information to the slave units to prevent other noise from being coupled into pin 11.

PACKAGE OUTLINE DIMENSIONS MO-127 HIGH PROFILE

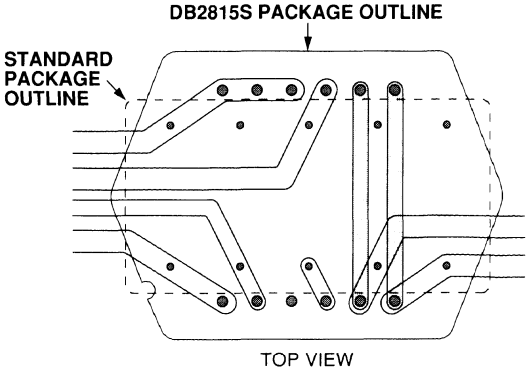


V_{ADJUST}

A 2kΩ potentiometer connected as shown below gives the ability to trim the output voltage between 13.5 and 16.5 volts. The nominal input impedance is 50Ωs measured between pins 4 and 7. An external reference and error amplifier can also provide input to this pin if an even higher degree of output voltage accuracy is desired.



DB2815S PACKAGE OUTLINE



The above diagram shows the form and function adaptability of the DB2815S with the industry standard pinout. The connections shown denote the use of the DB2815S without the synchronization or remote sense features, which are unique to the Apex product.

APPLICATION NOTES

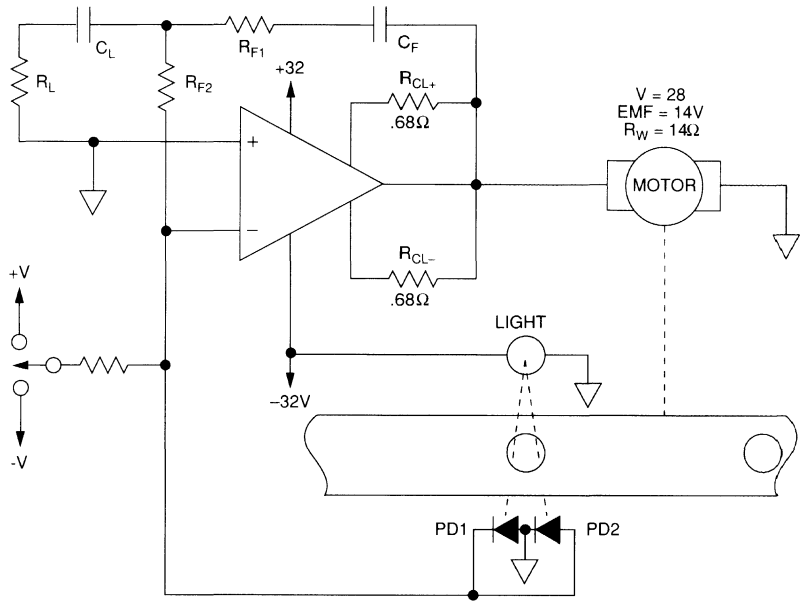


FIGURE 1. SEQUENTIAL POSITION CONTROL

INTRODUCTION

Power Op Amps are ideally suited for position control because their response time is fast compared to any mechanical drive train. The optoelectronic technique of position control can move to and maintain fixed index points on linear or rotary motion components while adding no linkages or independently moving parts. The resulting system features high reliability, accuracy and repeatability. If the integration of photodiode currents is required, select a power amplifier with an FET input to maintain very low bias current levels such that the integrating capacitor voltage will remain constant during periods when both photodiodes are not illuminated. Further selection criteria should be based on motor ratings and/or available power.

SEQUENTIAL POSITION CONTROL

In the circuit shown in Figure 1, the PA07 integrates the differential output of the pair of photodiodes and drives the motor in the proper direction until the photodiode currents are equal. This differential configuration negates the well known temperature and time instabilities of optoelectronic devices. To move between index points, a fixed input current is momentarily switched to the amplifier input causing the amplifier to drive the motor in the desired direction. The charge on C_F will maintain motor drive as the input current is switched off prior to reaching the index point. As the first photodiode is illuminated, its output reinforces the current direction of motion. As the second photodiode is illuminated, its current will reverse the motor drive, causing the system to lock to the index point.

As motor response and system inertia vary widely, C_F and R_F must be selected for the individual application to provide proper damping. C_F must be small enough to allow drive reversal before the index point passes the second photodiode or the system will continue on to the next index. Very small values of C_F can cause severe overshoot or oscillation leading to motor burnout and/or drive train failure. R_{F1} and R_{F2} are required to stabilize the control loop at the unity gain point and to minimize overshoot. R_L and C_L form a lead network which may be included to improve response time by enabling the amplifier to modify the motor drive based on a change of the sensor output. In this manner, a braking force can be applied to the motor prior to reaching the index point. The motor shown in Figure 1, having EMF of 14V, will apply a 46V stress across the conducting output transistor when reversed. With a duration longer than 5ms, the steady state secondary breakdown line of the SOA for the PA07 curves requires the current limits to be set to 1A. See PA07 data sheet.

SINGLE POINT POSITION CONTROL

A variation of the above technique shown in Figure 2 can be used to return a wheel to a single index point after rotating in either direction. The low inertia, fast response system will take the shorter route to the index point when switched from run to stop. The PA12A was selected for this application because it provides high power while keeping bias current levels low with respect to the photodiode currents. To improve response time, the lead network compensates for motor response lagging behind any change in drive voltage. A run control current of sufficient amplitude to override the photodiode currents is fed to the amplifier inverting input. Removal of this current restores control to the photosensors.

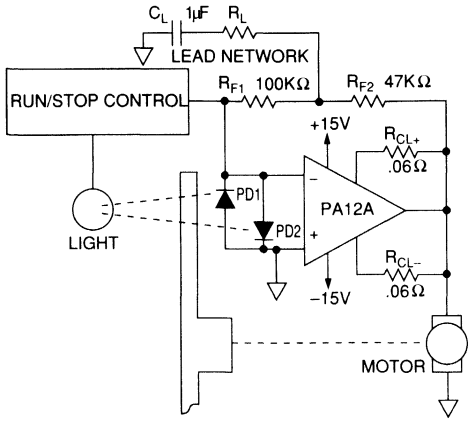


FIGURE 2. SINGLE POINT POSITION CONTROL

POSITION CONTROL MASK

Figure 3 shows details of the wheel preparation and sensor placements at the stop index. Arrows indicate direction of rotation when the corresponding photodiode has the higher output. While it is theoretically possible to achieve a stable position on the opposite side of the wheel, system noise or a slight movement will imbalance the equal photodiode currents and the higher current sensor will receive even more light. This causes the wheel to seek the desired index point. Masking of the wheel at an angle to the radial softens the control function and prevents overshoot.

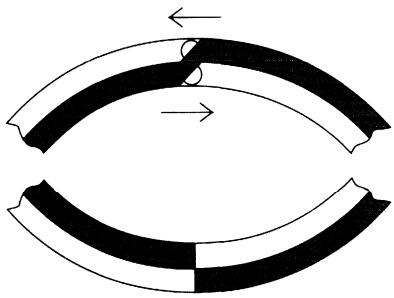


FIGURE 3. SINGLE INDEX POINT DISK

SPOT SIZE

Optimum relationship of beam size to active areas of the photodetectors is shown in Figure 4. A centered beam should illuminate half the photosensitive area of each diode. Too large a beam will produce no change of sensor output for a range of positions, while a smaller beam will produce a nonlinear transfer function near the center line between the photosensitive areas. This makes selection of C_F to dampen the circuit difficult and requires a higher intensity light source.

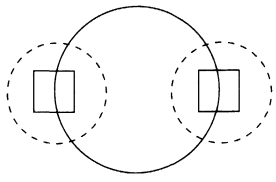


FIGURE 4. BEAM-SENSOR ALIGNMENT

DIGITAL INTERFACING

For systems with digital control, Figure 5 illustrates a method not requiring generation of bipolar control signals thus saving the cost of digital to analog conversion. When logic lines are low, the signal diodes will not conduct. This condition leaves control to the photodiodes. A high level on line 2 will cause current to flow to the summing junction and the amplifier will swing negative. A high level on line 1 will raise the summing junction voltage above ground, and the amplifier will swing positive. Select a resistance value such that a high logic level will provide at least twice the maximum current from each photodiode to insure control override regardless of photodiode signals.

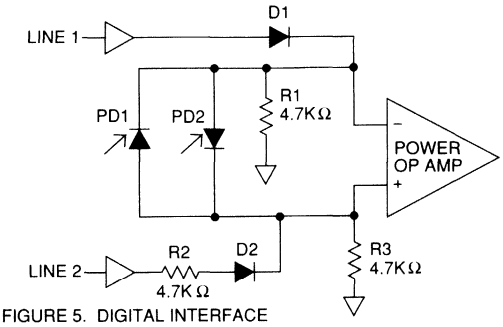


FIGURE 5. DIGITAL INTERFACE

DUAL SENSORS

For applications requiring high precision, the use of a dual element position sensing PD1(Figure 5) will allow smaller beam size, tighter beam control and provide better thermal equilibrium. The specified resolution of the detector recommended for this application is better than .0127mm (.0005 inch). The detector is a three terminal device requiring a current inverter as shown in Figure 6 to achieve the differential configuration. Two equal resistors, R1 and R2, should be scaled to the maximum photodiode current and swing capability of the signal amplifier.

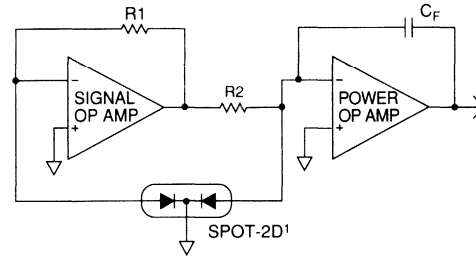


FIGURE 6. CURRENT INVERSION

[1]A line of multi-element position sensors is available from:
United Detector Technology
12525 Chadron Avenue
Hawthorne, CA 90250
(213) 978-0516

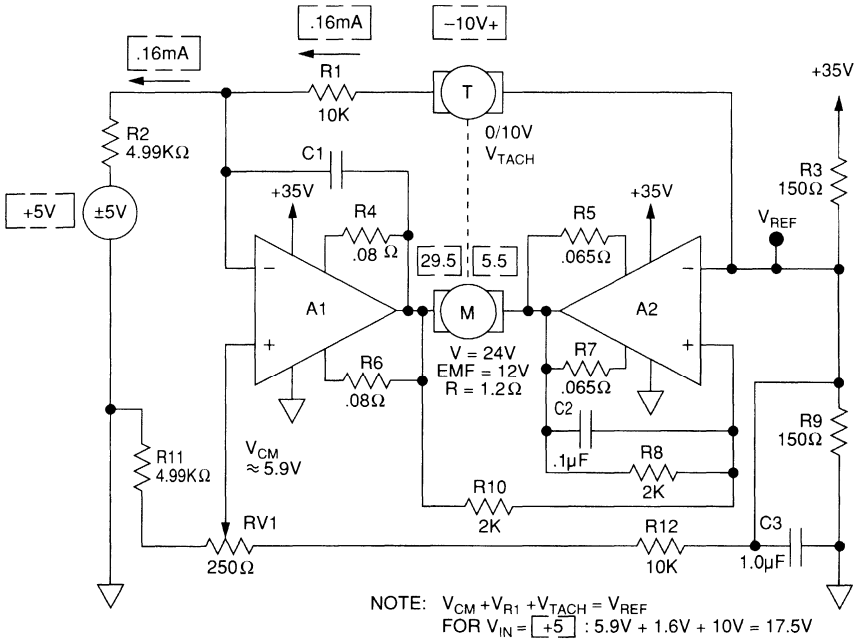


FIGURE 1. BI-DIRECTIONAL BRIDGE FOR A SINGLE SUPPLY

INTRODUCTION

Two power op amps configured in a bridge circuit can provide substantial performance advantages:

1. Bi-directional output with a single supply
2. Twice the output voltage
3. Twice the slew rate
4. Twice the output power
5. Half the power supply requirement

With power op amps currently from APEX, output voltage swings as high as 580Vpp at ±75mA and 180Vpp at ±15A can be obtained. To achieve these levels of performance, both terminals of the load must be driven and extra components are required.

BI-DIRECTIONAL DRIVE ON A SINGLE SUPPLY

Figure 1 depicts a bi-directional motor speed control using a single supply which features ground referenced bipolar input signals. A mid-supply reference created by R3 and R9 establishes the DC operating levels for A1 and A2. Inverter A2 drives the load equally in the opposite direction with respect to the output of input amplifier A1. This configuration places both load terminals at the reference voltage with a zero input condition and prevents premature saturation of either amplifier.

To understand the operation of the circuit, consider A1 as having two sets of inputs:

1. Voltage dividers from the supply voltage to establish common mode bias.
2. Actual input signal and tachometer feedback.

One sixth of any supply voltage variation will appear equally at both inputs of the amplifier. However, the common mode rejection (CMR) of the op amp will reduce its response by four orders of magnitude at low frequencies. The low pass function of C3 insures optimum rejection by keeping the common mode inputs in the low frequency spectrum. The common mode voltage (CMV) range of the amplifier sets the minimum common mode bias at the inputs of A1. The circuit shown provides a nominal 5.9V from the supply rail (ground) which allows power supply variations to 10% below nominal.

For the actual input signal, C1, R1, R2, and A1 form an integrator (non-inverting input is constant). With the control voltage applied across R2 and the tachometer voltage applied across R1, integration forces the motor speed to be proportional to the input voltage. The value of C1 must be selected for proper damping of the total system which includes the mechanical characteristics of the drive train.

Resistors R4 and R6 set current limits of A1 to 7.5A. When A1 current limits, A2 will reduce its output voltage equal to the voltage change of A1. By insuring A1 will limit prior to A2, power stress levels of the two amplifiers are equalized. In addition to amplifier protection, this programmability is being utilized to limit the temperature rise in the motor, thereby increasing expected life of the system. Maximum continuous load rating of the motor shown is 10A and locked rotor (stall) current is 20A. Since locked rotor ratings generally refer to abnormal conditions, the motor is being used near capacity while maintaining a comfortable safety margin for motor and drive circuit.

The key to accuracy of this circuit lies in matching the division ratios from the reference voltage to ground for both the inverting and non-inverting inputs of A1. The inverting side division ratio is affected by the impedances of the control signal and tachometer. Normally, the

impedance of a voltage output DAC and the winding impedance of the tachometer are negligible. This allows use of cost effective 1% resistors and requires only trimpot RV1 to provide precision adjustment. Ratio match errors will appear as tachometer output errors. These errors will be of a size equal to the ratio of mismatch times the reference voltage.

The second major accuracy consideration of this circuit is the voltage offset of A1. As this error will appear at the tachometer at a gain of three, the PA12A was selected for its improved specification of 3mV compared to 6mV for the regular PA12.

Changes of input voltage range, RPM range or tachometer output ratings are easily accommodated. Lowering the values of R1 and R12 (ratio match still required) will re-scale smaller tachometer voltage

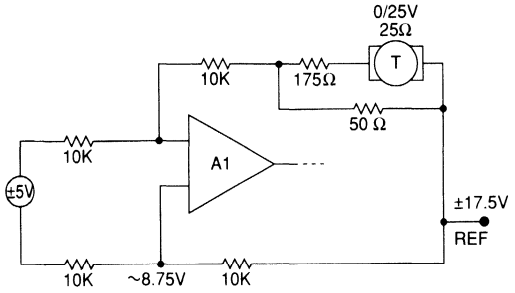


FIGURE 2. HIGH OUTPUT TACHOMETER

spans or lower RPM ranges to the ±5V input level. While increased input signal levels could be re-scaled in the same manner, increasing R2 and R11 provides the required re-scaling with the added benefit of lowering control signal drive requirements.

Higher voltage tachometer voltage spans require a different approach to re-scaling due to the CMV limitations at the inputs of A1. Figure 2 illustrates a technique using a 25V tachometer which will maintain adequate CMV for A1 with supply voltages down to 20V. Calculations for the divide by five network at the tachometer includes winding impedance to achieve accurate scaling to the ±5 input signal. For error budgets, this factor of five must be applied to both the ratio mismatch errors and voltage offset errors as above. Total gain for calculating offset errors will be 10.

ELECTROSTATIC DEFLECTION

The cathode ray tube (CRT) shown in Figure 3 requires 500Vpp nominal drive. Allowing for a ±5% gain error plus a 10% (of full scale) centering voltage tolerance, brings the desired deflection voltage swing to 575Vpp. Two PA84 high voltage power op amps provide this differential voltage swing. Slew rates of 400 volts per microsecond at the CRT enable the beam to traverse the face plate in less than 1.5 microseconds.

The gain of A1 is set by (R3+RV1)/R1 at 100. The circuit provides for both gain adjustment (RV1) and beam centering (RV2). For proper scaling, R4 and R6 reduce the centering control voltage of trimpot RV2 to ±250mV. C2 provides the desired low AC impedance to ground to enhance stability and eliminate noise pickup. A2 inverts the output of A1 at unity gain (set by R8/R5), to yield an overall gain of 200 for single ended input signals measured at the differential output. R9 and C4 constitute a second input to A2 with an AC gain of 100 (R9/R8). Using ground as an input has no direct signal contribution, but it does allow both amplifiers to use the phase compensation recommended at a gain of 100 (20K, 50pF), thereby achieving a large power bandwidth of 250kHz.

TRANSIMPEDANCE BRIDGE FOR MAGNETIC DEFLECTION

The circuit shown in Figure 4 drives the electro-magnetic deflection yoke of a precision x-y display. Two factors constitute the design challenge of this circuit:

1. Greater than 15V drive levels are required to change current magnitude and polarity to achieve fast endpoint-to-endpoint display transition times.

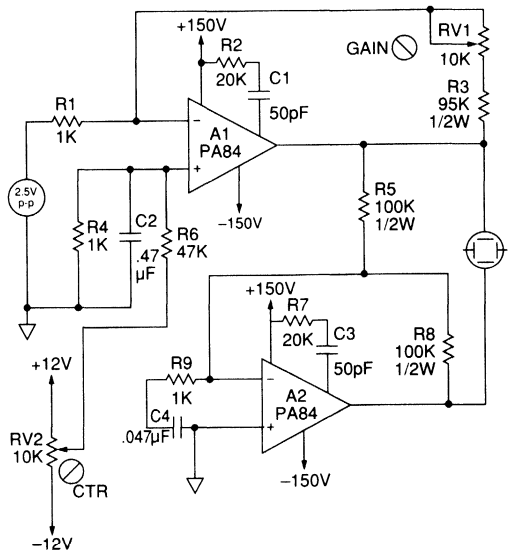


FIGURE 3. ELECTROSTATIC DEFLECTION AMPLIFIER

2. Only ±15V power supplies are available in the system.

The bridge circuit can drive almost double the single power supply voltage, thereby eliminating the need of separate supplies solely for CRT deflection. The maximum transition time between any two points is 100μs for display ratings of:

Yoke inductance = 0.3mH
Full scale current = ±3.75A
DC coil resistance = 0.4 ohms

The voltage required to change the current in an inductor is proportional to current change and inductance, but inversely proportional to transition time.

V = di*L/dt
V = 7.5A*0.3mH/100μs = 22.5V

The Apex low voltage power op amp PA02 is an ideal choice for this circuit due to its high slew rate and ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the

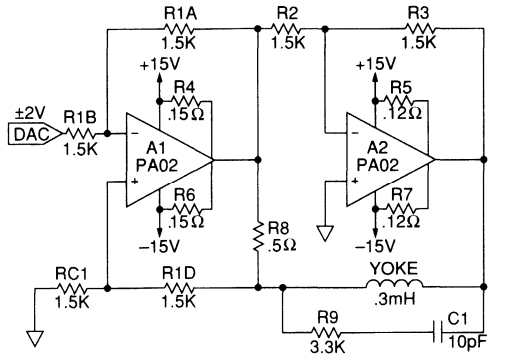


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

beam transition time will be greater than 26V. The configuration shown in Figure 4 utilizes current sense resistor R8 to implement a voltage controlled current source for A1 while A2 functions as an inverter to double the voltage drive to the load.

In detail, the differential input configuration of A1, and R1A through R1D, feeds back the output voltage of A1 as a common mode signal. In this manner, the amplifier CMR and divider ratios maintain a transimpedance function by removing the output voltage of A1 from a first order calculation of performance. Since R1A/R1B and R1C/R1D must divide this output voltage equally for both amplifier inputs, these resistors form a precision resistor network with initial matching and temperature tracking of the divider ratios. Mismatch errors can be modeled as control voltage errors equal to the percent of mismatch times the output voltage of A1. The voltage proportional to output current developed by R8 is fed back as a differential signal for comparison with the input voltage.

As the current to voltage phase relationship of the inductive load changes with frequency, the conversion function of R8 introduces phase shift up to 90° into the feedback circuit. At high frequencies, it is possible for the sum of the inductive phase shift, plus the amplifier phase shift, to equal 180° while the amplifier still has a gain of unity. The series RC damping network placed in parallel with the inductive load reduces its phase shift and thereby eliminates the potential for oscillations.

EFFICIENT USE OF POWER SUPPLIES

To illustrate the advantages of the bridge circuit, Figures 5 and 6 show two high performance audio amplifier designs with equal output power, but substantially different supply requirements. In the circuit of Figure 5, the instantaneous load current will appear on only one supply rail. This means each supply rail must support the total wattage requirement and utilization is only 50% at peak outputs. In contrast, the equal and opposite drive characteristic of the bridge circuit shown in Figure 6 loads both positive and negative supply rails equally during each half cycle of the signal. This improved utilization reduces size, weight and cost of the power supply for the circuit in Figure 6 even though input and output power ratings are essentially equal.

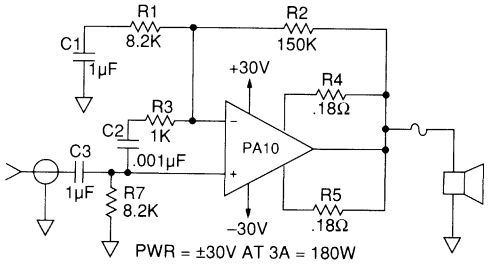


FIGURE 5. STANDARD AUDIO AMPLIFIER

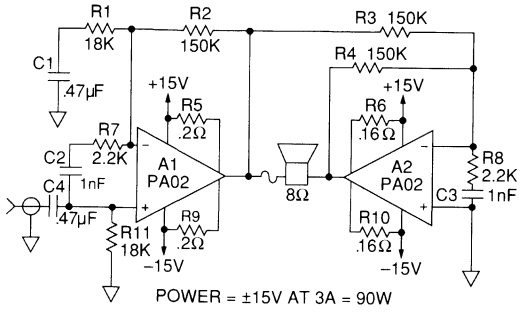


FIGURE 6. BRIDGE AUDIO AMPLIFIER

CONCLUSION

Bridge circuits can make the difference when performance requirements exceed voltage limitations of either the available power supplies or the power op amps. The input section of these circuits consists of a standard amplifier circuit for driving a single ended load. The added amplifier serves merely as an inverter. It doubles drive voltage by providing an equal and opposite output, thereby making the output fully differential. The performance increases usually outweigh the increased cost and complexity.

INTRODUCTION

Closed loop power op amp circuits offer distinct advantages in current control over open loop systems. Using a power op amp in the conventional voltage to current conversion circuit, the negative feedback forces the coil current to stay exactly proportional to the control voltage. The resulting accuracy makes many new applications feasible. For example, by placing the non-linear impedance of the deflection yoke inside the feedback loop, steady state positioning, which is difficult, if not impossible, to achieve with open loop circuits, can easily be implemented with a power op amp. In addition, sweep systems with substantially improved linearity can be designed using power op amps.

Typical applications include: heads-up displays, which require random beam positioning or E-beam lithography; and other complex data displays which can achieve the needed accuracy with a power op amp. Moreover, the versatility and ease of use of power op amps will help speed up the design process while at the same time reducing development cost. The final result will be a more accurate and reliable display using fewer parts.

HIGH RESOLUTION AND HIGH EFFICIENCY

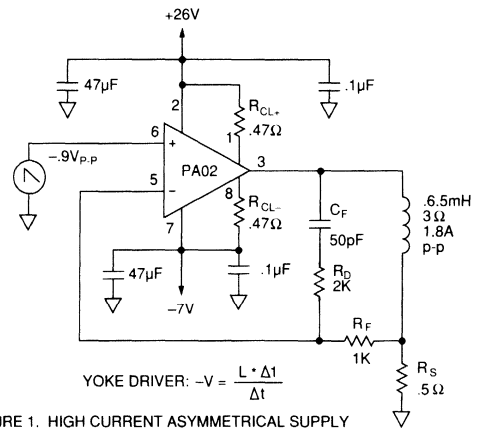


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

The vertical deflection circuit of Figure 1 was designed to drive a high efficiency RCA CODY II tube. The PA02 was selected for this configuration because of its exceptional linearity and other advantages such as high slew rate, fast settling time, low crossover distortion, and low internal losses. All of these advantages contribute to a superior resolution display.

The key to this circuit is the sense resistor (R_S) which converts the yoke current to a voltage for op amp feedback. With the feedback applied to the inverting input and the position control voltage applied to the non-inverting input, the summing junction's virtual ground characteristic assures the voltage across R_S is equal to the input voltage. Thus, the highly linear control of the voltage across R_S insures accurate beam positioning.

The value assigned to R_S has significant impact on the performance of this circuit. All op amp input errors such as voltage offset, imperfect common mode rejection, offset drift, etc., will appear across the sense resistor and produce an error; therefore, the R_S should be as large as possible to insure that errors will be small when translated into current. Very large values of R_S will reduce these errors to a point of insignificance. Unfortunately, on the downside, the voltage drive capability will be diminished and circuit power dissipation will increase because the total coil current flows through the sense resistor.

Weighing these trade-offs between errors and efficiency in the selection of R_S value will produce the optimum choice for each application. The voltage drive requirements will then be defined by inductance, transition times and current. This display must operate at 50Hz or 60Hz with retrace times of 730µs and coil currents of $2.25A_{P-P}$.

The drive voltage required to change the current in an inductor is proportional to both current change and inductance, but inversely proportional to transition time.

$$V_{DRIVE} = dI*L/*dt \quad (1)$$
$$V_{DRIVE} = 2.25A_{P-P}*6.5mH/15ms = .98V \quad \text{(sweep)} \quad (2)$$
$$V_{DRIVE} = 2.25A_{P-P}*6.5mH/730\mu s = 20.03 \quad \text{(retrace)} \quad (3)$$

To determine the power supply levels, add the supply-to-output differential rating of the power op amp (from the Amplifier Data Sheet) and the voltage dropped across the combined values of the sense resistor plus the coil resistance, to these drive requirements to arrive at +26V and -7V as follows:

$$V_{DROP} = 1_{PK}* (R_S + R_L) \quad (4)$$
$$V_{DROP} = 1.125A_{PK}* (.5\Omega + 3\Omega) = 3.94V \quad (5)$$
$$V_S = V_{DRIVE} + (V_S - V_O) + V_{DROP} \quad (6)$$
$$V_S = .98V + 2V + 3.94V = 6.92V \quad \text{(sweep)} \quad (7)$$
$$V_S = 20.03V + 2V + 3.94V = 25.97V \quad \text{(retrace)} \quad (8)$$

Caution should be exercised when using asymmetric power supplies, because the inductive load has the potential to store energy from the higher supply. This could be initiated by an abnormal condition causing the high output voltage to remain on the yoke longer than the normal retrace time. After such an occurrence, the collapsing magnetic field would discharge the stored energy into the lower voltage supply via the inductive kickback protection diodes in the power op amp. This will produce a voltage transient on the supply rail with its amplitude a function of stored energy and the transient impedance of the power supply. If this transient added to the supply voltage exceeds the rail-to-rail voltage rating of the amplifier, the result will be destructive. In such cases, a zener clamp on the amplifier output should be used.

A note of caution when using modular construction. Instruction manuals always specify, **"power down first, then remove the module."** However, because this doesn't always happen, protective action should be taken. The mechanical break of the connection to any inductance, coil or wire, causes high voltage flyback pulses. The stored energy must be absorbed somewhere. It's much better to use the zener clamp than to risk the op amp.

STABILITY CONCERNS

Since the current control capabilities of this circuit rely on feedback from the current-to -voltage conversion sense resistor, phase shift due to the inductance of the yoke will be evident in the feedback signal. Because the phase shift approaches 90° on a perfect inductor and the phase margin of an op amp is always less than 90°, design adaptations are required to prevent oscillation.

The network consisting of R_D, R_F and C_F, serves to shift from a current feedback via R_S to a direct voltage feedback at the upper frequencies. This bypasses the extra phase shift caused by the inductor. In selecting component values for this network, R_F should be much larger than R_S, but should not exceed 1KΩ for the PA02, because the input capacitance of the op amp would otherwise add phase shift. Next select R_D to properly dampen the circuit at the unity gain frequency. Generally, its value is a multiple of R_F, a safe starting value is 2 * R_F. Select C_F for a 3dB corner frequency with R_D at 1/3 the unity gain frequency of the amplifier. For the PA02's bandwidth of 4.5MHz, the C_F should be 50pF.

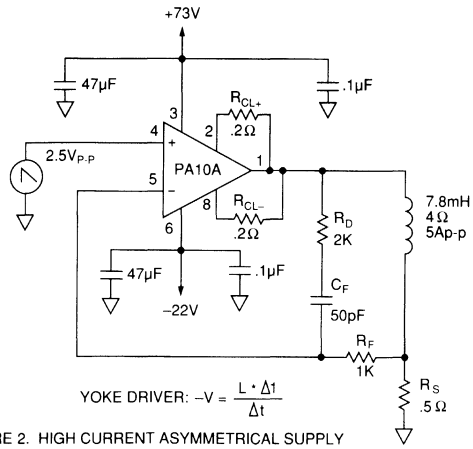


FIGURE 2. HIGH CURRENT ASYMMETRICAL SUPPLY

For an even more powerful version of this circuit, the PA10 power op amp can be used, as shown in Figure 2. With this device, a 7.8mH 4Ω coil can be driven at $5A_{P-P}$ with the same timing requirements. Calculations for this design are:

$V_{DRIVE} = 5A_{P-P}{}^{*}\ 7.8mH/15ms = 2.6V$	(sweep)	(9)
$V_{DRIVE} = 5A_{P-P}{}^{*}\ 7.8mH/730\mu s = 53.43V$	(retrace)	(10)
$V_{DROP} = 2.5_{PK}A^{*}\ (.5\Omega + 4\Omega) = 11.25V$		(11)
$V_S = 2.6V + 8V + 11.25V = 21.85V$	(sweep)	(12)
$V_S = 53.43V + 8V + 11.25V = 72.68V$	(retrace)	(13)

Both of the circuits illustrated have a 730µs retrace time requirement, met easily by the op amp's slew rate and settling time which is substantially faster.

To better understand this and other applications, Figure 3 illustrates the output voltage waveforms generated by the power op amp to obtain the desired retrace output current step for Figure 2. The wave form preceding point A is the end of the sweep wave-form with a relatively slow rate of change of the current. The peak output voltage at point A equals the sum of equations 9 and 11.

Retracing begins at time A where equation 10 dictates the drive voltage required to achieve the retrace di/dt. From time A to time B, the amplifier is running at the slew rate limit. The current in the yoke starts to track the input voltages at time B. From time B to time C, the output voltage produced is the sum of equation 3 plus the value of instantaneous IR drops (Equation 11 indicates the final value).

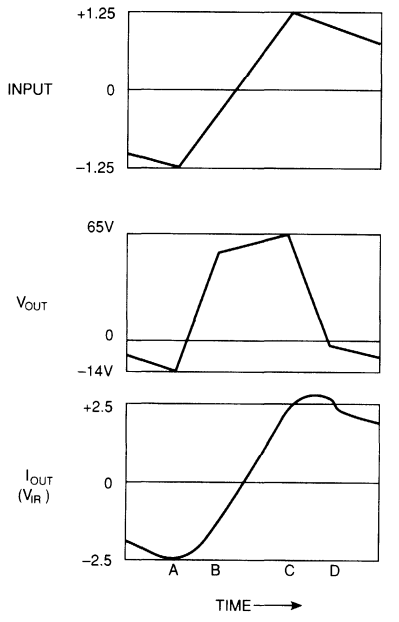


FIGURE 3. RETRACE WAVEFORMS

The abrupt slope change of the input waveform at point C, again puts the amplifier in slew rate limit until the output current is proportional to input voltage according to equation 9, plus IR drops. At point D, the equation is satisfied and the amplifier will maintain the required current for the sweep portion of the waveform.

Time expansion has been used for Figure 3 to better illustrate the slew rate and voltage swing requirements for the amplifier. During the retrace section of the waveform, the amplifier has to slew the sum of drive voltage (Equations 9 and 10) twice. For the circuit of Figure 2, this amounts to 112V. With the PA10's typical slew rate of 5V per microsecond, the slew time is only 22.5 microseconds, an insignificant portion of the total retrace period. However, by understanding the voltage swing requirements, it can be seen that slew rate becomes important as the scan rates increase.

Both the PA02 used in Figure 1, and the PA10 used in Figure 2, have raised accuracy levels by placing the non-linear inductive element inside the op amp feedback loop. The very high gain of the op amp and the use of negative feedback produces superior linearity.

RAPID TRANSITION FOR HEADS-UP DISPLAY

Heads-up displays demand swift transition between any two points on the screen. The waveforms of Figure 4 depict the input drive voltage and required current to the yoke to achieve a single full-scale step in beam position for the circuit in Figure 5. The 3V levels sustain the steady state current through the coil resistance and the sense resistors. The 29V level corresponds to the peak output voltage required for a position change.

Starting with amplifier slew rates and settling times from the data sheet, it is determined what percentage of the total transition time will be required for slewing and settling. A reasonable starting point would be to allow 50% of the total transition time.

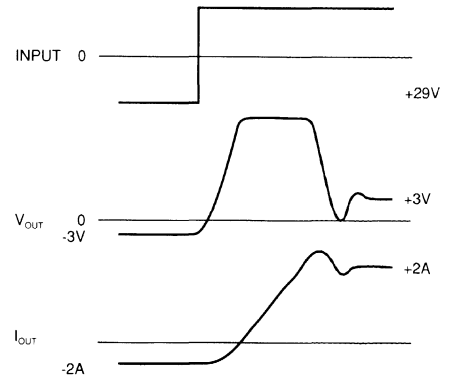


FIGURE 4. FULL SCALE STEP FUNCTION WAVEFORMS

This circuit was designed for a maximum transition time of 4µs when delivering $2A_{PK}$ currents to the 13µH coil. While the fundamentals of this circuit are the same as previously detailed, there are differences due to the higher speed. To achieve rapid transitions, amplifier slew rates must be optimized. The PA09 Video Power Op Amp with external phase compensation allows this. However, close examination of poles and zeros in the feedback loop is required because reactive feedback elements force the amplifier to operate over a very wide range of gains, very high during transition but unity at steady state.

The network of C_F, R_D and R_F set gain to approximately 100 at high frequencies. This allows phase compensation for a gain of 100 and correspondingly high slew rates. The next step shown in Figure 6 is to plot the feedback zero of the yoke inductance and the sense resistor. Then the high frequency feedback level of the R_C network, approximately 40dB, can be drawn in and C_F selected to produce a pole approximately one decade below the intersection point. Figure 7 shows the PA09 open loop bode plot and the modification due to

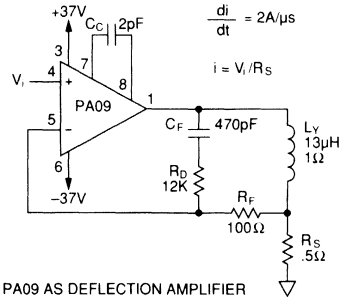


FIGURE 5. PA09 AS DEFLECTION AMPLIFIER

feedback effects. A slope increase below 500kHz and a shallow slope at the unity crossing point to insure stability.

If 50% of the total transition time is allowed for slewing and settling, 2µs will remain to change the yoke current with full voltage applied to the coil. Voltage requirements are calculated as follows:

$V = di^* L/dt$ (14)

$V = 4A^*13\mu H/2\mu s = 26V$ (15)

$V_{DROP} = 2A^* (.5\Omega + 1\Omega) = 3V$ (16)

$V_{DRIVE} = 26V + 3V = 29V$ (17)

$V_S = 29V + 8V = 37V$ (18)

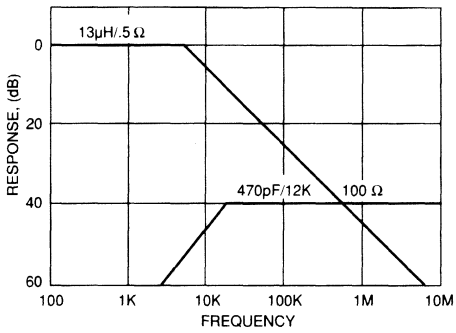


FIGURE 6. FEEDBACK RESPONSE

Selection of the external phase compensation will also need to be calculated as applicable to the PA09. Component values are recommended on the Amplifier Data Sheet according to the effective gain setting of the circuit (R_D to R_F)

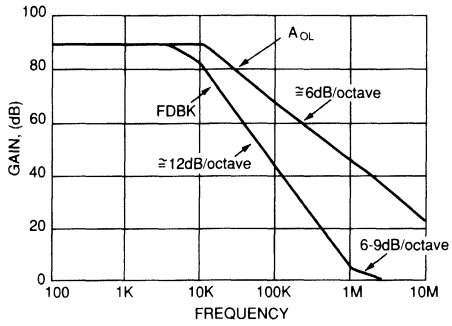


FIGURE 7. COMPOSITE RESPONSE

With the external compensation selected, the PA09 Data Sheet indicates the amplifier slew rate will be 400V per microsecond. For a calculated swing of 58V, the required voltage slewing time is 145 nanoseconds. Adding the settling time to 0.01% of 1.2µs, the total is comfortably below the 50% allotment of 2 microseconds.

When the circuit was tested, values were further optimized for best performance. The value of R_D had a considerable effect on damping of the circuit. This could be predicted because R_D affects the corner frequency where the roll off slope must be flattened near the unity gain point. The value of C_F was not critical; however, a compensation capacitor of 2pF, as opposed to the data sheet recommendation of 5pF, helped to increase the slew rate without significant affect on stability.

Due to the high speed of PA09, specific precautions are recommended to insure that optimum stability and accuracy are maintained:

1. To help prevent current feedback, use single point grounding for the entire circuit or utilize a solid ground plane.
2. To insure adequate decoupling at high frequency, bypass each power supply with a tantalum capacitor of at least 10µF per ampere of load current, plus a .47µF ceramic capacitor connected in parallel. The ceramic capacitors should be connected directly between each of the two amplifier supply pins and the ground plane. The larger capacitors should be situated as close as possible.
3. Use short leads to minimize trace capacitance at the input pins. Input impedances of 500Ω or less combined with the PA09 input capacitance of approximately 6pF will maintain low phase shift and promote stability and accuracy.
4. The output leads should also be kept as short as possible. In the video frequency range, even a few inches of wire have significant inductance, thereby raising the interconnection impedance and limiting the output slew rate. Also, the skin effect increases the resistance of heavy wires at high frequencies. Multistrand Litz Wire is recommended to carry large video currents with low losses.
5. The amplifier case must be connected to an AC ground (signal common). Even though it is isolated, it can act as an antenna in the video frequency range and cause errors or even oscillation.

TRANSIMPEDANCE BRIDGE FOR HIGHER DRIVE VOLTAGE

The circuit illustrated in Figure 8 drives the deflection yoke of a precision x-y display from an available ±15V supply. Only the bridge configuration can provide the high voltage drive levels required with the power supplies available. This enables the system to drive double the single amplifier output voltage. Consequently, the need for separate power supplies solely for CRT deflection is eliminated.

Figure 8 shows the current sense resistor R8 utilized to implement a differential voltage-controlled current source (transimpedance) with A1, where A2 functions as an inverter to provide an equal but opposite phase voltage drive to the load. To convert the single ended input to the differential output, the differential feedback of R1A through R1D makes the output voltage a common mode signal for A1 negating any feedback effects. In this manner, the amplifier common mode rejection and the resistive divider ratios, maintain the transimpedance function (differential feedback from R8 only). Because R1A/R1B and R1C/R1D must divide the output voltage equally for both amplifier inputs, a matched or precision resistor network must be used. In addition to initial matching, temperature tracking of the divider ratios is also critical. Mismatch errors are

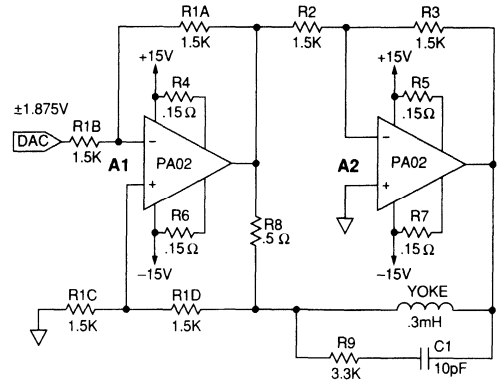


FIGURE 8. CURRENT-OUT BRIDGE DRIVE

equivalent to control voltages equal to the percent of mismatch multiplied by the output voltage of A1. The series R_C damping network placed in parallel with the inductive load reduces its phase shift at high frequencies, which effectively eliminates the possibility of oscillations.

The maximum transition time between any two points is 100µs for display ratings:

Yoke inductance = 0.3mH
Full-scale current = ±3.75A
DC coil resistance= 0.4Ω

Calculations are identical to previous examples:

$V = di*L/dt$ (19)
$V = 7.5A*0.3mH/100\mu s = 22.5V$ (20)
$V_{DROP} = 3.75A^* (.5\Omega + .4\Omega) = 3.375V$ (21)
$V_{DRIVE} = 22.5V + 3.375V = 25.875V$ (22)

One-half the total drive level required for the bridge circuit is provided by each amplifier, or approximately 13V of output swing per amplifier.

The Apex low voltage power op amp PA02 perfectly meets the criteria for this circuit because of its high slew rate of 20V/µs and its ability to drive the load close to the supply rail. The average output voltage swing of the circuit during the beam transition time will be greater than 26V as illustrated in Figure 9.

Due to the inductive nature of the load, the direction of current flow changes only after the transition is 50% complete. This allows both amplifiers to swing to their no load saturation levels (less than one volt from the supply rail) for this time period. Furthermore, IR drops during this time period generating voltages which add to the amplifier drive. During the second half of the transition, current direction changes and the amplifier output swing decreases; however, even at 75% completion, each amplifier will still swing in excess of 13V because the current magnitude has not yet reached 2A (see data sheet).

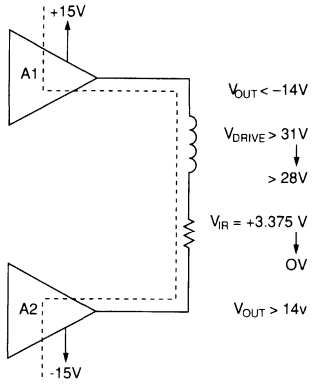


FIGURE 9. CURRENT PATH AND VOLTAGES DURING THE FIRST 50% OF A FULL SCALE TRANSITION

CONCLUSION

The capabilities of the power op amp provide higher accuracy levels, the ability to position beams in any desired position and to retain a steady state position. Having both the power and signals stage in one compact package offers space/weight advantages. The lower parts count increase reliability.

Power op amps are comparatively inexpensive and easy to use. They represent the most efficient solution to reducing development costs and decreasing design time.

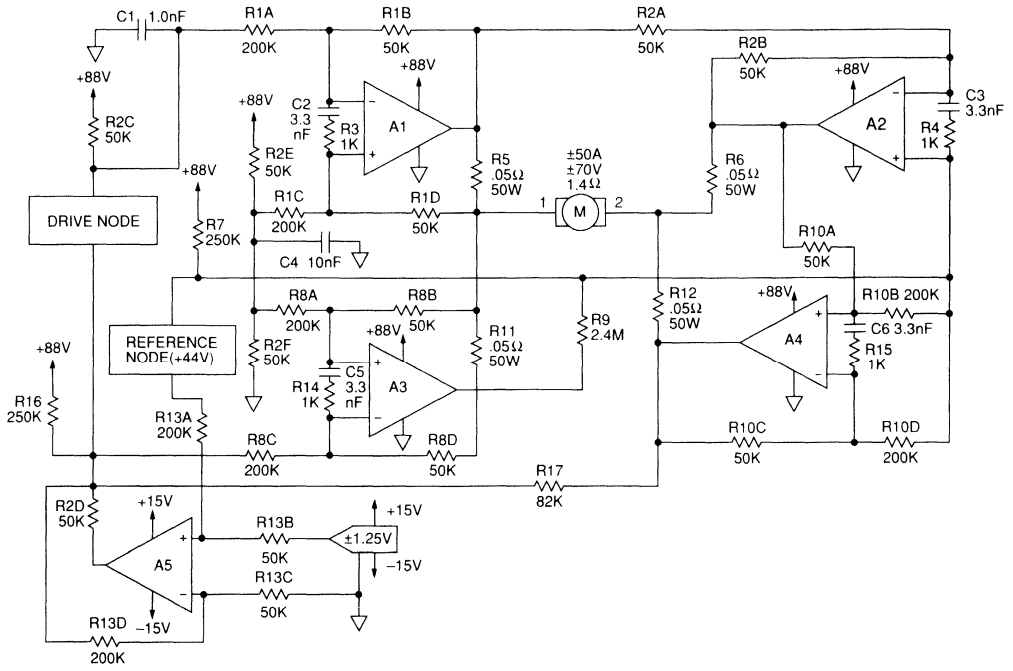


FIGURE 1. APPLYING THE SUPER POWER PA03

INTRODUCTION

The super power PA03 is the result of a design effort to substantially increase output power without sacrificing the high performance engineers are accustomed to when using small signal op amps. Thus, this new building block can perform accurate and complex tasks previously reserved to modular and rack mount devices.

The major applications for the PA03 will be in single ended circuits where up to 1,000W must be delivered to the load or in bridge motor servo systems delivering up to 2,000W peak. Linear motion control, magnetic deflection, programmable power supplies, and power transducer drives are typical of these applications. High power sonar, such as phased array, is another key application made possible by the accurate phase response and linearity of the class A/B output stage. Robot, motion control, and other high current applications which were previously impossible to implement with IC Power Op Amps because of power limits, are now possible using the PA03 as a building block.

The most powerful TO-3 hybrid IC's currently available can dissipate up to 125W and drive loads up to 250W (APEX PA12), while available monolithic IC's handle less. Where peak power requirements for dynamic motor control exceed 250W, three approaches were commonly used to increase power output: (1) parallel or bridge operation of two or more power op amps; (2) external booster transistors; (3) modular or rack mount power op amps.

While these options extend power capabilities, they can have major drawbacks in increased cost, excessive weight and reduced reliability. Furthermore, the large size can be a cumbersome design burden. System designers need a small, reliable power op amp capable of producing up to 1,000W while maintaining top notch performance. The PA03 meets this challenge!

Using the super power PA03 offers many advantages. With an internal power dissipation of up to 500W, the PA03's ratings top the previously most powerful op amp (Apex PA12) by a factor of *four*, and *one* PA03 is more cost effective and far more reliable than *four* less powerful op amps. Its thermal tracking of internal bias components makes the PA03 much safer to use under abnormal conditions than several units in parallel. Moreover, internal protection circuits insure that almost any power level not violating the 2,400W, 1ms Safe Operating Area (SOA) is safe. The amplifier will shut down upon overload, avoiding self-destruction. Internal current limiting resistors eliminate bulky, expensive milliohm external resistors which are normally required for power op amps. The common collector complementary output stage allows the output to swing within 4V of the supply rail at 12A and within 6V at 30A and has full shut-down control. This gives the designer a tool to protect sensitive loads or to minimize power consumption under battery operation. By operating in class A/B, it exhibits low crossover distortion, a feature hard to implement without the inherent thermal tracking of single package construction.

An external balance control option allows the already low offset voltage to be zeroed. The PA03's high overall accuracy makes it suitable for interfacing directly to photo-diodes; to build long time period integrators; or to design 12 bit and better resolution programmable power supplies.

The super power PA03 is a hybrid IC housed in the innovative Power-Dip dual in-line package. It has .060 pins on .200 centers to accommodate higher currents and allows layout on the standard 0.100 grid. The Power-Dip copper header of the PA03 provides 8.5 times the thermal conductivity, and three times the area of the conventional steel TO-3 package.

A SUPER POWER TORQUE DRIVE

The parallel bridge circuit in Figure 1 is shown to demonstrate several possible power enhancement techniques in one application. It operates in the transimpedance mode to drive the torque motor. This allows the D to A converter (DAC) to be programmed directly for delivered torque, since motor torque is directly proportional to armature current. The bridge uses an economic and efficient single output power supply and doubles delivered power levels again by increasing the current drive capability. Delete A3 and A4, and associated components if this option is not required.

Looking at the bridge configuration first, A2 and A4 invert the output of A1 and A3 with respect to the mid-supply reference node. Therefore, A2 and A4 drive the load equal to A1 and A3 in the opposite direction about the mid-supply reference point. The mid-supply node assures that neither amplifier saturates prematurely. Figure 2 shows the actual output voltages of A1/A3 and A2/A4 when delivering full scale output currents to the torque motor.

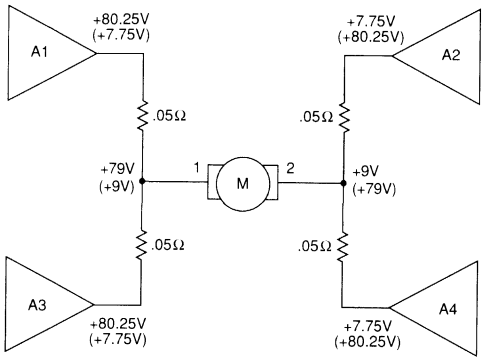


FIGURE 2. FULL SCALE DRIVE VOLTAGES

A5 (Figure 1) configured as a level shifter at a gain of 4, takes the 1.25V input from the DAC and swings the drive node to ±5V with respect to the reference node. A1 and A3 each amplify this differential 5V signal to a ±25A output level driving terminal 1 of the motor. A4 is a unity gain follower of the A2 output voltage. Since A2 and A4 have equal output voltages and equal current control resistors, they share the total 50A current equally.

The very low bias current of the PA03 FET input stage makes it possible to keep power dissipation low by using relatively large value precision resistors. This not only minimizes temperature variations in the resistive networks, but also reduces power dissipation in A5. Current balancing for both the reference and drive nodes is used to prevent level shifting of the high impedance nodes as a function of drive voltage. This is an easy task because of the symmetric drive levels with respect to the reference node.

Figure 3 shows a breakdown of the currents associated with the reference node. R2E and R2F form the basic voltage divider. At a zero drive level, the current through R13A and R13B will match the current through R7. The voltages applied to R1, R8, R9, and R10 will all be zero with respect to the 44V reference so the circuit is balanced. The voltages shown correspond to full scale drive level. R7 roughly balances the current through R13A and R13B to the +1.25V DAC input. R10A, R10B, R10C, and R10D current will nearly match the currents of R1C and R1D plus R8A and R8B. The differences encountered so far total 15 microamps, which is provided by R9 to insure the reference node remains at 44V.

Figure 4 illustrates currents associated with the drive node where R2C and R2D form the basic voltage divider. At zero drive, no voltage is applied to R17, R1 and R8, and the output of A5 will be zero and the drive node voltage will be 44 volts. This means currents of R2C and R2D balance. The currents in R16 balance the currents of R13C and R13D and the remaining resistor currents are zero. For a full scale input of +1.25V, A5 will drive to approximately +10V. The currents through R16, R13C and R13D are no longer balanced because the drive node voltage has risen to 49V. The currents through R1A and R1B, plus R8C and R8D, make the node even less balanced. R17 was selected to slightly over compensate the current imbalance. Since the differential circuit of A5 (Figure 1) controls drive node voltage, its

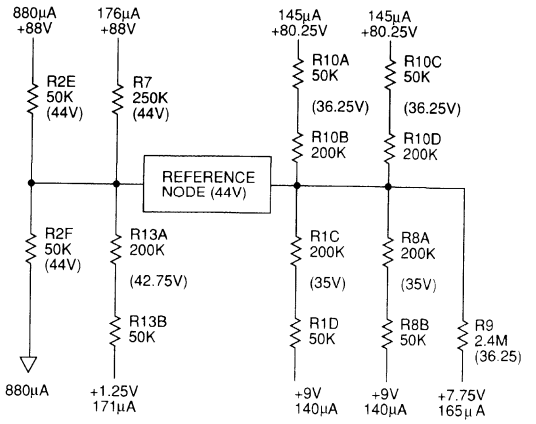


FIGURE 3. CURRENT BALANCING OF THE REFERENCE NODE

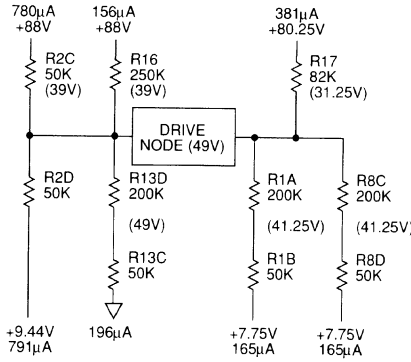


FIGURE 4. CURRENT BALANCING OF THE DRIVE NODE

nominal swing will be a 9.44V, correcting the overall current imbalance of 12µA. Thus the overcompensation of R17 insures A5 will not be required to swing beyond its rated 10V due to component tolerances.

There are a lot of resistor networks in the circuit, but each has a critical task. The ratios are most important to insure gain accuracy. In addition, ratio matching provides common mode rejection and differential voltage amplification. Specifically, the R13 quad around A5 sets drive node swing to +5V with respect to the reference voltage even though the reference changes with supply variations. Similarly, the R1 quad and the R8 quad set the full scale voltage across sense resistors R5 and R11 at ±1.25V. The ±35V output swings across the impedance of the torque motor are rejected as a common mode signal to maintain the programmed voltage to current transfer function. Thus impedance variations of the motor winding and the associated connections do not affect accuracy. R10 fixes the gain of A4 to unity while keeping its input pins about 4V closer to the reference than the amplifier's output voltage. With the output swinging to within nearly 7V of the supply rails, the common mode voltage requirement of ±Vs −10V is satisfied.

A PROGRAMMABLE POWER SUPPLY USING THE PA03

Figure 5 shows the PA03 in a simple, reliable programmable power supply which utilizes the PA03's shutdown features. It requires little calibration because the current to voltage conversion of the D to A converter output is done by the power op amp itself, and the 12 bit DAC80 provides accuracy levels high enough to eliminate the need for adjustments.

The programmable power supply is designed to test DC-to-DC converter modules drawing up to 15A. The majority of tests are

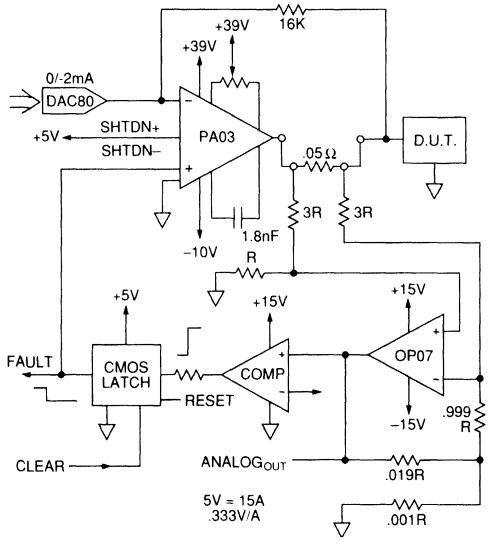


FIGURE 5. HI-POWER PROGRAMMABLE POWER SUPPLY APPLICATION

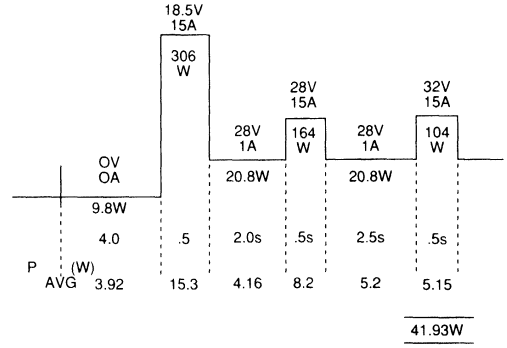


FIGURE 6. PROGRAMMABLE POWER SUPPLY INTERNAL POWER DISSIPATION

performed at 28V. High and low limits of 18.5V and 32V will be applied for 500ms. The outputs must be accurate to within 0.5% and survive an occasional short circuit to ground.

The OP07 differential amplifier circuit senses the D.U.T. current on the four-terminal shunt resistor, and provides a signal of 0.333V/A to the comparator. The comparator will trip at a current of 18A, setting the latch, and the latch then shuts down the PA03 until the fault is cleared and the latch is reset. This safety circuit limits arcing hazards in the test socket.

The feedback resistor of 16KΩ yields the required 32V full-scale output when the DAC output is 2mA. The 0.05Ω current sense resistor develops a 0.75V signal at the full-scale output current of 15A. This amplitude is a compromise between monitoring the current accurately without imposing an excessively high power rating on the sense resistor. However, the sense resistor still must be mounted on a heatsink due to 11.25W dissipation at 15A and the possible 88W at the built-in maximum current limit of 42A.

To derive the power supply voltage needed, the 0.75V drop on the sense resistor must be added to the headroom (supply-to-output differential) required by the op amp. From the PA03 specifications (a drop of 7V at 30A and 5V at 12A), a maximum drop of 6V at 15A can safely be assumed. Selecting a positive voltage of 39V leaves a margin of 0.25V. Without remote sensing, such a conservative approach is best due to potential IR drops in the high current leads. For the negative supply, a minimum operating voltage of 10V is required to satisfy the input common mode voltage specifications.

Four power levels must be examined to determine the worst case maximum power dissipation of the power op amp. The first three are the output voltage levels for the devices under test at the maximum current of 15A. Calculating all three shows the 18.5V output to be the worst case scenario. The 18.5V output plus the 0.75V drop across the sense resistor leaves a voltage of 19.75V across the output stage of the PA03. At 15A, this produces an internal power dissipation (including quiescent power of 9.8W) of 306W and a junction to case temperature rise of 92°C (PA03 =0.3°C/W).

Because the worst case power demand exists only for 500ms, an examination of average power and thermal time constants will help to reduce the heatsink size. Figure 6 shows the general test plan and the specific testing sequence with the resulting power dissipation levels demanded of the PA03. The 32V output level requires 103.6W (39V supply less 32V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for 500ms. The 28V level amounts to 163.6W (39V supply less 28V output and 0.75V across the sense resistor times 15A plus 9.8W of quiescent power) for another 500ms.

For the balance of the test of 4.5s, the maximum current of 1A amounts to 20.8W. During the minimum removal/insertion time of 4s, the power dissipation is only the quiescent power of 9.8W. This means the average power dissipated is only 41.9W. With a heatsink that has a thermal time constant of ten seconds, the highest peak (306W for 500ms) amounts to 5% of the time constant, or 4.9% of the rise for 306W continuously. Adding this spike equivalent of 15W to the 41.9W average will bring the peak short term equivalent power to 57.23W (though this peak could vary slightly depending upon the exact timing).

If, for reliability, a peak junction temperature of 150°C is selected, and a maximum ambient temperature of 38°C is assumed, the allowable temperature rise of the heatsink is 18°C (150°C– 38°C–92°C). At a peak short term equivalent of 52.2W, this requires a heatsink rated at 0.35°C/W. The Apex HS06 (0.6°C/W free air) with a forced air velocity of 500 ft/min can provide the required rating.

In this application, if abnormal situations arise due to faulty timing or defective test units, short term operation at the 306W level will not destroy the PA03 because the thermal shutdown will limit the temperature rise. The worst case would be a short in the test socket which could push the PA03 to a maximum current limit of 42A. At this current, the sense resistor (R_S) would drop 2.1V leaving 36.9V across the PA03. These current and voltage levels (1.55KW) are well within the PA03's 1ms second breakdown line of the SOA curve. Therefore, the fast response of the PA03's thermal shutdown circuit will protect the power op amp for the time required to eliminate the short.

REMOTE SITE MOON BOUNCE ANTENNA MOTOR DRIVE

Power conservation is essential for solar powered data gathering, while a considerable amount of motive force is required for positioning a 40 Ft dish antenna.

With a 3° beam angle and a position accuracy of 0.5°, the lunar angular velocity of 14.4°/Hr allows a position update only once per minute. The PA03's shutdown control used for intermittent operation combined with a worm gear drive to hold position during shutdown periods, facilitates an energy efficient positioning system.

The D to A Converter in Figure 7 converts position data to a voltage which is fed to the inverting input of the PA03 configured as an integrator by feedback capacitor C1 and input resistor R1. The precision reference and potentiometer apply a feedback voltage equivalent to actual position to the non-inverting input. The PA03 drives the motor with the integrated difference between the desired and actual positions. R2 acts as a damping element limiting the integration time constant to minimize overshoot.

The shutdown control is released for six seconds after each position update, which allows the PA03 sufficient time to position the antenna and reduces the standby power to 2W for 54 seconds or 90% of the time.

The normal current requirement of the motor is 8A, but under high wind conditions, up to 17A may be drawn. In this application, the amplifier output will be decaying pulse; thus driving the motor to a new position once a minute. Because the amplifier is at maximum

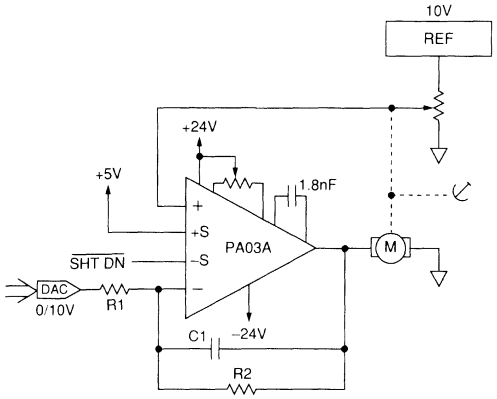


FIGURE 7. REMOTE SITE MOON BOUNCE APPLICATION

output (saturated) most of the time, the power dissipation at the full output voltage is the appropriate level to calculate.

At 17A the PA03 will drive to within 5.5V of the supply voltage (rail) dissipation of 93.5W. The quiescent current of 0.2A times the total supply voltage of 48V adds another 9.6W for a total of 103.1W dissipated in the amplifier. At the maximum ambient temperature of 45°C and a maximum junction temperature of 140°C, the allowable rise is 95°, which requires a thermal resistance for the heatsink as follows:

Q_{HS}= 95/103.1– 0.3 = 0.62°/W.

The Apex HS06 meets this criteria.

Under normal low wind conditions, the peak battery drain will be 201.6W. However, due to the 10% maximum duty cycle and the power-saving shutdown feature of the PA03, the average power consumption will be only:

P_{AV} = 0.1 (24*8+48*0.2) +0.9 (48 *0.040) = 22W

To further reduce standby power to 2W, the shutdown feature can be activated only when communications are required.

USING THE PA03 IN YOUR APPLICATION

To achieve maximum efficiency, the power supply voltage should be selected for the minimum voltage necessary to produce the required output.

For example, to obtain a ±45V output at 12A, add the supply-to-output differential as specified on the Data Sheet (±5V) to produce ±50V.

Dual supplies may be as high as ±75V and asymmetric or single supply operation is permitted as long as the total rail-to-rail voltage doesn't exceed 150V. Input voltages must always be at least 10V less than the power supply voltage due to the common mode voltage specification being supply voltage minus 10V.

Because of the greater power levels involved, the thermal path to remove the heat from the amplifier is of great importance to the successful application of the PA03. A 1°C/W rated heatsink may be suitable to remove 20-50W, but it is insufficient to handle 500W. For the PA03, a heatsink with a thermal resistance on the order of 0.1°C/W is often required such as: very large surfaces, forced air cooling, or even water cooling. Fortunately, if insufficient heatsinking is provided, the unique safety circuits of the PA03 will generally result in thermal shutdown rather than destruction. Destructive power levels are so high that in most applications they need not be of any concern.

As with all high current Power Op Amps, precautions must be taken to avoid current feedback due to voltage drops in the wiring of electromagnetic radiation. This is especially true when using the PA03 because of its higher current rating. The wiring for all supply and output leads must be done with wire equivalent to 12 gauge or thicker, as the PA03 has a higher current capacity than most branch circuits in residential wiring.

To avoid feedback through the power supplies, they must be bypassed with a ceramic capacitor of 0.47µF or greater, in parallel with a 10µF per ampere of peak output current (up to 300µF), mounted not more than 1.5 inches from the supply lines.

Even when using excellent bypassing components, good layout techniques and quality power supplies can easily cause substantial AC ripple. Ripple must be considered as a possible source of error. Positive feedback can also occur if the power supply also powers other circuit elements.

WATCH THE POWER DISSIPATION

The internal power dissipation (P) in a DC circuit is:

$$P = (V_S - V_O)\, I_O + (|+V_S| + |-V_S|)\, I_Q$$

where: I_Q: OUTPUT CURRENT
I_Q: QUIESCENT CURRENT
V_O: OUTPUT VOLTAGE
V_S: SUPPLY VOLTAGE

Errors often arise in the calculation if the wrong supply voltage is used. The voltage (V_S) must be the one at the supply pin sinking or sourcing the current. Incorrect selection of the worst case conditions (short to ground or supplies) can also create errors.

When driving reactive loads, due to the phase shift between output voltage and current, the power dissipation may be several times higher than the equivalent resistive loads. These have a totally different, but equally simple approach that can be used to obtain the correct power dissipation (P):

$$P = P_I - P_O$$

where: P_I = POWER DRAWN FROM THE POWER SUPPLY
P_O = POWER DELIVERED TO THE LOAD

Keep in mind that using purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier.

JUNCTION TEMPERATURES

The absolute maximum power dissipation of the PA03 is 500W and was derived using the industry standard derating procedure. This assumes operation at maximum junction temperatures (175°C) with the case at 25°C.

With the power dissipation and the maximum ambient temperature (T_A) of the application known, the operating temperatures of both case (T_C) and junction (T_J) of the power transistors can be determined:

$$T_C = T_A + P \cdot \Theta_{HS}$$

where: Θ_{HS} = THERMAL RESISTANCE FROM THE HEATSINK MOUNTING SURFACE TO AMBIENT AIR

Θ_{JS} = INTERNAL THERMAL RESISTANCE, JUNCTION TO CASE

Apply this to the PA03 by following these steps:

1. Calculate the maximum internal power dissipation (P).
2. Determine the maximum junction temperature allowable to achieve the desired reliability of the PA03. This must be less than 175°C. Apex recommends 150°C or less.
3. Calculate $T_J - T_A$, the allowable rise of the junction temperature above the maximum ambient temperature.
4. Calculate the required thermal resistance of the heatsink:
$\Theta_{HS} = (T_J - T_A)/P - \Theta_{JC}$

For example, in a circuit dissipating 300W at an ambient temperature of 30°C and the junction temperature not to exceed 150°C:

Θ_{HS} = (150 – 30)/300 – 0.3 = 0.1°C/W

HOW THE PA03 WORKS

The circuit diagram shown in Figure 8 shows that the input section of the PA03 is similar to most Apex FET input hybrid power op amps. Q21, D1 and D4 form voltage references to bias both input and output stages of the amplifier. Q31 is the current source for the input stage which consists of Q20A and Q20B (the FET input pair), Q17 and Q18 (the cascode transistors), and Q2 and Q3 (the half dynamic load). The current through Q5 sets the operating voltage (source-drain) for the FET input pair. Q12 acts as an impedance buffer between the high

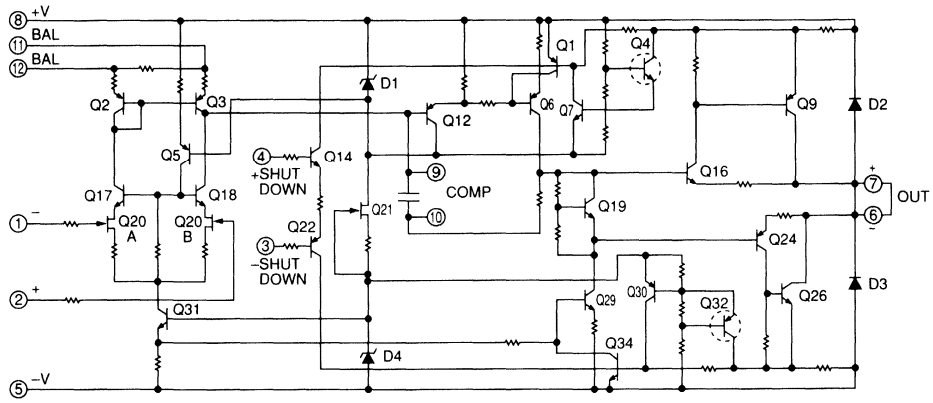


FIGURE 8. PA03 EQUIVALENT SCHEMATIC

output impedance of the input stage and Q6, the output driver.

The collector load of output driver Q6 consists of current source, Q29, and the output stage consisting of Q16, Q9, Q24, and Q26. The common collector configuration of Q9 and Q26 enable the PA03 output to swing close to the supply rails. Inverters Q16 and Q24, form local feedback networks which cause the output stage to be linear like an emitter follower with very high input impedance. The V_{BE} multiplier Q19, provides DC bias for the output transistors via Q16 and Q24, and is thermally coupled to the power dissipating transistors in the output stage. In addition, the V_{BE} multiplier utilizes thermistors to fine tune the temperature stability of the quiescent current through output transistors Q9 and Q26. This class A/B stage provides low crossover distortion, as well as stability of the quiescent current over the full temperature range.

D2 and D3 are high speed diodes which protect the output stage from inductive kickback by bypassing it into the supply rails. The 18.6 milliohm emitter resistors of Q9 and Q26 sense the output current of the amplifier. Currents in excess of 35 amps will develop .65 volts, thereby turning on Q1 or Q34. In turn, these transistors rob the base drive from Q6 or Q29, thus limiting the output currents to 35A. Q4 and Q32 are the sensors for the innovative SOA protection of the PA03. These two transistors are mounted directly on top of power transistors Q9 and Q26, eliminating thermal gradients and minimizing the response time to temperature changes in the output transistor junctions. The emitters of the sensors are connected to Q7 and Q30 which act as level translators to turn on current limit transistors Q1 and Q34, respectively. The complementary pair Q14 and Q22 activate the shut down of the PA03. While common mode voltage is rejected, differential voltages applied between these two transistors turn on the current limit circuit consisting of Q1 and Q34, thereby shutting down the entire output stage. In this mode the output pins appear as a high impedance to the load. Figure 9 illustrates the physical arrangements to achieve fast and reliable thermal shut down.

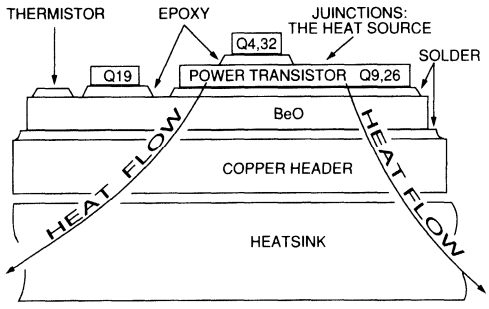


FIGURE 9. THERMO-MECHANICAL DESIGN

CONCLUSION

The PA03 is a versatile new building block which eases many design tasks and overcomes size and weight barriers which previously prevented implementation of linear power controls in limited space. The giant step up in power levels, improved protection circuits and high performance small signal characteristics make the PA03 a very cost effective innovation.

APPLICATION NOTE 7

POWER OPERATIONAL AMPLIFIER

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

INTRODUCTION

The programmable power supply (PPS) is not only a key element in automated test equipment, but it is also used in fields as diverse as industrial controls, scientific research and vehicular controls. When coupled to a computer, it bridges the gap from the software to the control task at hand. This application note examines the basic operation of the PPS, the multitude of possible configurations and the key accuracy considerations.

VOLTAGE OUTPUT VERSIONS

The most basic and often most accurate version of the PPS requires only a current output Digital to Analog Converter (DAC), a power op amp and a feedback resistor as illustrated in Figure 1. According to op amp theory, the voltage at the inverting input (summing junction) will be zero and op amp input current will be zero. As a result, all current from the DAC flows through the feedback resistor R_F. Ohm's law then causes the circuit to provide a precise output voltage as function of DAC output current. Given a perfect DAC and feedback resistor, only two op amp parameters contribute significantly to the output voltage errors. These are voltage offset (V_{OS}), modeled by the battery, and bias current (I_B), represented by the current source. Due to the high output impedance of the current output DAC in relation to R_F, V_{OS} errors appear at the output without gain.

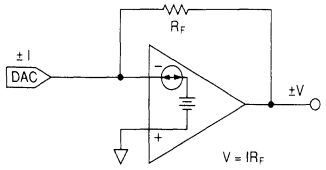


FIGURE 1. CURRENT TO VOLT CONVERSION

For a 10V output and op amp offset of 5mV, this error contributes only 0.05%. For a 100V output, a 0.5mV offset contributes an error of only 5ppm. Clearly, the DAC can easily be the major error source.

Op amp bias currents add to the DAC output current. The majority of available DAC's have full scale currents of ±1mA or 0/2mA. Most of today's bipolar input power op amps feature bias currents of less than 50nA. This results in errors of only 25 ppm maximum of the full scale range (FSR). FET input bias currents at 25°C are seldom over 100 pA and are specified as low as 10pA. These errors translate to 0.05ppm and 0.005 ppm. Since FET bias currents are generally characterized as doubling every 10°C, the bias current of the two examples could become 100nA and 10nA at 125°C, producing errors of 50ppm and 5.4ppm, respectively. Again,the DAC is the critical error source.

To determine the significance of the error contribution of a specific power op amp to the performance of various systems, refer to Table 1, next page. The least significant bit (LSB) is the value of the smallest step change of output. Comparing the calculated errors to the LSB values reveals system compatibility. For current output, DACs op amp bias currents compare directly with the DAC current LSB and V_{OS} errors compare directly with the full scale output voltage. Thus, the importance of low bias currents is dependent solely on system resolution. However, the significance of voltage offset specifications varies with both resolution and full scale voltage range.

USING VOLTAGE OUTPUT DACs

When using a voltage output DAC, the power op amp can be added with either inverting or non-inverting gain to form the PPS. It usually costs more than implementation with a current output DAC, and has less accuracy. However, system or logistic factors may dictate the use of the voltage output DAC.

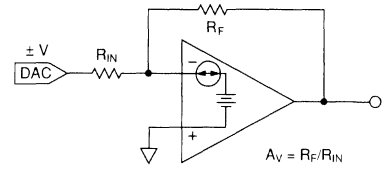


FIGURE 2. INVERTING VOLTAGE GAIN

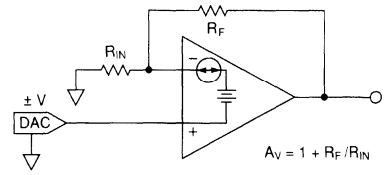


FIGURE 3. NON-INVERTING VOLTAGE GAIN

Figure 2 illustrates the basic inverting gain version and Figure 3 shows a non-inverting setup. Error calculations are still simple even though some new variables have been added. Voltage offset errors appear at the output multiplied by the gain of the circuit (A_V+1 for inverting circuits). To maximize accuracy, the highest output DAC's should be used with minimum voltage gains in the op amp configuration. When using ±10V DAC's, a direct Vos to LSB comparison can be made using the 20V FSR values listed in Table 1. Also, bias currents flow through the feedback resistor producing output voltage errors; thus, values of R_F and R_{IN} are usually kept as low as possible.

A CASE FOR REMOTE SENSING

The circuit of Figure 4 shows the wire resistance (R_W) from the power op amp to the load and back to the local ground via the power return line. A 5A load current across only 0.05Ω in each line would produce a 0.5V IR drop. Without remote sensing, this would become an error at the load. With the addition of the second ratio matched R_F/R_{IN} pair and two low current sense wires, IR drops in the power return line become common mode voltages for which the op amp has a very high rejection ratio. Voltage drops in the output and power return wires are inside the feedback loop; therefore, as long as the power op amp has the voltage drive capability to overcome the IR losses, accuracy remains high.

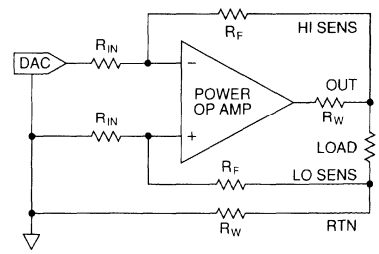


FIGURE 4. REMOTE SENSING PROGRAMMABLE POWER SUPPLY

CURRENT OUTPUT VERSIONS

A current output PPS using a current output DAC can be implemented as shown in Figure 5. Another version of the current output PPS is shown in Figure 6. This allows the load to be grounded, but is more complex and has additional errors. Especially if the output currents are relatively low, the current through the lower R_F/R_{IN} pair may become significant because it is also sensed by R_S. Major errors can be caused by ratio mismatching between the R_F/R_{IN} pairs. The resulting voltage errors across the sense resistor equal the output voltage times the ratio mismatch. For example, consider a 0.2Ω sense resistor, a 5A output requiring a 20V drive and a ratio mismatch of only 0.1% causes an error of 2%. Even an 8-bit LSB is only 0.39%!

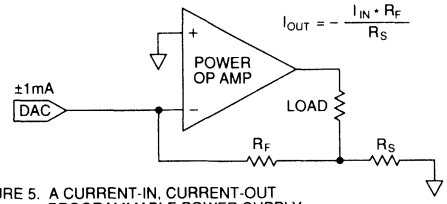


FIGURE 5. A CURRENT-IN, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

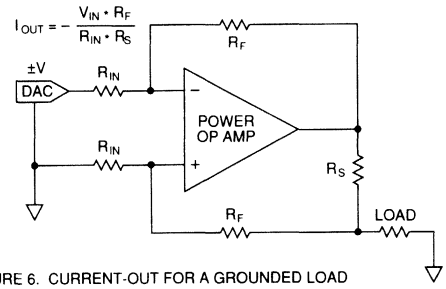


FIGURE 6. CURRENT-OUT FOR A GROUNDED LOAD

In all of the current output circuits discussed, errors due to voltage offset appear across the sense resistor at a gain of one or more. This means higher sense resistor values will minimize output current errors at the expense of increased power dissipation in R_S, the power op amp and system power supplies. One other word of caution, if the load contains inductive elements, refer to Applications Note 5 which discusses maintaining stability in precision current output circuits having reactive loads such as deflection coils. A current output PPS using a voltage output DAC is shown in Figure 7. The power op amp drives current through the load until voltage on the sense resistor (R_S) equals the input voltage. To achieve high efficiency (low voltage across R_S compared to the load voltage), this circuit requires a low voltage DAC or a high voltage op amp. If neither is possible, the circuit of Figure 8 allows the sense resistor voltage drop to be lower than the input voltage.

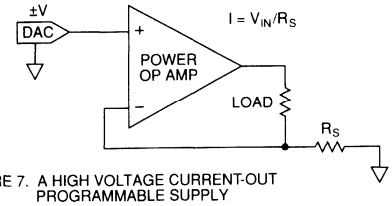


FIGURE 7. A HIGH VOLTAGE CURRENT-OUT PROGRAMMABLE SUPPLY

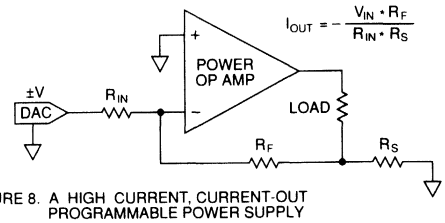


FIGURE 8. A HIGH CURRENT, CURRENT-OUT PROGRAMMABLE POWER SUPPLY

PROGRAMMABLE ACTIVE LOADS

To obtain the V-I characteristics of a power source, it may be desirable to control the output voltage and measure the output current or visa versa. The current output circuits shown are suitable as active current loads. The circuit of Figure 9 performs voltage loading of a solar cell panel. The power op amp forces the DAC voltage to appear across the panel and also performs an I to V conversion providing the data to plot V-I characteristics.

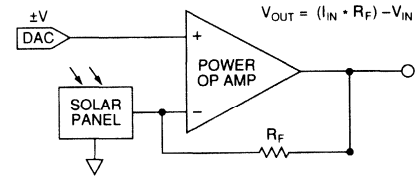


FIGURE 9. SOLAR PANEL TESTER

Due to its flexibility, accuracy and ease of use, the power op amp is the leading choice when programmable power supplies are called for. They greatly simplify circuits requiring unipolar outputs and are very cost effective when designing bipolar power supplies. The only remaining question is whether to buy the power op amp or to make one in discrete form. For low quantity production runs, the required design effort renders the "make" option too expensive. For high volume runs, the question is more involved. In many applications, the smaller size and lower weight plus high reliability, make the "buy" decision the only reasonable choice. (See "The Advantages of IC power op amps.") In all applications, the hybrid power op amp enhances design quality, speeds assembly and reduces overhead costs.

FULL SCALE RANGE					
BITS	PPM	2mA	20V	50V	200V
8	3906	7.8μA	78mV	195mV	.78V
10	977	1.95μA	19.5mV	48.8mV	195mV
12	244	488nA	4.88mV	12.2mV	48.8mV
14	61	122nA	1.22mV	3.05mV	12.2mV
16	15.3	30.5nA	305μV	.763mV	3.05mV

TABLE 1. LSB VALUES FOR VARIOUS OUTPUT LEVELS

THE MODERN POWER OP AMP

Power op amps are attractive because they reduce circuit design time enormously. Assembly costs of the power op amp design amount to a fraction of the discrete counterpart due to vastly reduced parts count. Careful attention to the power aspects of a circuit is required, as the well known op amp design rules based on low power devices. The objectives are to maximize reliability plus optimize output power and system efficiency. This application note points out some optimizing techniques and some areas to be especially watchful.

INTERPRETING SPECIFICATIONS

The first step in achieving high power levels is to operate within specifications. This means check the data sheet first. Apex data sheets are divided into product description, absolute maximum ratings, specification table, typical performance graphs, and application hints. Each section should be checked for relevant information.

Absolute maximum ratings are stress levels which, when applied to the amplifier one at a time, will not cause permanent damage. However, proper operation is only guaranteed over the ranges listed in the specifications table. For example, most amplifiers have an absolute maximum case temperature range of –55°C to 125°C. If the specified operating temperature range is less, i.e. –25°C to 85°C, an amplifier may latch to one of its supply rails when operating above that temperature (+85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area. Simultaneous application of two or more of these maximum stress levels, such as maximum power and temperature, may induce permanent damage to the amplifier.

The generally accepted industry method of specifying absolute maximum power dissipation assumes the case temperature is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick to compare ratings of various manufacturers. However, it is not a reliable operating point. An ideal heatsink is required, and even with the best heatsink, it would still result in reduced product life due to operation at extreme temperatures. APEX recommends maximum junction temperature of 150° or less.

The specifications table should be the prime working document while designing the application. In addition to the minimum/maximum parameters (voltage offset, output capability, etc.), this table contains the guaranteed linear operating ranges: common mode voltage, temperature ranges, power supplies, etc.

Typical performance graphs are most useful in determining performance variation as operating conditions change. For example, all amplifiers are specified for a minimum voltage output at maximum current rating. If your application needs only 75% of this current, you might determine from the typical graph you will gain 0.5V at this level. A safe design will assume output capability of 0.5V better than the specification table, not the actual number on the typical graph. Bear in mind, if your design is based on the typical performance graphs, it will statistically work 50% of the time.

OPTIMIZING THE POWER SUPPLY

To deliver the most output power and achieve maximum efficiency, internal power dissipation must be minimized. This condition is met if the power supply voltage is selected for the minimum voltage necessary to produce the required output. Internal power dissipation is the sum of quiescent power *plus* the product of output current *and* the supply to output differential. Supply voltage is the only variable for the designer to optimize. Refer to the product data sheet's specified minimum supply to output differential voltage. Each extra volt here dissipates one more watt for every ampere of output current. Trade-offs in this area are not recommended. Deriving required outputs from existing system supplies reduces efficiency if the difference between supply and required output exceeds the supply to output differential of the op amp. Also, this supply vs. efficiency trade-off must be considered when contemplating the use of unregulated supplies. When using unregulated supplies, line and load variations must be taken into consideration along with the ripple content of the supply. The result is a voltage band above the minimum operating voltage required by the power op amp to produce the required output. Power in this band must be dissipated. Voltage above the minimum operating voltage decreases the power handling capability of the power op amp.

The choice is whether to dissipate the power in the power op amp or in a separate regulator. As current levels increase, the dollar per watt cost generally rises faster for the power op amp than it does for a DC regulator.

Usually, unregulated supplies are not economical because they lack transient protection. Power lines are notorious for being extremely noisy. They have high voltage, high speed spikes riding on the sine wave which pass right through the power transformer. Furthermore, the large electrolytic capacitors used for filtering often do not have low equivalent series resistances at those high frequencies. A 1K volt spike on the incoming line can result in an excessive voltage spike at the amplifier supply pin. Destruction of the op amp may be the result. Therefore, line filters and zener clamps are required to eliminate the voltage spikes; thus, the economy of unregulated supplies is reduced.

Once the minimum supply voltages above have been selected, steps need to be taken to minimize IR losses. Some of today's modern hybrid power op amps handle currents higher than most branch circuits in residential wiring. Losses can be kept to a minimum, especially as frequencies increase, if leads are as short as possible between supply and amplifier, as well as between the amplifier and the load. In the video frequency range, where even a few inches of wire have significant inductance, and the skin effect increases the resistance of heavy wires at high frequency, multi-strand litz wire is recommended.

SINGLE OR ASYMMETRIC SUPPLY OPERATION

Asymmetric output swings present another opportunity to optimize power supplies. Consider the circuit of Figure 1. If the symmetric power supplies were used, power dissipation would be substantially increased, a power op amp with a higher voltage rating would be necessary and output power would be reduced.

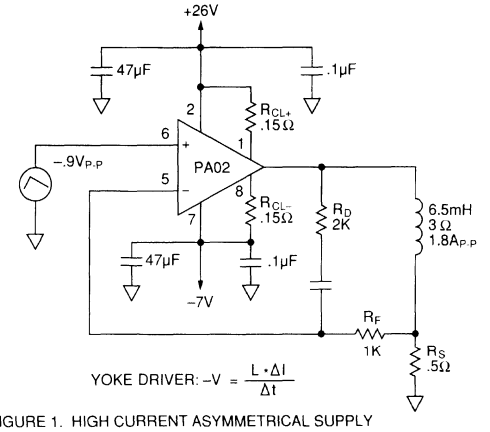


FIGURE 1. HIGH CURRENT ASYMMETRICAL SUPPLY

Fortunately, most power op amps are suitable for operation from a single supply voltage. The common mode operating requirements do, however, impose the limitation that the input voltages not approach

closer than 5 to 10 volts to either supply rail (determined by the common mode voltage specification). Thus, single supply operation requires the input signals to be biased 5 to 10V from either supply rail. Figure 2A illustrates one bias technique to achieve this.

Figure 2A illustrates a very practical alternative to single supply operation, a second low voltage supply. This allows ground referenced input signals, but also maximizes the voltage swing of the unipolar output. The 12 volt supply in Figure 2B must usually supply only the quiescent current of the power op amp unless the load is reactive or EMF producing.

KNOW YOUR POWER DISSIPATION

Power requirements of the load are most often well known, but

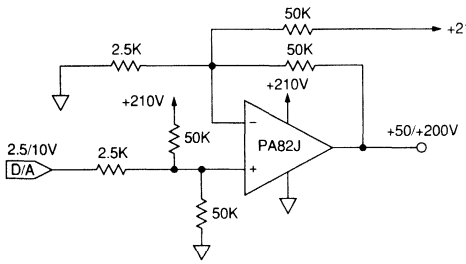


FIGURE 2A. TRUE SINGLE SUPPLY OPERATION

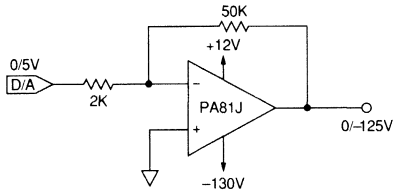


FIGURE 2B. ASYMMETRIC SUPPLIES

calculating the power dissipated inside the amplifier is not always simple.

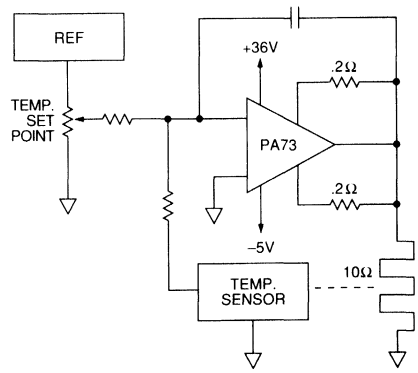
For purely resistive loads, maximum internal power dissipation occurs when the output voltage equals half the supply voltage. This is the worst case to analyze if the amplifier does not have to withstand short circuits. An example of DC application is the temperature controller in Figure 3.

Programmable power supplies (PPS) for automated test equipment must often tolerate short circuits in the device under test. For the PPS shown in Figure 4, the worst case dissipation will occur with a short to one of the 24V DUT supplies if the PPS is programmed to the opposite voltage. Assuming the current limit of the 24V supply is greater than the PPS limit, the PPS goes into current limit with considerably higher power levels than encountered under normal operation. Worst case for the amplifier could be its supply voltage plus the DUT supply voltage times the current limit.

AC OUTPUTS ALLOW HIGH POWER LEVELS

If an AC drive has a frequency of 60Hz or greater, the halfwave period of the power dissipating waveform is shorter than the thermal time constant of the power amplifier. The resultant power averaging between the output transistors results in a lower thermal resistance. This lower thermal resistance immediately increases the power handling capability of a given amplifier.

Apex data sheets provide both AC and DC ratings of thermal resistance. Power levels specified on both the absolute maximum



MAX INTERNAL POWER	MAX OUTPUT POWER
1/2 V_S = 18V	V_{OUT} = 28V
I_{OUT} = 1.8A	I_{OUT} = 2.8A
P_{OUT} = 32.4W	P_{OUT} = 78.4W
P_{INT} = 32.4W	P_{INT} = 22.4W

FIGURE 3. TEMPERATURE CONTROL CIRCUIT POWER LEVEL

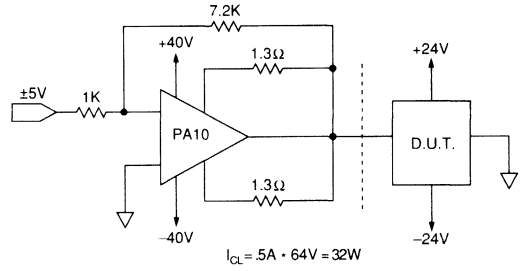


FIGURE 4. PPS POWER DISSIPATION CONSIDERATIONS

rating and the power derating typical performance graphs are based on DC thermal resistance. This means an AC only application is capable of delivering more power or running cooler (more reliably).

Sine wave circuits share a similarity with DC circuits. Maximum internal RMS power dissipation occurs when the peak output voltage swings to 63.7% of supply voltage. Maximum internal power may be calculated as follows:

$$P = V_{SS}^2/(2\pi^2 * R_L)$$

Where: V_{SS} = total rail-to-rail supply voltage
R_L = load resistance

REACTIVE LOADS INCREASE DISSIPATION

When driving reactive loads, more caution is required due to the phase difference between V_O and I_O. The actual power dissipation may be several times higher than the equivalent resistive loads. In such cases, It is best to use a totally different, but equally simple, approach to calculate power dissipation (P):

$$P = P_I - P_O$$

Where: P_I = Power drawn from the power supply
P_O = Real power delivered to the load

In calculating P_I, use DC supply voltage and RMS output current. For example, a 1A RMS output, with supplies of ±15V, means 15W plus quiescent current * 30V.

Driving purely reactive loads means that all power drawn from the supplies is dissipated in the amplifier because the load power factor is reduced to zero.

DEALING WITH MOTOR DRIVES

Motor control applications often place brutal requirements on the driving circuit. Section A of Figure 5 shows two output transistors of a power amplifier and the motor with its ratings. It is important to recognize that the winding resistance and the voltage rating of the motor alone do not determine the running current. The back EMF of the motor must also be considered when calculating the running current. This EMF can be modeled as a battery whose voltage is proportional to instantaneous velocity as shown in Section B of Figure 5.

When the amplifier is given a reversal command, it changes its output very quickly while the actual speed and EMF can diminish only as fast as mechanical system inertia is dissipated. The initial result of the vastly different response times between the electronics and the mechanics is shown in Section C of Figure 5. The amplifier has responded to its new drive command, but the EMF has not yet had time to change.

The model shows that if the amplifier could produce the programmed output level of –24V, a total of 36V would be applied across the winding resistance developing a current on 9A. In this situation, the output voltage is determined by the current limit of the amplifier rather than the control voltage. The programmed limit of 4A through the winding resistance produces 16V. Adding the initial 12V EMF places the amplifier output voltage at -4V. With 24V across the conducting transistor, the internal power dissipation is eight times the level encountered in steady state operation. Failure to analyze this situation has taken the lives of many power op amps.

A useful technique to maximize available power for steady state running requirements is to limit the rate of change of the drive voltage to approximately the same limitation imposed by the inertia of the mechanical system. In this manner, the extremely high power levels described can be avoided. In other words, fast reversal times can be traded off for high levels of running torque.

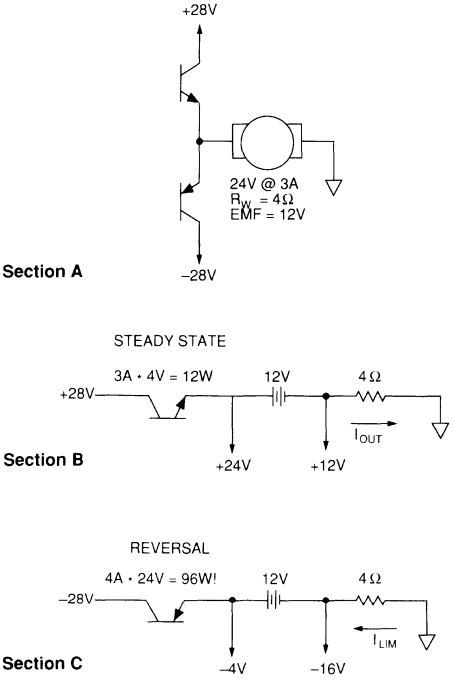


FIGURE 5. POWER DISSIPATION IN MOTOR DRIVES

CIRCUIT DESIGNS TO INCREASE OUTPUT POWER

Two power op amps configured in a bridge circuit can double power levels. To illustrate the advantages of the bridge circuit, Figure 6 shows a composite where alternate connections transform the circuit from single ended to a bridge. A1 is a standard single ended power op amp which would drive the 4 ohm speaker. If A2 is added, it completes a bridge circuit. The resulting doubling of the voltage drive would be suitable for an 8 ohm speaker. With this trick, not only are power levels doubled, but the same supply is capable of powering either circuit. This is possible because the single ended circuit peak current demand utilizes only 50% of the supply capability. In contrast, the equal and opposite drive characteristics of the bridge circuit loads both positive and negative supply rails equally during each half cycle of the signal.

Parallel operation is often used to increase output current or wattage. However, due to their low output impedance, power op amps cannot be connected in parallel without modifying the circuits. Figure 7 illustrates one method of doing this. This uncommitted *master* amplifier, configured as required to satisfy the circuit function, has a small sense resistor inside its feedback loop. The *slave* amplifier is a unity gain buffer. Thus, the output voltages of the two amplifiers are equal. If the two sense resistors connected to the load are equal, the amplifiers share current equally. More slaves may be added as desired.

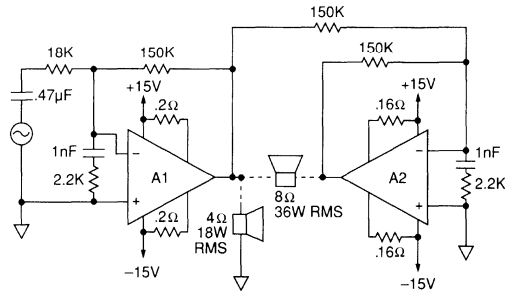


FIGURE 6. DOUBLING POWER WITH A BRIDGE

There are two factors to consider in the selection of the sense resistors. First, the output current will produce a voltage drop which adds to the supply requirements. Second, the voltage offset of the slave appears across the sum of the two sense resistors. Thus, a small current will circulate strictly between the two amplifiers. This wastes power. When this technique is used, it is recommended that inputs be limited in such a way that they demand only 50% of the typical slew rate of the amplifier. This prevents two amplifiers with different slew rates from generating large currents between each other during fast transitions.

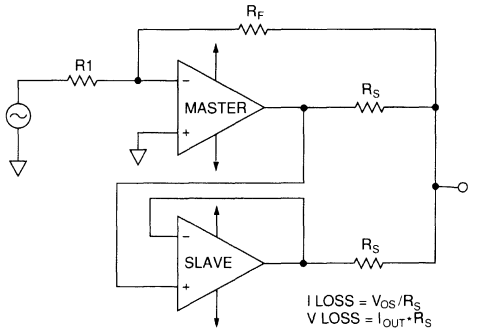


FIGURE 7. PARALLEL OPERATION

PROPER HEATSINKS INCREASE OUTPUT POWER

With a given power op amp, the larger the heatsink is, the higher attainable output power can be. Furthermore, as power levels increase, it is more cost effective to use a larger heatsink.

To minimize space and weight, forced air cooling or even liquid cooling is often used with power amplifiers. While obviously easier to implement, forced air cooling gives a maximum improvement of only about 2:1. At higher power levels, liquid cooling becomes a more attractive option. Reasonable heatsink ratings, which can be achieved given an area 6 inches square and 2 inches tall, are 0.85°C per watt for free air cooling, 0.4°C per watt for forced air, and 0.05°C per watt for a liquid cooled system. See the Apex application note on heatsinking for more information.

THERMAL SHUTDOWN CAN HELP

Internal thermal protection can increase output power under nominal operating conditions because the amplifier shuts off when the substrate temperature exceeds safe limits. This allows the amplifier circuit design to be based solely on normal conditions but prevents excessive temperature during abnormally high power conditions.

The thermal shutdown feature is especially valuable in circuits such as programmable power supplies (PPS). Here the output voltage is the normal operating voltage of the unit under test. Occasionally the unit under test will be defective which may short the output of the PPS to ground; thus, power levels increase substantially. Thermal shutdown will simply shut the device off rather than lead to destruction. Thermal shutdown is not a panacea for all problems. It does not mean to disregard the second breakdown curves of the safe operating area. Assume the time constant for operation of the thermal shutdown is 250-500ms. This means the worst case power levels should not exceed the steady state second breakdown line of the SOA curve.

OPTIMIZING IS A TEAM EFFORT

Apex power op amps employ unique thermistor circuits that provide superior control of internal currents and offer exceptional specifications plus a superb quality record. With careful attention to design of the application, the end result will be advanced products of greater value.

1-800-421-1865

FOLDOVER CURRENT LIMITING WHAT IT IS-WHAT IT DOES

Apex PA10 and PA12 power amplifiers are unique in that they offer the option of foldover current limiting. This type of current limiting offers the opportunity to operate these amplifiers with a better match to the safe operating area (SOA) envelope than conventional current limiting. Because of this capability the PA10 and PA12 can maximize power delivered while minimizing risk to the amplifier.

CURRENT LIMITING CIRCUITS

The simple current limiting circuitry shown in Figure 1 consists of a current sensing transistor across the emitter resistor of the power device which acts to fix the maximum current flow without regard to voltage stresses on the power device. SOA limitations are based on a combination of current and voltage stress on the power device, and simple current limiting is sensitive only to the current stresses. Figure 3 graphically shows the possible output voltages and currents for a PA12 with a fixed 3A current limit operated on ±50 volt supplies. Superimposed in solid lines is the 25°C SOA of the PA12. The amplifier is capable of wide excursions beyond the SOA as designated by the unsafe regions shown. To avoid SOA violations in such a circuit would require a severe derating of output current capability. To make the circuit safe for shorts to ground,for example, would limit current capability to 2.5A. Even more difficult would be making the circuit safe for shorts to either rail or large back EMF's. Then the current limits would have to be set at 300 milliamps!

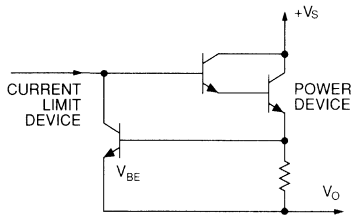
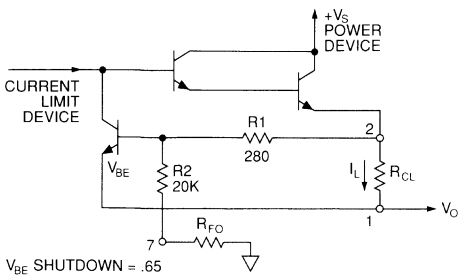


FIGURE 1. SIMPLE CURRENT LIMITING



$$V_{BE} = [V_O + I_L R_{CL}][(R_2 + R_{FO})/(R_1 + R_2 + R_{FO})] - V_O \quad (1)$$

$$V_{BE} = [V_{RCL}][(R_2 + R_{FO})/(R_1 + R_2 + R_{FO})] - [V_O][R1/(R_1 + R_2 + R_{FO})] \quad (2)$$

1. R_1 , $R_2 + R_{FO}$ divider action reduce available drive from V_{RCL} when close to + rail (large V to ground).

2. With V_O at 0, $I_{CL} = .65/R_{CL}$, since R_1 , $R_2 + R_{FO}$ ratio only causes slight attenuation, i.e., with $R_{FO} = 0$ (ground pin 7), $I_{CL} = [(.65)(.986)]/R_{CL}$.

FIGURE 2. FOLDOVER LIMITING CIRCUIT

FOLDOVER IMPROVES THE MATCH BETWEEN SOA AND POWER DELIVERY

Foldover can be used to increase current capability at full output swing, or can be used with reduced current limits for the same current capability at full swing with improved conformance to SOA requirements. Figure 4 shows the effect of grounding pin 7 on the circuit shown for Figure 3. The effect is to tilt the output capability of the PA12 for a better match to the safe output area. The current capability is now up to 5.75A at full output swing. There is still a considerable unsafe region and shorts to ground are not safe. The original amplifier shown in Figure 3 had a current capability of 3A, while Figure 4 is actually capable of much more. A better match of the 3A output requirement and SOA can be effected by using foldover and re-calculating current limit resistors.

Figure 5 shows the output capability vs. SOA for foldover with a .385 ohm current limit resistor which would normally be used for a fixed 1.6A current limit. Note that the output capability map now nearly matches the SOA of the PA12, yet a full 3.25A is available at full output swing. Shorts from output to anything are safe in this application. As a comparison, Figure 6 shows the same circuit with the foldover pin 7 open and foldover disabled. The fixed 1.6A current limit normally would have much larger unsafe regions if foldover were not utilized.

Figures 7 and 8 show similar examples for a PA10 operated on ±20 volt supplies with a desired current of 4A. Once again, optimum use of foldover requires recalculating current limit resistors. The lower supply voltages result in a less dramatic effect on the part of the foldover circuit. The difference in current limit values over the range of output voltage swings are not as large.

DESIGNING WITH FOLDOVER

To ease the design of current foldover schemes, Equation A is included to determine R_{CL} at a particular output voltage for the desired current capability at that voltage. Equation B will then give the current capability at $V_O = 0$. Further mapping of output capability can be done with Equation D, which is the same as Equation 3 in the PA12 data sheet. Mapping of output capability superimposed with SOA can be a useful tool in foldover limiting design. Maps as shown here are created by outlining the SOA on a graph of current vs. voltage and superimposing calculated output values. Preferably, points can be plotted on product SOA graphs to determine performance vs. SOA. Figure 9 shows how the performance of Figures 3, 4 and 6 appear plotted against the SOA graph of the PA12.

When using current foldover, some of the possible unusual behaviors which can occur should be considered. Behavior with a resistive load does not normally present any problems and will usually be predictable. Non-linear loads such as reactive loads and current

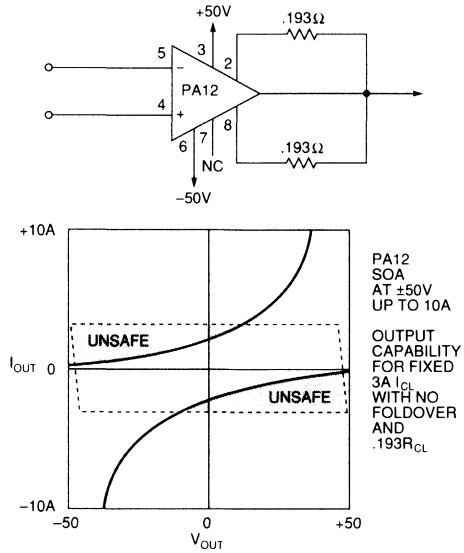


FIGURE 3. NO FOLDOVER .193Ω R_{CL}

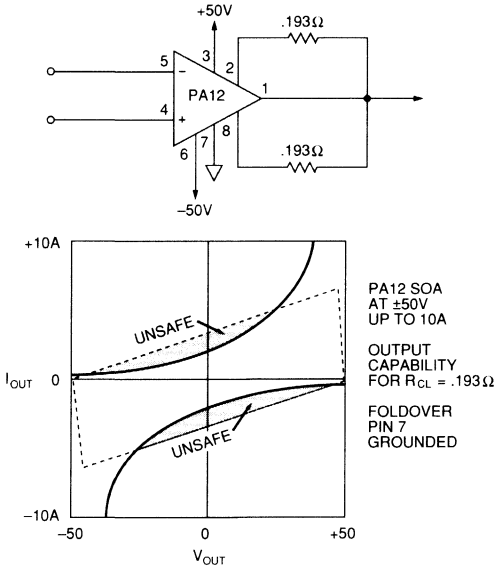


FIGURE 4. .193Ω R_{CL} WITH FOLDOVER

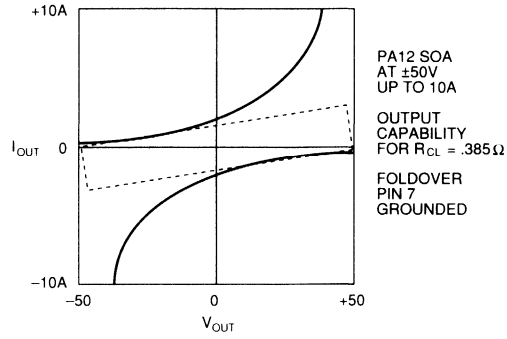


FIGURE 5. .385Ω R_{CL} WITH FOLDOVER

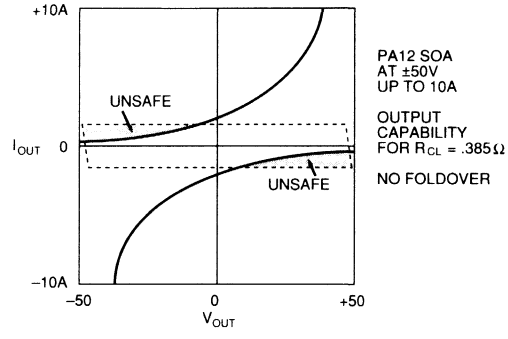


FIGURE 6. .385Ω R_{CL} NO FOLDOVER

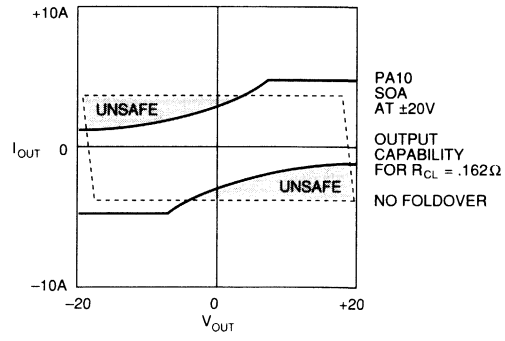


FIGURE 7. .162Ω R_{CL} NO FOLDOVER

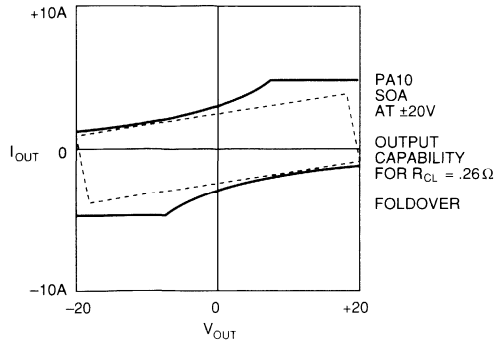


FIGURE 8. .26Ω R_{CL} WITH FOLDOVER

sources or sinks of any type should be tested carefully. Because voltage and current stresses on output devices are shifted in phase with reactive loads, foldover can interfere with reactive load driving and analysis can become complicated. In some cases instability can result from the use of foldover with reactive loads. Distortion can occur at points in the waveform where high currents are required at low output voltages, enough to prevent proper drive to the load. This shouldn't necessarily be looked at as a limitation of the use of foldover, since very often this condition may have resulted in an SOA violation if simple current limiting was used.

SAFE OPERATING AREA (SOA)

An example of a non-linear load effect could be simulated with a high compliance 4A current sink as a load, combined with an amplifier represented by the performance graph of Figure 5 and illustrated in the schematic of Figure 10. If the amplifier was operating at an output voltage greater than 30 volts and the current sink were connected, the output would remain at 30 volts and provide the proper 4A current to the load. However, if the current source were connected to the amplifier output with the amplifier at 0 volts out, as soon as voltage rises, the sink will attempt to draw 4A. This exceeds the current capability of the amplifier at this low output voltage and the output voltage would be unable to increase. This "two stable-state" behavior of current foldover circuitry is a manifestation of its negative resistance behavior, and this is the mechanism which can cause oscillation in conjunction with reactive loads.

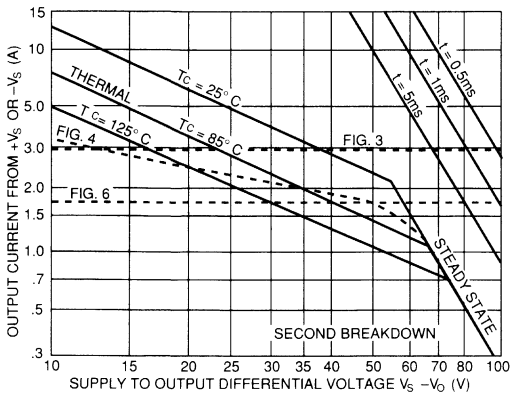


FIGURE 9. OUTPUT PLOTTED AGAINST SOA

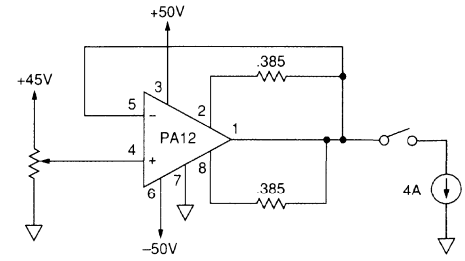


FIGURE 10. NON-LINEAR LOAD TEST

ADDITIONAL DESIGN EQUATIONS

If you know:

Current required at full swing, use Equation A.

Equation A:

$$R_{CL} + .01^{*} = \frac{.65\left(\frac{(.28 + 20) + R_{FO}}{20 + R_{FO}}\right) + V_O\left(\frac{.28}{20 + R_{FO}}\right)}{I_{LIM}}$$

Simplify by approximation: $(.28 + 20) \approx 20$

$$RCL + .01^{*} = \frac{.65 + V_O\left(\frac{.28}{20 + R_{FO}}\right)}{I_{LIM}}$$

Current required at 0 volts out, use Equation B.

Equation B:

$$R_{CL} = \frac{.65}{I_{LIM}} - .01^{*}$$

Current required at full swing without using R_{FO} (ground pin 7), use Equation C.

Equation C:

$$I_{LIM} = \frac{.65 + V_O\left(\frac{.28\ Vo}{20}\right)}{R_{CL} + .O1^{*}}$$

If you want current limit at output voltage between zero and full swing, use Equation D.

Equation D:

$$I_{LIM} = \frac{.65 + \left(\frac{.28}{20 + R_{FO}}\right)}{R_{CL} + .01^{*}}$$

* .01Ω = wire bond and pin resistance to R_{CL} connections.

POWER AMP OUTPUT IMPEDANCE
APPLICATION NOTE 10
POWER OPERATIONAL AMPLIFIER

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INTRODUCTION

In the design of power amp circuits, the need often arises for a power amp model with specified output impedance. Most often, this requirement revolves around the need to accurately predict the phase performance of power amp circuits.

Output impedance of any op amp is modified by the feedback network present around the device. In voltage source type circuits, the effect of the network is to reduce the output impedance by a factor equal to the ratio of open loop gain to closed loop gain. In power amps, the net result is an effective output impedance of milliohm levels at frequencies below 1kHz. Wiring and interconnections often create larger impedances than the output impedance of the closed loop power amp. Therefore, output impedance will play a minor role in the phase performance at low frequencies. At high frequencies, reactive load considerations are already addressed by capacitive load specifications given on many power amplifiers.

Current control circuits, or current sources, include the load as a series element in the feedback loop with a sense resistor developing a voltage proportional to load current. Figure 1 shows a generalized example of just such a circuit. The load often consists of an inductive element such as a deflection yoke which can have up to 90° of phase shift at higher frequencies. Totally accurate prediction of phase in the feedback loop might at first seem to involve the series equivalent of output impedance and yoke impedance. In reality, it's because the feedback the op amp is operating as a true current source with an impedance approaching infinity. A realistic approach to stabilizing the circuit merely involves an auxiliary feedback whose effect dominates before the combination of yoke feedback and amplifier phase approaches 180°. Output impedance is not necessary to determine stability.

It is also important to realize that output impedance of a power op amp is not related in any way to power delivery capability or internal losses. A model of a power amp with the output resistance in series with the output will develop inordinate losses which are not observed in real world op amps.

Output impedance is dependent on several variables such as frequency, loading and output level. Often, the impedance will rise at higher frequencies. A class C amplifier, such as PA51 or PA61, will exhibit higher impedances at lower levels due to bulk emitter resistance effects in the emitter follower outputs.

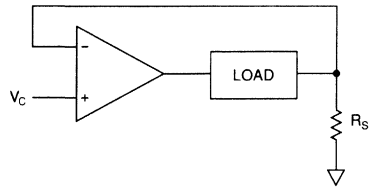

FIGURE 1. GENERALIZED CURRENT CONTROL CIRCUIT

OUTPUT IMPEDANCE MEASUREMENT

Several methods are available to measure output impedance. The simplest method is to measure open loop gain in loaded and unloaded conditions. This method measures the dynamic impedance in series with a perfect voltage source. Variations in output with loading are due to this impedance.

A more direct method is to generate a signal which is impressed into the output of an amplifier operating under open loop conditions. A measurement of current will determine the effective impedance that this signal is looking into.

ACTUAL IMPEDANCE VALUES

Several Apex power amplifiers were measured using the gain variation with loading method. The test circuit of Figure 2 was loaded with 10 ohms. To establish uniformity of measurement, the smallest possible amplitude at 10Hz was used. Where a range of values is shown, it represents a range observed for several devices.

PA02: 10-15 ohms
PA07: 1.5-3 ohms
PA08: 1500-1900 ohms (high voltage amplifier)
PA09: 15-19 ohms
PA10: 2.5-8 ohms
PA12: 2.5-8 ohms
PA19: 30-40 ohms
PA51: 1.5-8 ohms
PA61: 1.5-8 ohms
PA84: 1400-1800 ohms (high voltage amplifier)

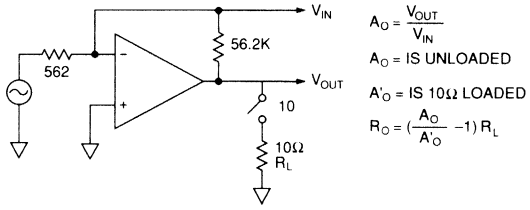

FIGURE 2. OUTPUT IMPEDANCE MEASUREMENT CIRCUIT

The high voltage amplifiers are much lower in current capability than the high current amplifiers. As a result, the higher impedance is to be expected.

The high impedance shown for PA19 is a result of the drain output MOSFET circuit without local feedback at the output stage. This is an example of how this parameter can be misleading. If 30 to 40 ohms of resistance were in series with the output, then the PA19 would never be capable of greater than 1 amp of output current. Under closed loop conditions, the output impedance is reduced to milliohm levels like any other power amplifier. Keep in mind the output impedance is an abstract term as far as output voltage and current capability are concerned.

To demonstrate the effect of output impedance when modeling, use the highest and lowest expected values. The results will verify that output impedance plays an insignificant role in power amp performance.

APPLICATION NOTE 11

POWER OPERATIONAL AMPLIFIER

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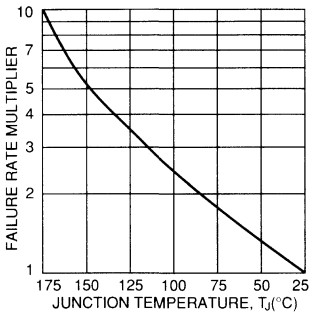
THERMAL MANAGEMENT

As power op amps shrink in size and become more powerful, the importance of a good thermal design is more critical than ever. Most importantly, reliability is a direct function of internal component temperatures and dissipated power. Furthermore, as the amplifier case rises above 25°C, derating factors do not just reduce the allowable power level. Voltage and current offsets drift, current limits change and, sometimes even dynamic performance is affected. This application note discusses thermal management starting with actual dissipation vs. allowable dissipation, the common cooling options, how to achieve maximum performance with sound mounting techniques, as well as the benefits of thermal capacity.

Thermal management techniques must be applied to remove as much heat as possible from the semiconductor junction, thereby maintaining minimum operating temperatures and maximum reliability. A further goal is to minimize the effects of the removed heat on other devices. Figure 1 shows the average of NPN and PNP power transistor failure rates at elevated temperatures relative to operation at 25°C. All electronic components encounter similar increased failure rates.



This data was extracted from the base failure rate tables of MIL-HDBK-217C, revision of 1 May 1980.

FIGURE 1. MTTF VS. TEMPERATURE

MAXIMUM POWER RATING

θ_{JC} is the thermal resistance from junction to case. A great deal of effort has been put into minimizing this thermal resistance. It is the major specification affecting power handling capability. When allowing for a case temperature of 25°C and maximum junction temperature, the maximum internal dissipation rating is developed.

$$P_{MAX} = (T_{JMAX} - 25°C) / \theta_{JC} \quad (1)$$

This rating is consistent with rating methods of most transistor manufacturers and should not be confused with advertised output power which is highly application dependent. Before using this rating, check for factors which might degrade the rating such as actual ambient temperature (T_R), heatsink thermal resistance (θ_{HS}) mounting, and in some cases, an isolation washer.

The optimum heatsink to case thermal resistance (θ_{HSC}) for a TO-3, using thermal grease and a mica isolation washer, is 0.375°C/watt. Without the washer, this is reduced to 0.1°C/watt. APEX amplifiers have an isolated case which negates the need for isolating the mounting surface and the mounting screws. Some vendors require isolation washers.

$$P_{MAX} = (T_{JMAX} - T_A)/(\theta_{JC} + \theta_{HS} + \theta_{HSC}) \quad (2)$$

To illustrate the importance of analyzing θ_{JC}, rather than using advertised ratings, Table 1 compares a 150W (output) rated amplifier (non-isolated) to the APEX PA12 rate at 125W (dissipation). For a stipulated audio application, the thermal resistance used is the typical AC rating and the power level is 100W for both devices. The table shows the 150W (output) device junction rises twice as much resulting in questionable reliability at just 100W. An ideal ambient temperature and infinite heatsink are assumed.

	150W Output	125W Dissipation
θ_{JC}	1.6	.8
θ_{CS}	.375	.1
Delta T_C	37.5	10
Delta T_J	197.5	90

TABLE 1. COMPARING TEMPERATURE RISE

SYSTEM LAYOUT

Thermal management starts with determination of actual dissipation and should result in a layout of an optimized thermal system to convey the heat to the ambient environment. In systems using natural convection, heat sources should be separated as widely as possible. In contrast, systems using high velocity air or liquid cooling perform optimally when localizing these devices. Understanding convection and radiation may help avoid layout related problems. Since convected heat rises, it is best to place the heat sources near the top of the enclosure and avoid having temperature sensitive circuits above or near the heat sources. The hot air should flow in its natural vertical direction using vertical board and fin orientation. Heatsinks should be oriented so air can pass freely over all the fins.

MOUNTING THE AMPLIFIER

The thermal joint from the case to heat sink, θ_{HSC}, is very important from both design and production points of view. Extreme care must be taken in this small but critical area. Heat generation occurs near the top of the silicon chip and typically spreads downward at an angle of 45° as it travels through the various materials to the heatsink. The 8 pins of the package surround the heat source. Unfortunately, the glass seals present a high thermal resistance to heat flow toward the outer edges of the package. To maintain optimum heat flow, heatsink material should never be removed from the inside of the pin circle. For example, drilling one large hole rather than eight small holes to mount an amplifier will increase thermal resistance dramatically.

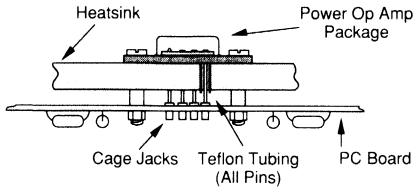
Figure 2 illustrates a common mounting setup employing direct wiring, using cage jacks and mating sockets. A consistent and stable thermal joint vs. time, including temperature cycling, is an absolute must. Compression washers will help to accomplish this. The washers have a spring-like quality that maintains a constant pressure over temperature. Steel screws should be torqued from 4 to 7 inch-pounds. If the assembly process includes a flow or wave solder step after the device has been mounted and torqued down, re-torquing is required. Torque control is one of the least expensive but more effective ways to maintain the thermal resistance over time.

There are a number of thermal compounds that have been successfully used for years to fill tiny gaps between cases and heatsinks. Most of these products work well, but a word of caution is in order. The shelf life for most thermal greases is indefinite when sealed in its container, but the vehicle and the thermally conductive part may separate. If the separated material is used, the resultant joint will have poor thermal properties. Mixing the components back into solution restores the material's thermal properties. To make the re-combination easier, it is best to purchase the grease in a jar instead of the more common tube. In one year, life tests at 100°C with compression washers, the thermal joint did not degrade. However, this vehicle evaporated leaving a dry joint. This does not degrade the thermal resistance provided the joint is not loosened.

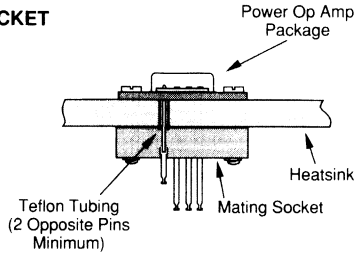
For the heatsink, a vast array of devices are available. The proper match of heatsink to actual power dissipation, in accordance with "Heatsink" in "General Operating Considerations" section, will maintain a safe junction temperature and determine whether the circuit is

"indestructible" or has unpredictable failures. Please note that altitude, air pressure, flow rate, and power level all have a major influence on heatsink efficiency. Also, a word of caution: forced air heatsink ratings are usually functions of linear feet per minute (FPM) or air flow, while fan ratings are usually given in cubic feet per minute (CFM). For example, a four inch diameter fan at 50 CFM pushes that volume through only 0.87ft² producing 573 FPM at the fan. Also keep in mind that if you reduce the airflow cross section below that of the fan, you must consult its static pressure curves.

PC BOARD



MATING SOCKET



DIRECT WIRE

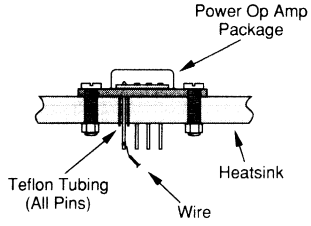


FIGURE 2. MOUNTING TECHNIQUES (CROSS SECTION VIEWS)

When utilizing structural elements to dissipate heat, it is advisable to check the proposed mounting area. Surfaces must be flat and have a smooth finish. The extrusion flatness of 4mils/inch and a surface finish of 63 micro inches are typical of commercial heatsinks. This is perfectly acceptable in applications using TO-3 packages where heatsink compound is used and results in a θ_{HSC} of 0.1°C/W as noted under power rating. For high power applications or packages larger than the TO-3, a surface flatness of 1 mil/inch is recommended.

THERMAL CAPACITY

The power levels that can be achieved in the pulse mode of operation are elevated far above those of steady state operation. This is due to the thermal capacity of the heatsink. As heat is first applied, the rate at which the case temperature increases can be compared to its electrical equivalent, the voltage build up on a capacitor of a R-C network. Figure 3 displays this analogy.

The thermal capacity of a mass is the product of its density, specific heat and volume. In most tables, the density is given in gm/cm³ (multiplied by 16.39 to yield gm/in³). The specific heat is usually in units cal/cm–°C. To obtain the more familiar units of watts-sec/°C, convert by multiplying by 4.1819. The thermal time constant (Tau) is equal to the product of thermal resistance and the thermal capacitance. This time constant defines the rate at which the material reaches thermal equilibrium. The time required to achieve 95% of the equilibrium temperature is 3 times the thermal time constant.

To illustrate the principle, aluminum has a density of 2.7cm/cm³ (44.245gm/in³), and specific heat of .220cal/gm–°C, yielding 9.734cal/°C or 40.71 watt-second/°C per cubic inch. Using the conversion factor of 10.22 cubic inches per pound, and the Apex HS05 heatsink weight of 1.04 pounds, results in a volume of 10.63 cubic inches and a thermal capacity of 434 watt-second/°C. The time constant for this heatsink is the thermal resistance of 1.1°C/W x 434 watt-second/°C, or approximately 346 seconds. The thermal resistance rating used above is for a free air mounting only because application of forced air reduces both thermal resistance and thermal time constant. Thermal capacity remains constant.

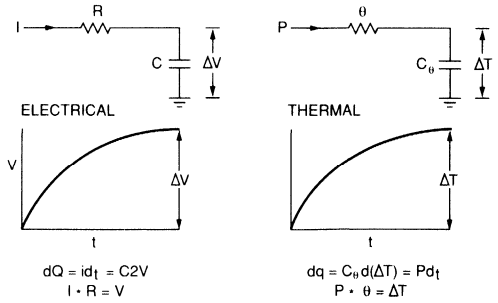


FIGURE 3. ELECTRICAL AND THERMAL MODELS

If power is applied as a single pulse, the case temperature follows the curve in Figure 4. The delta T in °C for both heating and cooling follow these equations :

$$\text{delta } T_{HEAT} = W^{*}\theta_{HS}\,(1-e^{-t/tau}) \quad (3)$$

$$\text{delta } T_{COOL} = \text{delta } T_{HEAT}(e^{-t/tau}) \quad (4)$$

The Figure 4 curve indicates that thermal capacity plays a major role when the duty cycle is extremely low.

Figure 5 shows the initial response to application of repetitive pulses. The pulse train is repetitive when the duty cycle does not allow the circuit to return to its initial temperature between pulses. The following procedure will predict operating temperatures after the heatsink has reached equilibrium. Peak power is multiplied by duty

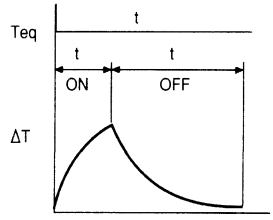


FIGURE 4. SINGLE PULSE RESPONSE

cycle to arrive at average power. The average temperature of the case will be $T_A + (P_{AVERAGE} * \theta_{HS})$. To determine the peak power, the pulse duration and time constant are substituted into equation 3 above. Then 1/2 delta heating is added to average temperature to yield the maximum case temperature. This case temperature should be used in conjunction with the SOA curves to determine the maximum power available from the device.

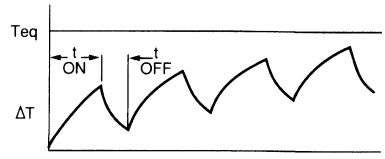


FIGURE 5. REPETITIVE PULSE RESPONSE

CONCLUSION

Thermal management optimizes space, cost and size for your power levels and temperature range. When properly applied, it will get the heat out and keep your circuits cool; thereby, maintaining the highest possible reliability and performance.

VOLTAGE TO CURRENT CONVERSION

Voltage controlled current sources (or VCCS's) can be useful for applications such as active loads for use in component testing or torque control for motors. Torque control is simplified since torque is a direct function of current in a motor. Current drive in servo loops reduces the phase lag due to motor inductance and simplifies stabilizing of the loop.

VCCS's using power op amps will assume one of two basic forms, depending on whether or not the load needs to be grounded.

CURRENT SOURCE: FLOATING LOAD

Figure 1A illustrates the basic circuit of a VCCS for a floating load. The load is actually in the feedback path. R_S is a current sense resistor that develops a voltage proportional to load current.

Note the inclusion of resistor R_B in Figure 1A and subsequent figures where non-inverting VCCS's are described. This resistor is present to prevent the non-inverting input from floating when the input voltage source is disconnected or goes to high impedance during the power on cycle. R_B provides a path for input bias current of the amplifier and commands the amplifier output current to zero in cases where V_{IN} is disconnected or goes to a high impedance. Figure 1B shows an implementation of a VCCS for a floating load. At low frequencies the added components Cf, Rd, and R_F have no effect and are included only to insure stability. Considerations for these components are discussed in the section on "Stabilizing the Floating Load VCCS" covered later in this application note.

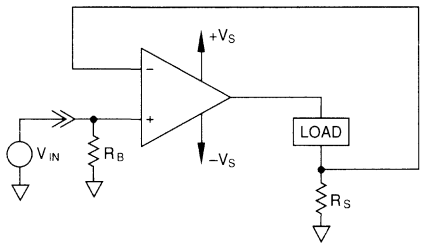


FIGURE 1A. BASIC VCCS FOR FLOATING LOAD

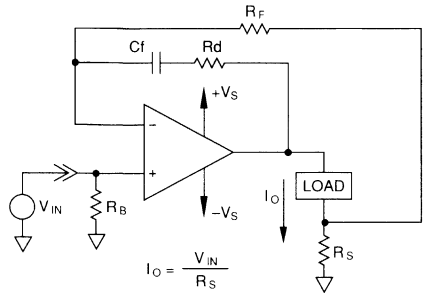


FIGURE 1B. VCCS FOR FLOATING LOAD WITH STABILITY COMPENSATION

The amplifier's loop gain will force the voltage across R_S to assume a value equal to the voltage applied to the non-inverting input, resulting in a transfer function of:

$$I_O = V_{IN}/R_S$$

Several variations are possible for this basic circuit. It is not necessary to have a direct feedback connection from R_S to the inverting input; components can be included to raise the gain of the circuit. Figure 2 shows a higher gain version with its equivalent transfer function. Higher gain circuits will lose some accuracy and bandwidth, but can be easier to stabilize.

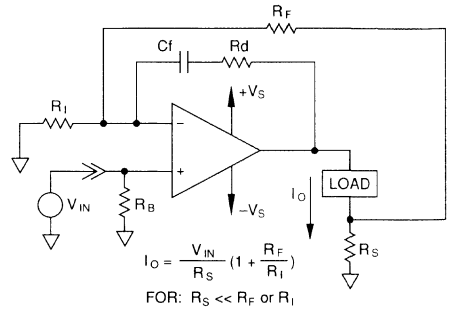


FIGURE 2. VCCS FOR FLOATING LOAD; INCREASED GAIN CONFIGURATION

Figure 3 shows an inverting VCCS. The input voltage results in an opposite polarity of current output. Just as in the case of inverting voltage amplifiers, the advantage of not having any common mode variation at the amplifier input is higher accuracy and lower distortion.

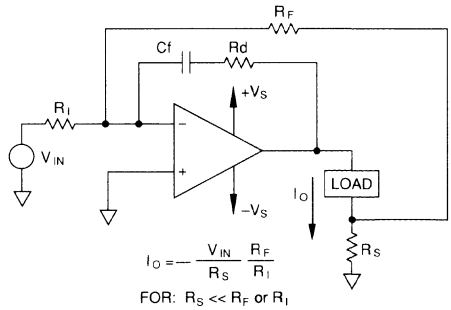


FIGURE 3. VCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

Figure 4 is a current input version which is actually a CCCS, or current controlled current source. This is truly a current amplifier. This circuit could be useful with current output Digital-to-Analog Converters (DAC's), or in any application where a current is available as an input.

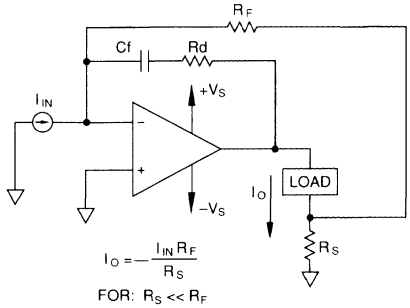


FIGURE 4. CCCS FOR FLOATING LOAD; INVERTING CONFIGURATION

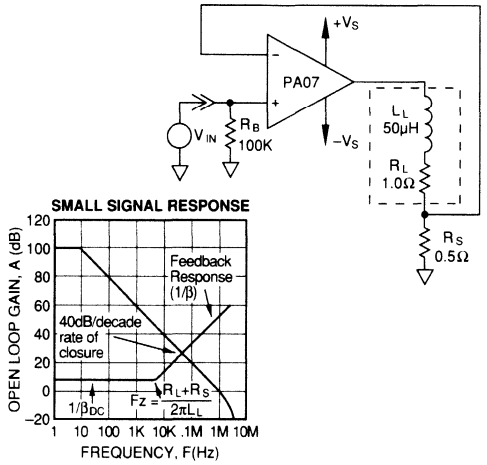
STABILIZING THE FLOATING LOAD VCCS

Because the load is in the feedback loop on all of these circuits, it will have a significant effect on stability. If the load was always purely resistive, the analysis would be simple and many circuits would not require any additional components (such as Cf and Rd) to insure stability. In the real world however, we usually find ourselves using these circuits to drive such complex loads as magnetic coils and motors.

Stability analysis is most easily accomplished using **"Rate of Closure"** techniques where the response of the the feedback is plotted against the amplifier open loop gain. This technique uses information easily obtained on any amplifier data sheet.

Rate-of-closure refers to how the response of the feedback and amplifier Aol intersect. If the slope of the combined intersection is not over 20 dB per decade, the circuit will be stable.

For an example, consider the amplifier of Figure 1A. Assume a PA07 amplifier with a 0.5 ohm current sense resistor will be used to drive a 50 µH coil with 1 ohm of series resistance. In Figure 5 we have superimposed on the Aol graph of the PA07 the response of the load and sense resistor.



$$\beta_{DC} = \frac{.5\Omega}{1.5\Omega} = .333 \rightarrow 1/\beta = 9.5dB \qquad Fz = \frac{1.0\Omega + .5\Omega}{2\pi\ 50\mu H} = 4.77kHz$$

FIGURE 5. PLOTTING FEEDBACK RESPONSES

The intersection of the responses exhibits a combined slope of 40 dB per decade, leading to ringing or outright oscillation. Let's refer to that point as the **"critical intersection frequency."** Compensation for this circuit is best accomplished with an alternate feedback path; the response of which will dominate at the critical intersection frequency.

A good criteria for the response of the alternate feedback would be:

1. A response which dominates by at least an order of magnitude (20 dB) at the critical intersection frequency.
2. The alternate feedback response should have a corner occurring at a frequency an order of magnitude less than the critical intersection frequency.

To provide this response, the alternate feedback components have been selected to provide the compensating response illustrated in Figure 6. A_B in Figure 6 is the dominant feedback path the amplifier will see in its closed loop configuration. R_F merely acts as a ground leg return impedance for the alternate feedback loop, and should be a low value between 100 and 1000 ohms. Rd is then selected to provide the desired high frequency gain, and Cf is selected for the alternate feedback corner.

Note that these are similar to techniques used to stabilize magnetic deflection amplifiers described in Apex AN #5, **"Precision Magnetic Deflection."**

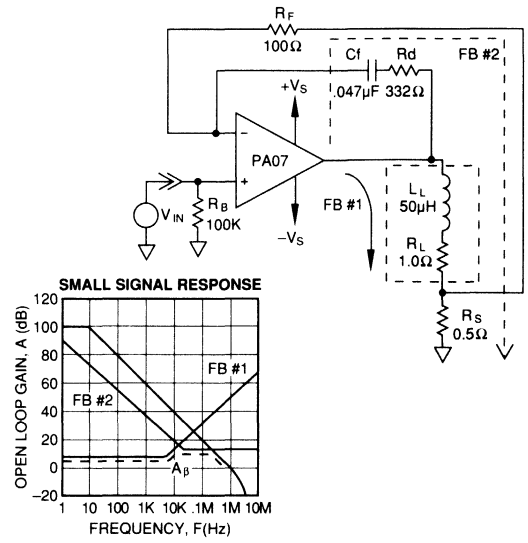


FIGURE 6. COMPENSATING THE AMPLIFIER

CURRENT OUTPUT FOR GROUNDED LOAD

The VCCS for a grounded load is sometimes referred to as the **"Improved Howland Current Pump."** It is actually a differential amplifier which senses both input signal and feedback differentially.

Figure 7 shows a general example for this VCCS with its associated transfer function .

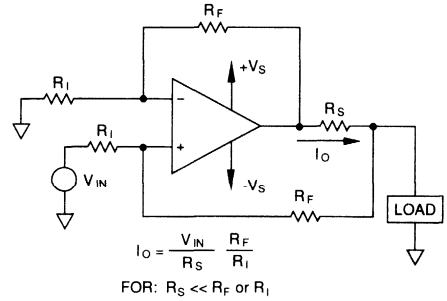


FIGURE 7. VCCS FOR A GROUNDED LOAD

First among the special considerations for this circuit is that the two input resistors (R_I), and the two feedback resistors (R_F), must be closely matched. Even slight mismatching will cause large errors in the transfer function and degrade the output impedance causing the circuit

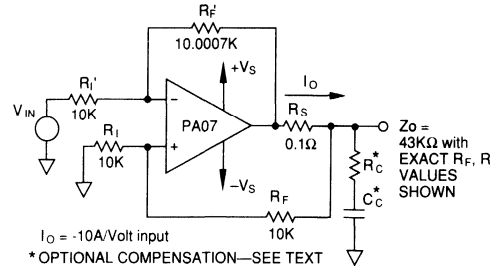


FIGURE 8. ACTUAL PA07 VCCS

to become less of a true current source.

As an example of the matching requirement, consider the actual example using PA07 in Figure 8. Matching the resistors as closely as tolerances permitted produced an output impedance of 43 K ohms. A 1% mismatch reduced output impedance to 200 ohms and introduced nearly 20% error into the transfer function.

This suggests that matching to better than 0.1% is required which is probably best accomplished with prepackaged resistor networks with excellent ratio match. The circuit of Figure 8 actually required a slight amount of mismatch in the two (R_F) resistors to compensate for mismatches elsewhere, suggesting that the inclusion of a trimpot may be necessary to obtain maximum performance.

STABILITY WITH THE GROUNDED LOAD CIRCUIT

The grounded load circuit is remarkably forgiving from a stability standpoint. Generally, no additional measures need to be taken to insure stability.

Any stability problems that do arise are likely to be a result of the output impedance of the circuit appearing capacitive. The equivalent capacitance can be expressed as follows:

$$Ceq = \frac{R_I + R_F}{2\pi foR_IR_S}$$

Where: fo = THE GAIN-BANDWIDTH PRODUCT OF THE AMPLIFIER

This capacitance can resonate with inductive loads, resulting most often in ringing problems with rapid transitions. The only effective compensation is a simple **"Q-snubber"** technique: determine the resonant frequency of the inductive load and output capacitance of the circuit. Then, select a resistor value one-tenth the reactance of the inductor at the resonant frequency. Add a series capacitor with a reactance at the resonant frequency equal to one-tenth of the resistor value. An alternate method would be to put a small inductor and damping resistor in series with R_S.

Also keep in mind that the equation favors larger values of R_I and R_S, and the use of op amps with better gain-bandwidth to reduce effective capacitance. In circuits where good high frequency performance is required, this will necessitate increasing either or both R_I and R_S with the upper limits being established where stray capacitance and amplifier input capacitance become significant.

An infrequent second cause of instability in this circuit is due to negative resistance in the output impedance characteristic of the circuit. This problem can be solved by trimming the feedback resistors to improve matching.

THE CURRENT MIRROR

The current mirror circuit is a handy device for generating a second current that is proportional to input current but opposite in direction.

The mirror in Figure 9 must be driven from a true current source in order to have flexible voltage compliance at the input. Any input current will attempt to develop a drop across R1 which will be matched by the drop across R2 causing the current through R2 to be ratioed to that in R1. For example, if R1 were 1.0 K ohm and R2 were 1 ohm, then 1 mA of input current will produce 1 Amp of output current.

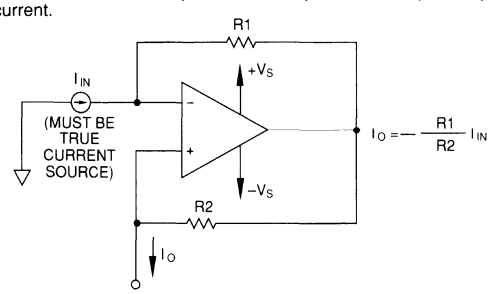


FIGURE 9. CURRENT MIRROR

APPENDIX A.

RATE-OF-CLOSURE AND FEEDBACK RESPONSE

Rate-of-closure stability analysis techniques are a method of plotting feedback response against amplifier response to determine stability.

The closed loop gain of any feedback amplifier is given by:

$$Acl = Aol/(1-\beta Aol)$$

Where: Aol IS THE OPEN-LOOP GAIN OF THE AMPLIFIER, AND Acl IS THE RESULTANT CLOSED LOOP GAIN

β is a term describing the attenuation from the output signal to the signal fed back to the input (see Figure 10). In other words, β is the ratio of voltage fed back to the amplifier over the amplifier's output voltage. (Vfeedback=βVout)

In the examples used in this application note, the plotting of β versus amplifier response is facilitated by plotting an equivalent closed loop response (1/β) of the amplifier circuit and superimposing this response on the amplifier open loop response. This **"equivalent closed loop response"** is also referred to as noise gain, Av (n).

In the example in Figure 5, the curve referred to as feedback response is actually representative of the closed loop noise gain response of the amplifier due to the feedback network consisting of yoke and sense resistor. In Figure 6, an additional feedback response for Cf, Rd, and R_F is plotted independently of all other responses. There are several important points to be noted in the use of these graphs:

1. In the case of multiple feedback networks such as in Figure 6, the response with the lowest noise gain at any given frequency will be the dominant feedback path. In Figure 6 this dominant feedback path is labelled A_β.
2. Whenever the noise gain and open loop gain intersect with a combined slope, or rate of closure, exceeding 20 dB/decade, poor stability will result. 40 dB/decade will definitely oscillate since this represents 180 degrees of phase shift. An example of this is shown in Figure 5.

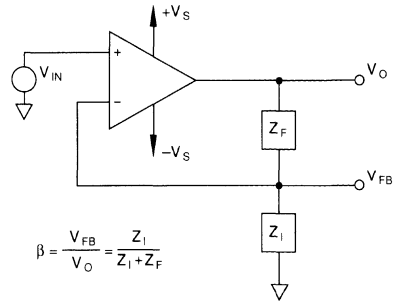


FIGURE 10. FEEDBACK FACTOR, β

APPLICATION NOTE 14

POWER OPERATIONAL AMPLIFIER

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

The Apex PB series of power booster amplifiers, PB50 and PB58, are high performance, yet economical and flexible, solutions to a wide variety of applications. Their voltage and current ratings of up to 200 volts at 2 amps for the PB50, and 300 volts at 1.5 amps for the PB58, satisfy most high voltage and high current requirements. In addition, the PB series is fast. The 100 V/µs slew rate these boosters offer is matched or exceeded by only a few expensive power or high voltage op amps. If accuracy, in the form of low offset, drift, and/or bias current, is the system requirement, the PB series, with the proper choice of driver amplifier, can deliver high voltage performance with accuracy equal to the best small-signal op amps available on the market, and do it economically.

DESIGNING WITH BOOSTER AMPLIFIERS: BASIC CONNECTIONS

Power supply requirements for the PB50 dictate that the negative supply rail must be at least 30 Volts below the COMMON terminal (pin 5), setting the minimum supply voltage at +/-30 V. The PB58 can operate from supplies as low as +/-15 volts.

The INPUT terminal of the PB series devices is a low impedance input typically on the order of 50 KΩ. Maximum safe input voltage range must be limited to less than +/-15 volts. These power boosters will always have an offset of typically .75 volts as a result of the common base bipolar input stage. When used with a driver amplifier, this offset will subtract from the swing available from the driver. For example, a driver op amp that is required to swing 20 volts peak-to-peak will actually swing -10.75 and +9.25 volts. This offset has no effect on offset of the total driver and booster circuit since this offset is effectively reduced by the open loop gain of the driver amplifier. Remember that this offset will always be apparent when used without a driver amplifier.

The COMMON terminal provides a ground reference for the internal input and feedback circuitry. It might be noted that it is possible to use this "ground" terminal as an input; however, the PB series has not been characterized for such usage. The ground terminal would appear as a low impedance inverting input which must be driven from a low impedance source such as an op amp output.

The GAIN terminal allows the connection of additional resistance in series with the built-in feedback resistor of the PB series. The compensation capacitor connected to COMP, pin 8, is in parallel with the feedback resistor. Designers can predict the frequency response of the PB series amplifiers for any compensation by simply calculating the pole frequency of the parallel connection of feedback resistor, R_G, and compensation capacitor. The pole frequency is given by:

$$F_P = \frac{1}{2\pi(R_G+6.2K)C_C}$$

Where: R_G = EXTERNAL FEEDB ACK RESISTANCE
C_C = EXTERNAL COMPENSATION CAPACITOR

For example, a 22 pF compensation capacitor across the 6.2 K ohm feedback resistor results in a pole frequency of 1.2 MHz. This corresponds with the Closed Loop Small Signal Response graph on the PB50 data sheet. A gain of 10 will require placing a 22 K ohm resistor in series with the built-in 6.2 K ohm internal feedback for a total feedback resistance of approximately 28 K ohm. In this case a 22 pF compensation capacitor produces a rolloff at 260 kHz, again corresponding to the PB50 small signal response graph.

COMPOSITE AMPLIFIER STABILITY CONSIDERATIONS

The PB series data sheets provide 4 guidelines for insuring the stability of circuits designed with these boosters. Use of these guidelines can be complemented by the use of standard techniques such as plotting the overall gain response of the driver/booster combination and superimposing the feedback network response.

An example for determining the Aol (open loop gain) response of the composite amplifier is illustrated in Figure 1. At any given point on the frequency response, the overall gain is the sum of the gains (in dB) of the two amplifiers.

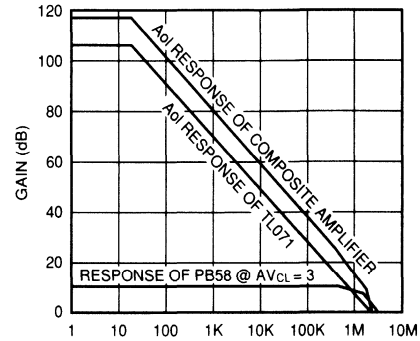


FIGURE 1. PLOTTING Aol FOR THE COMPOSITE AMPLIFIER

Figure 2 shows an example of such a plot for the deflection amplifier described in this application note. As a general rule, the intersection of the feedback response and open loop response should equate to a slope of no greater than 20 dB/decade to insure stability.

The particular deflection amplifier described in this application note is a testament to the ease with which the PB series devices can be designed into circuits where stability is usually a problem. The magnetic deflection circuit, which is a current source with an inductive load inside the feedback loop, is inherently unstable. The composite amplifier responded quite well to standard techniques used to stabilize deflection amplifiers (see AN #5, **"Precision Magnetic Deflection"**) and presented no special stability problems.

The designer who may be apprehensive about using a booster (buffer with gain) need have no reservations when using PB50 or PB58.

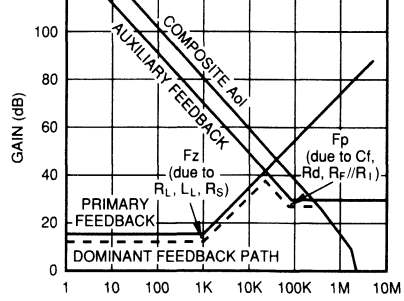
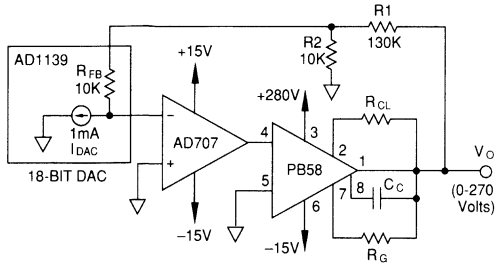


FIGURE 2. DEFLECTION AMPLIFIER FEEDBACK (I/β)

APPLICATION EXAMPLES: PROGRAMMABLE POWER SUPPLIES

The programmable power supply (PPS) application is useful to demonstrate the versatility of the PB series boosters. Along with the need to supply high voltages and currents, programmable power supplies often need high accuracy and low drift, while at other times they may need to be fast-responding. The PB series allows the

designer to optimize the circuit for these choices. Figure 3 is an example of a high accuracy PPS. An AD707 is selected as the driver amplifier to provide the extremely low offset required to obtain best possible performance from a high accuracy 18-bit DAC. The divider network on the output, R1 and R2, scale the output swing down to the full-scale range of the DAC. Accuracy will be affected by this divider, necessitating the use of high quality, low temperature coefficient (TC) resistors. If a packaged network can be used, then absolute TC is not nearly as important as TC ratio between R1 and R2. The use of this divider is preferable to the alternative technique of using an external DAC feedback resistor, since using the internal DAC feedback resistor insures the best possible temperature drift performance of the DAC itself. Most DAC's can exhibit up to 300 ppm/°C drift with external feedback resistors.



$$V_O = I_{DAC}\left\{\frac{R_{FB}\ R2 + R2\ R1 + R1\ R_{FB}}{R2}\right\} = I_{DAC}\ (270K)$$

FIGURE 3. HIGH ACCURACY PPS

APPLICATIONS AT LESS THAN FULL VOLTAGE AND CURRENT

The PB series do not have to be used at high voltages to realize all their performance benefits. Presently, only a few expensive IC power amplifiers can match these parts for slew rate and power bandwidth. Magnetic deflection applications require amplifiers with good speed performance at current levels often within those that the PB series can supply. While these applications don't always require high supply voltages, the high voltage capability of the PB series is useful when fast transitions are required with high inductance yokes, necessitating high supply voltages as a result of the yoke energy requirement:

$$V = L\frac{dI}{dt}$$

The basic techniques of magnetic deflection amplifier design are detailed in AN#5, **"Precision Magnetic Deflection."** Figure 4 is an example of these techniques put to use in the design of a magnetic deflection amplifier using the PB58. This circuit forces a yoke current proportional to input voltage by including the yoke within a current sensing feedback loop. In this example, the feedback resistors R_F and R_I are configured for a minimum gain of 5 to compensate for the added booster gain, thereby easing stability considerations. The auxiliary feedback network Cf and Rd act to bypass the 90° phase shift of the yoke/sense resistor feedback at higher frequencies ensuring stability with best transition times. The fastest transition time in any magnetic deflection amplifier is determined by the available voltage swing and yoke inductance. In the circuit of Figure 4, nearly 140 volts could be made available for the 200 microhenry yoke, resulting in a minimum possible transition time of 2 microseconds. The TL071 and PB58 combination can slew at 40 V/microsecond which means the amplifier requires an additional 4 microseconds to provide full voltage swing. The end result is a circuit that can deliver total transition times of less than 6 microseconds, equating to sweep speeds of 83 kHz.

An important advantage of a separate booster amplifier in deflection applications is the ability to swing the output stage supply rails to improve efficiency. Slower sweep speeds can use lower power supply voltages than higher speeds. In addition, during a high speed sweep the high voltage is only needed for a short period of time until yoke current builds and can then be switched to a lower value. Using the lower supply voltages whenever possible improves efficiency and reduces dissipation. In applications where the supply rails will be **"flexed"** in this manner, only the rails connected to the power booster need to be flexed. The constant supply available at the driver

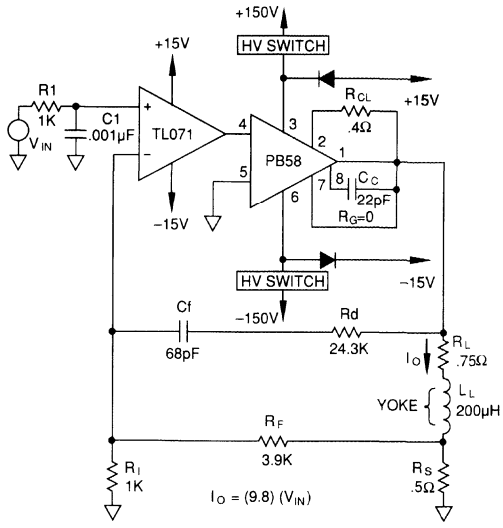


FIGURE 4. ELECTROMAGNETIC DEFLECTION AMPLIFIER

amplifier enhances the driver amplifier's ability to maintain overall loop control by preventing the coupling of supply switching transients into the input section of the amplifier.

Figure 4 provides a general idea of the circuitry involved in switching the supply rails. The actual implementation could take on many forms that are beyond the scope of this application note.

A final performance consideration in magnetic deflection amplifiers is avoidance of slew rate overload (or any condition which could result in input overload). This problem actually occurs during the rapid retrace transition, but shows up during the trace interval. The evidence of input overload is ringing during the trace interval. To eliminate this problem, reduce the transition time of the retrace portion of the input waveform to a rate which is within the slew rate specification of the amplifier. Slower transition times do not necessarily reduce circuit performance since the amplifier was overloaded to begin with, and eliminating ringing is actually an improvement on settling time when returning to the trace interval. Controlling input slew rate can be accomplished in many ways. If the actual risetime of the input signal itself cannot be controlled, a simple lowpass R-C filter at the input of the amplifier will suffice. In the example shown in Figure 4., R1 and C1 provide a filter which limits the slew rate of any input signal rise time to within the amplifier's slew rate.

Selection of the correct filter time constant takes into account both amplifier slew rate and gain of the circuit. In the case of a magnetic deflection amplifier, the appropriate value for gain would be the effective gain of the alternate feedback path Cf and Rd.

$$t = \frac{V_{IN}\ Av}{SR}$$

Where: V_{IN} = PEAK TO PEAK INPUT VOLTAGE
Av = COMPOSITE AMPLIFIER CLOSED LOOP GAIN
SR = RATED SLEW RATE OF THE AMPLIFIER

BOOSTER WITH NO DRIVER

It is entirely possible to use power boosters without an external driver. This could be done for simplicity or economy. It also provides the best slew rate and bandwidth performance possible with the PB series. All of this is made possible due to the boosters' self-contained internal feedback loop.

When used without a driver, the PB50 will have an inherent offset of typically 750 millivolts. Harmonic distortion remains under 0.5% at up to 30 kHz. Input impedance will be 25 K ohms minimum. Power bandwidth will typically be the full 320 kHz at the 100 Volts P-P output the PB50 is capable of.

The ground terminal on pin 5 of the PB50 presents possibilities as an additional input. Some improvement in bandwidth would be noted if this terminal were used as an input with the actual input terminal grounded. This forces the input transistor into a cascode connection. It is possible to utilize the booster as if it had true op amp type inverting and non-inverting inputs.

INTRODUCTION

The WB05 is capable of solving a wide range of problems in achieving both high current and wide bandwidth. This capability is delivered through hybrid design and construction methods. The advantages include low stray capacitances, low stray inductances and good thermal coupling. The WB05 (Wideband Buffer) was optimized for use with an external high speed driver amplifier.

VOLTAGE GAIN CONFIGURATION

Figure 1 illustrates a typical configuration using the WB05 to buffer the output of a conventional driver amplifier which supplies voltage gain.

In this configuration, R_F and R_I should be kept as low as possible and consistent with input impedance and gain requirements. Using low value resistors prevents high impedance nodes from acting as antennas. These nodes could cause output signals to be picked up as positive feedback and result in oscillations. Low values also keep input and stray capacitance time constants low for high speed and improved settling time. C_F is used to optimize settling time by compensating for input and stray capacitances. R_D reduces settling time and helps minimize overshoot. R_D loads the output of the driver amplifier which reduces its output impedance. R_D is typically in the 500 ohm range. The driver op amp must be capable of supplying adequate phase margin for itself and the WB05 at the closed loop gain used.

The driver amplifier also must be capable of providing enough current to drive R_D, as well as charge the WB05's input and any other stray capacitances, at the intended slew rate. The phase shift introduced by the WB05 will increase the minimum required gain of the driver amplifier to guarantee stability. If the driver amplifier is a transimpedance amplifier, the inverting configuration shown in Figure 1 will typically exhibit better slew rate and rise time than a noninverting configuration. This is due to the nature of the front end of most transimpedance amplifiers and the current available for turning on the output stage in the two different gain configurations.

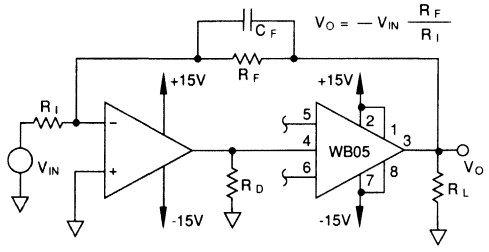


FIGURE 1. VOLTAGE GAIN CONFIGURATION

VOLTAGE TO CURRENT CONVERSION

For applications where the current through the load must be controlled (V to I Conversion) Figures 2, 3 and 4 illustrate some options depending upon the type of driver amplifier used.

The configuration in Figure 2 is optimized for driver amplifiers that are conventional op amps as opposed to transimpedance op amps. R_S should be as large as possible consistent with voltage drop, power dissipation, and efficiency requirements. The sum of R_F and R_I appear in parallel with R_S and contribute some error. R_F and R_I force the driver amplifier to run in a higher closed loop gain since its feedback is being reduced. Recall that closed loop gain = 1/feedback ratio. The advantage of higher closed loop gain is increased phase margin for stability. C_F provides a means for optimizing settling time and R_D reduces overshoot and contributes also to improved settling times.

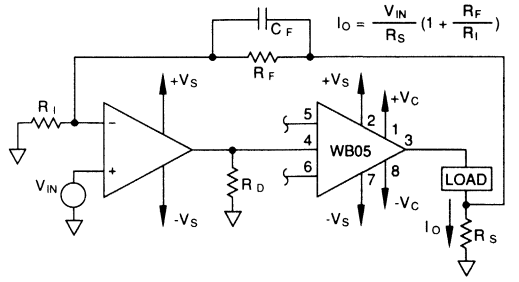


FIGURE 2. V to I CONVERSION WITH CONVENTIONAL OP AMP DRIVER

Figure 3 illustrates optimal configuration for transimpedance driver op amps. If the driver op amp has an internal, uncommitted feedback resistor (R_{FI}), it should be connected to R_S as shown. In addition, R_{FE} (lower value than R_{FI}) is added in parallel with R_{FI} to increase bandwidth and reduce settling time.

The value of R_S should be as large as practical to increase signal to noise ratio. The values of R_{FE} and R_I should be as low as possible consistent with gain, efficiency and input impedance requirements. C_F and R_D are used to improve settling time and overshoot. In some cases there will be a compromise between desired transconductance and stability using this configuration.

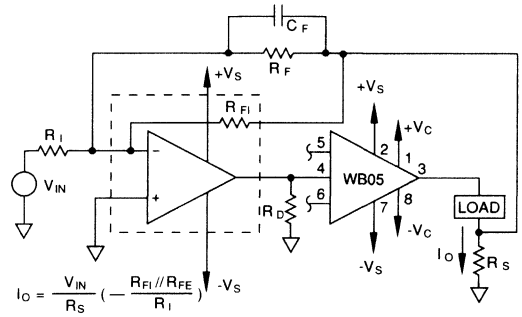


FIGURE 3. V to I CONVERSION WITH TRANSIMPEDANCE DRIVER

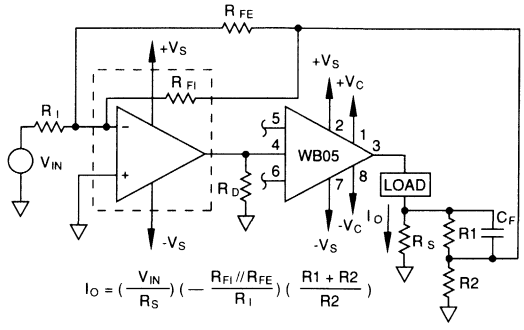


FIGURE 4. V TO I CONVERSION USING TRANSIMPEDANCE DRIVER; IMPROVED PHASE MARGIN CONFIGURATION

Figure 4 shows a configuration for V to I conversion with a transimpedance driver that can be made tolerant of phase shift problems as they relate to stability. The price paid is a greater error in output current due to tolerances of R1 and R2 and the additional feedback division they provide. This reduced feedback forces the driver amplifier to run in higher gain which increases phase margin for stability. Once again the compromise made is reduction of bandwidth. When calculating transconductance, R1 and R2 must be included.

MINIMIZING POWER DISSIPATION

The power dissipation in the WB05 can be reduced in some cases by running the output stage at reduced voltages. Figure 5 shows an application that uses this approach. Operating the transimpedance drive amplifier and the WB05 front end at ±15V results in maximum bandwidth for both, while operating the WB05 output stage at ±8V lowers power dissipation in the WB05. The value of the reduced output supplies will be a compromise between reduced power dissipation and voltage drop margin. As this margin changes slightly with temperature, it is best to compromise in the power dissipation direction.

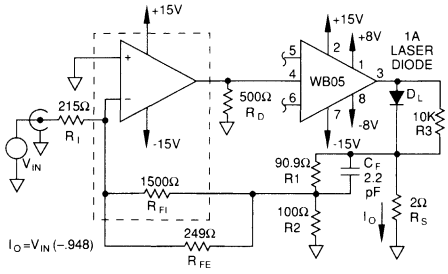


FIGURE 5. LASER DIODE DRIVER WITH BUFFER DISSIPATION

WIDE BANDWIDTH APPLICATIONS

In applications requiring maximum bandwidth, there is no choice but to use the WB05 without a driver amplifier. The circuit shown in Figure 6 maintains a constant bias current of 200mA through the laser diode D_L, while supplying a sinewave modulation of 100mA peak to peak at a frequency of 250MHz. The input pad reduces input VSWR. A1 provides the bias current set point, nulls the effects of the WB05's V_{OS} and $T_C V_{OS}$, and compensates for temperature effects in D_L.

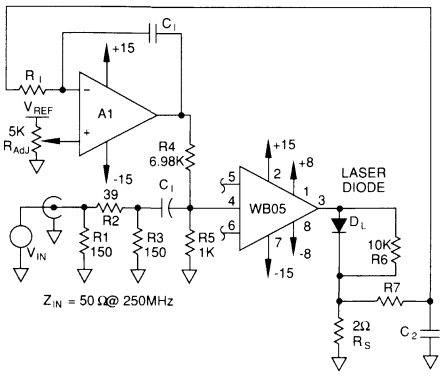


FIGURE 6. WIDE BANDWIDTH LASER DIODE DRIVER

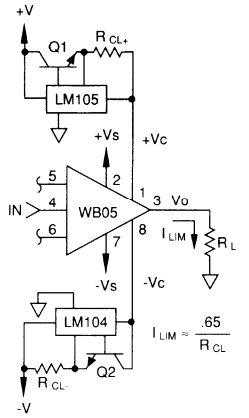


FIGURE 7. OUTPUT VOLTAGE REGULATION AND CURRENT LIMIT

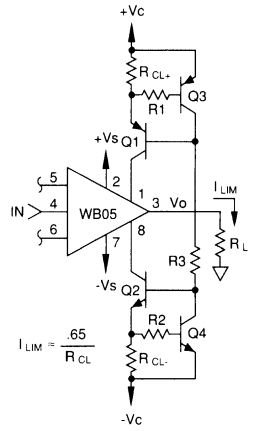


FIGURE 8. CURRENT LIMIT: FAST RESPONSE TIME

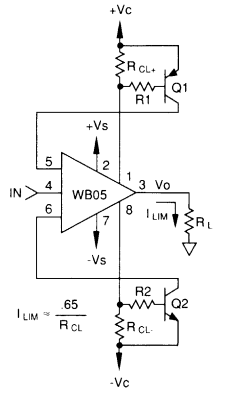


FIGURE 9. CURRENT LIMIT USING SLEEP PINS

CURRENT LIMITING THE WB05

The WB05 does not have internal current limiting. Four methods for external current limiting are presented here.

The first current limiting method is presented in Figure 7. This approach is not very fast but can be used to advantage if the WB05 output stage is run at reduced voltages compared to its input stage or other available supplies. The LM104 and LM105 are operated with external pass transistors to provide adequate current drive. The values of R_{CL+} and R_{CL-} are used to set the current limit value and may be scaled asymmetrical if so desired.

The second method for current limiting is presented in Figure 8. This has the fastest practical response time, but a penalty is paid in waste base current through Q1 and Q2. In this case it is important that Q1 and Q2 have good beta at the current limiting value. Darlingtons should not be used if fast response time is desired. R_{CL+} and R_{CL-} are used to provide approximately .65V drive to Q3 and Q4 when the desired current is reached in the respective WB05 positive and negative output stage. R1 and R2 are used to limit base current in Q3 and Q4 and should be no larger than required. R3 is used to guarantee enough base current in Q1 and Q2 to provide collector currents as high as the desired current limit value. Storage time of Q1 and Q2 limit the response time, but it can be made short enough to prevent damage to the WB05 and also to most loads.

The third current limiting method is shown in Figure 9. This approach takes advantage of the WB05 sleep pins. The response time of this method is approximately 10 microseconds – quick enough to protect the WB05 under most circumstances. Some loads may not be able to withstand overcurrent for this long. Q1 and Q2 put the upper and lower halves, respectively, of the WB05 to SLEEP (output goes to high impedance). R_{CL+} and R_{CL-} are sized for the V_{BE} of Q1 and Q2 at the desired value of current limit. Approximately 2 mA of collector current will have to be provided by Q1 and Q2 during sleep mode activation. R1 and R2 limit base drive current in Q1 and Q2.

The fourth and final current limiting technique is shown in Figure 10. Worst case fault currents through the output stage of the WB05 are limited by some internal resistance. The WB05 output stage can be modeled as in Figure 10. The maximum fault current that will flow with a short to Vfault is then given by:

$$Isc = (V_C - Vfault) / (Rfault + 0.6 + R_{CL})$$

R_{CL+} and R_{CL-} are normally zero ohms. In some applications it is practical to assign values to R_{CL+} and R_{CL-} that substantially lower fault currents without affecting drive capability. In those cases, electronic, active current limiting schemes may be replaced by this simple method.

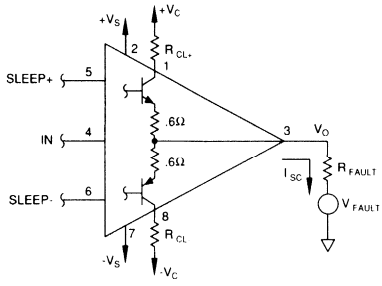


FIGURE 10. SIMPLE RESISTIVE CURRENT LIMITING

POWER SUPPLY BYPASSING

Proper power supply bypassing to prevent undesired, destructive oscillations is a must when using the WB05 because of its large small signal bandwidth, high voltage slew rate and high current slew rate. If the front end supplies are tied to the output stage supplies, bypassing should be done per Figure 11. C1 and C1' are ceramic capacitors of 330 to 1000 picofarads; C2 and C2' are ceramic capacitors of .01 to .033 microfarad; and C3 and C3' are low ESR, tantalum electrolytic capacitors of 2.2 to 6.8 microfarads.

If separate front end and output stage supplies are used, bypassing should be done per Figure 12. C4 and C4' are ceramic capacitors of 330 to 1000 picofarads. C1, C1', C2, C2', C3, and C3' are the same as those used in Figure 11. All capacitors, especially C1, C1', C4, and C4', must be as close to the buffer power supply pins as possible with short leads (1/8" to 1/4") and / or short, wide PCB traces to minimize stray inductances.

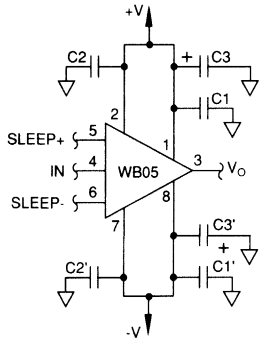


FIGURE 11. BYPASSING WITH V_C EQUAL TO V_S

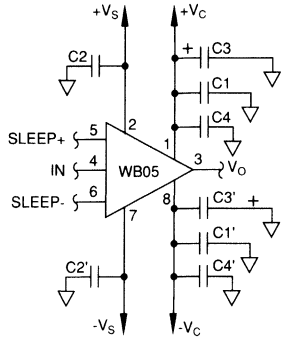


FIGURE 12. BYPASSING WITH V_C NOT EQUAL TO V_S

HIGH Z_L AND/OR C_L

The WB05 has been optimized for high current/low impedance loads. With large load impedances or high capacitive loading, the part may show peaking in the small signal response. If required, a series R-C network with 22 ohms and 68pF can be connected from the output to ground to flatten the response. Refer to Figure 13.

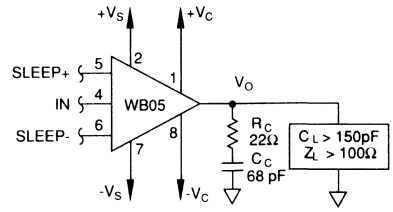


FIGURE 13: COMPENSTATION FOR HIGH Z_L AND/OR C_L

NEW MOSFET POWER OP AMPS EASE SAFE OPERATING AREA LIMITATIONS

Hybrid power op amps continue to provide higher levels of performance and power handling than their monolithic counterparts. Power MOSFET's promise to continue the dominance of the hybrid power op amp in terms of power delivery and Safe Operating Area (SOA).

Protection issues must not be neglected regardless of amplifier choice, but the compromises required to protect the amplifier are eased with MOSFET designs. Protection of an amplifier is a matter of keeping it within its SOA under all expected conditions including faults such as short circuits.

An example of a common mistake in selecting an amplifier for a motor drive application is to use a 5A rated amplifier to drive a 1A motor. Specifying an amplifier for a motor drive application is not that simple, and stall or reversal conditions could overstress the amplifier.

Here is an illustration using a motor with the following specifications:

Winding resistance: 1.24 ohms
Voltage constant: 7.41V/K RPM
Torque constant: 10oz/in/A

The actual running current depends on the required torque. Of most concern is the worst-case current requirements that occur under stall and acceleration conditions. Under stall conditions, the amplifier is presented with a load equal to the winding resistance of the motor. This condition must be within the SOA of the amplifier.

The motor's speed determines the applied voltage. If there are sudden reversals, the motor back EMF could theoretically reach a value equal to the full applied voltage or equal to the amplifiers supply rails. This would be equivalent to shorting the amplifier output to one of its supply rails with only the motor winding resistance in series.

While the MOSFET power op amps are often featured for their high speeds, motor drive applications can take advantage of the MOSFET SOA that is free from second breakdown. Second breakdown is a limitation of all bipolar output power op amps. Second breakdown severely limits an op amp's current capacity under conditions of high voltage stress. The MOSFET on the other hand is strictly limited by its power dissipation, or thermal limits. Figure 1compares the 25°C SOA of the PA04 MOSFET amplifier with the bipolar PA03. While the PA03 is rated for higher currents and dissipation, the PA04 has greater current capacity when there is more than 110V stress on the output devices.

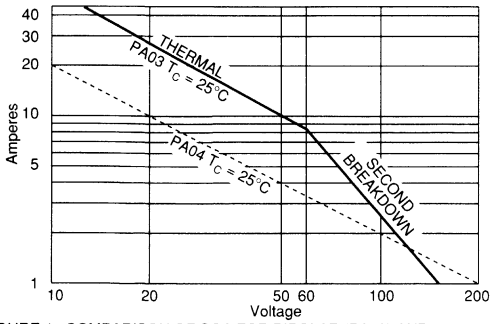


FIGURE 1. COMPARISON OF SOA FOR BIPOLAR (PA03) AND POWER MOSFET (PA04) POWER OP AMPS

For 25°C SOA calculations with a MOSFET amplifier an SOA graph is not even necessary. As long as the product of voltage and current stress is within the power dissipation rating, the amplifier is safe. MOSFET's, to reiterate, are strictly power limited.

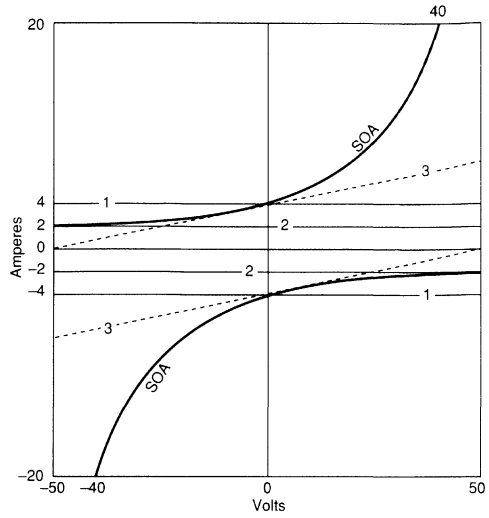


FIGURE 2. PLOT OF OUTPUT VOLTAGE AND CURRENT WITH SOA SUPERIMPOSED

Proper selection of current limit will determine if an amplifier is safe under fault conditions. One way of viewing this limitation is to draw a graph of output voltage and current, and superimpose SOA limits as shown in Figure 2. This graph (PA04 and ±50V supplies shown) illustrates how greater currents are available when the output voltage swings closest to the rail supplying the current. The tradeoff occurs when setting current limits, usually for either of two fault conditions: shorts to ground or shorts to either supply rail. A stalled motor is equivalent to a short to ground through the motor winding resistance, while a reversal could assume the stresses of a short to either rail.

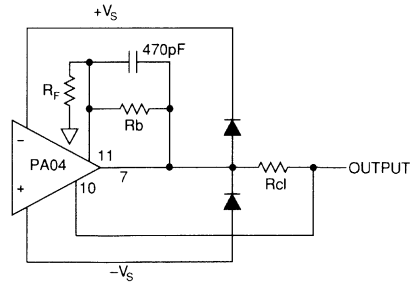


FIGURE 3. FOLDOVER CURRENT LIMITING CIRCUIT

From Figure 2, line 1, a limit safe for shorts to ground would be 4A (4A*50V=200W). This is well below the amplifier's full 20A capability. Even more stringent is the current limit for a short to either rail of 2A indicated by line 2 of Figure 2. A 2A limit, combined with external flyback diodes, would result in an amplifier tolerant of virtually any short or voltage kickback stress on its output. Keep in mind that this brief example uses as its basis, the 25°C SOA limits. In reality, internal dissipation and heatsinking limitations elevate temperatures, further reducing safe current levels.

FOLDOVER CURRENT LIMITING

The PA04 features four-wire current limit to overcome sensing errors occurring when working with such low resistances. While this four-wire current limit is useful in improving accuracy of current limit, it also facilitates implementing foldover current limiting. This limiting is known as load line limiting.

Foldover current limit allows more amplifier current as the output swings closer to the rail supplying the current shown by line 3 in Figure 2. Figure 3 shows the circuit to implement foldover current limiting. Rb and Rf configure a voltage divider that reduces the signal to the current limit transistors as the output swings closer to the current-supplying rail. Rf determines the slope of the foldover function. The value selected for Rb corresponds to the similar resistor internal to PA12 (actually 280 ohms) so that equations and methods developed for use with PA12 foldover limiting would be easily applied to PA04 external foldover limiting. The capacitor across Rb prevents stability problems while in current limit.

The foldover slope must not be too steep, or latching may occur. This sets a limit to the value of Rf equal to $V_S/.0025$ which results in a foldover characteristic where current available when the voltage output has swung fully to the rail opposite to the one supplying current is zero. The current available when the output is closest to the rail supplying current is twice that available when the output is at zero volts. When using PA12 equations, substitute this value of Rf, in Kohms.

A PA04 incorporating foldover limiting at ±50V and requiring safety for a short to ground, would have R_{CL} selected for a 4A limit (this presumes the amplifier case can be maintained at 25°C for the duration of the short, otherwise it would have to be reduced further to stay within temperature limitations). The foldover limiting would then allow 8A at full output swing, or near zero current when delivering current from the rail opposite the output voltage polarity. A bipolar amplifier such as PA12 would be limited to 3.2A under the same criteria. The most powerful monolithic would be limited to 300mA because it is configured only for simple single resistor current limiting.

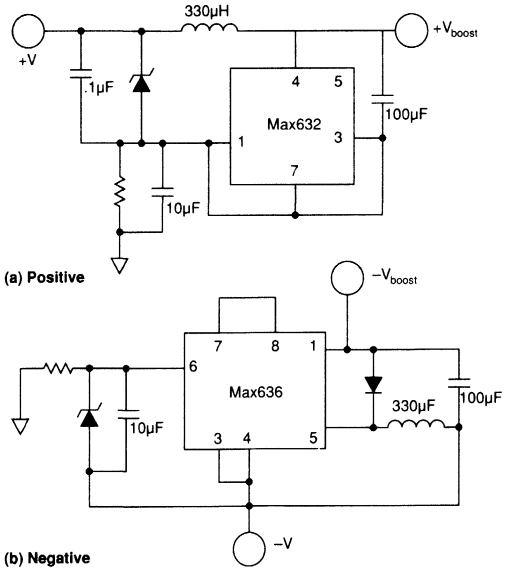


FIGURE 4. VOLTAGE BOOST CIRCUITS

SATURATION VOLTAGE AND BOOST PINS

In motor drive applications at lower voltages, the saturation voltage, described on the data sheet as *voltage swing*, the PA04 could result in considerable power dissipation. At 15A, the PA04 output can only swing to within 8.8 volts of the rail resulting in 132W of dissipation. Boost pins are provided on the PA04 to power the front-end of the amplifier on voltages higher than the output stage, thus improving saturation. Using these terminals reduces the swing-to-rail to 5.3V at 20A for 106W dissipation. At 15A it is 4.7V for 60.5W dissipation.

Several methods can be used to supply the higher voltage required by the front-end. Additional power transformers, or additional taps on existing power transformers, or additional regulated supplies are obvious options. Modern voltage converter IC's make it inexpensive to develop these voltages under almost any condition. In Figure 4, zener regulated voltages are referred to each rail and provide power to Maxim voltage converter IC's to develop the boost potentials.

MOSFET ADVANTAGES AT HIGHER VOLTAGES

The PA04 is rated at ±100V or 200V rail-to-rail. This is twice the rating of any bipolar hybrid power op amp other than PA03, and 2.5 times the rating of any monolithic power op amp.

MOSFET's have made possible this increase in voltage ratings and this can be useful in motor drive applications at high voltages. Surprisingly, some DC motors require voltages around 100 volts. The PB50 power booster is a low-cost hybrid *buffer with gain* that gives the same ±100 volt capability of PA04 with a maximum current of 2A. Because the PB50 is a MOSFET device, it can still provide 200mA at a full 200V stress.

An upgrade to the PB50 is the PB58 providing voltage capability up to ±150 volts. While PB58 is rated 1.5A, the premium PB58A is specified up to 2A. A key advantage of PB58, especially for motor drives, is its 87W dissipation. Operated at ±100V, the PB58 can provide 435mA with complete safety. At ±50V, PB58 can deliver up to 870mA. This is well over twice what could be tolerated from an amplifier such as the PA12 under the same conditions, much less from monolithic power op amps.

Both PB50 and PB58 are power booster amplifiers, not stand alone op amps. Refer to PB50 and PB58 data sheets for typical examples of actual composite amplifier circuits. Several alternatives are given. They range from low speed, high accuracy circuits, to high speed circuits.

ADVANCED AMPLIFIER PROTECTION

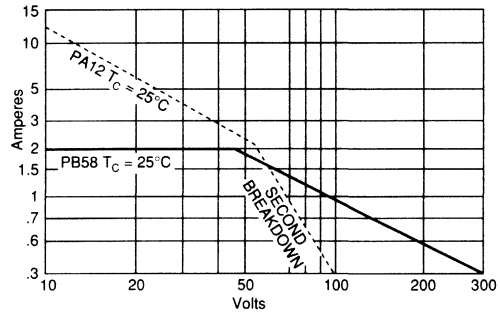


FIGURE 5. COMPARISON OF SOA FOR PA12 AND PB58

The PA04's adaptability to foldover current limiting is important but not the last word in protection. Prior efforts at SOA protection have been based on bipolar transistor designs sensing output transistor temperature combined with current limiting. These techniques have shortcomings when overstress occurs while operating in the second breakdown region of bipolar power devices. The isolated hot spot occurring during second breakdown can escape sensing by the temperature sensor.

For example, PA03 senses power transistor temperature to provide a high degree of protection. But at total rail-to-rail voltages in excess of 60V (±30V), second breakdown still makes the amplifier prone to failure in extreme stresses.

In a MOSFET power output device, if a local hot spot occurs, the local transconductance decreases along with an increase in Rds at the hot spot. This facilitates thermal spreading rather than concentrating heat. As a result thermal sensing should prove extremely effective with power MOSFET's. Apex is developing such amplifiers and early testing has shown that this may be the key to ultimate amplifier protection.

WIDEBAND, LOW DISTORTION TECHNIQUES FOR MOSFET POWER AMPS

Shake table systems, function generators and acoustic instruments all have requirements similar to quality audio amplifiers: wide bandwidths along with low distortion. In the past, industrial grade power op amps have traded off bandwidth to insure unity gain stability, and the bipolar designs have not always met the linearity requirements of demanding applications. The PA04 changes all this with a MOSFET based architecture that sets new standards for bandwidth and linearity of integrated circuit power amplifiers.

The development of the PA04 was driven by sonar application requirements for a highly linear, high power amplifier with a power bandwidth in excess of 100 kHz. MOSFET's are the optimum choice power device to provide this performance, and in the PA04 Apex goes several steps further in using MOSFET's in all active gain stages. While this application note will focus on getting best bandwidth and linearity from the PA04, the techniques described apply to any power op amp.

Op amps depend on negative feedback to improve performance in all ways including accuracy, linearity and bandwidth. The ideal condition is to use feedback around a design which has inherently good open loop characteristics. Evaluation of prospective amplifiers under open loop conditions quickly reveals linearity and bandwidth deficiencies. Even a simple distortion measurement under open loop conditions will give rapid comparative evaluation. Alternatively, an X-Y comparison using an oscilloscope and the circuit of Figure1, which multiplies summing node error by 100, will give a visual display of amplifier linearity. The circuit of Figure 1 will reveal that PA04 has an inherently linear characteristic while even the best bipolar designs such as PA07 have quite a bit of curvature in their open loop linearity. This is traceable to the better inherent linearity of MOSFET devices in comparison to bipolar transistors.

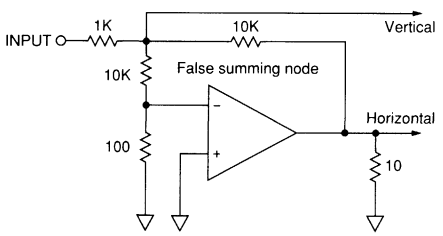


FIGURE 1. SIMPLE TEST CIRCUIT

CIRCUIT CONSIDERATIONS

The design considerations desirable for wideband, low distortion designs can be summed up with four guidelines:

1. Lowest possible closed loop gain.
2. Inverting configuration.
3. External phase compensation.
4. Input slew-rate limiting.

Distortion reduction in an op amp circuit is proportional to the amount of feedback, and this corresponds to lower gain circuits having reduced distortion. Distortion reduction is described mathematically as:

$$Df = D\left(\frac{Af}{A}\right)$$

Where: Df = % DISTORTION WITH FEEDBACK
D = % DISTORTION OPEN LOOP
A = OPEN LOOP GAIN
Af = CLOSED LOOP GAIN

It is obvious that open loop distortion is an important criteria in amplifier selection. A high open loop gain is also desirable, but op amps with high open loop gains most often have a severe tradeoff in gain-bandwidth.

The minimum useful closed loop gain is determined by the amplitude of the drive signal available to the power op amp circuit. Most often this drive is likely to come from a small signal op amp with the customary ±10 V peak drive capability. If for example a PA04 power op amp is being designed which operates at the full ±100 V supply rail limit of the PA04, this will require a minimum gain of 10.

In the event the drive signal is not a full ±10V peak, a tradeoff must be made as to whether the power op amp should be operated at a higher gain, or an additional small signal op amp be included for additional gain. Consider that the additional small signal op amp will result in insignificant contributions to distortion as long as its gain is low (<30). The light loading of the power amp circuit further minimizes distortion from the small signal op amp. These considerations favor this multiple op amp approach with a lower gain power op amp compared to a single high gain power op amp.

Low closed loop gain in the power op amp equates to increased amounts of negative feedback. This condition occasionally meets with unfounded objections when the requirement is low distortion, especially under transient conditions. However, this is dealt with by slew rate limiting to be discussed later.

The inverting amplifier configuration forces common mode potentials to zero. By doing so, non-linearities due to common-mode effects are also reduced to zero. The main advantage a non-inverting configuration would have is greater freedom of design regarding input impedance of the power op amp circuit along with the obvious lack of inversion.

Although the inverting configuration reduces input impedance, the two amplifier approach insures that the power amp circuit is driven by a source adequate to handle the resultant impedance. The cascade of two inverting amplifiers yields a non-inverting circuit. A further possible useful feature of the inverting power amp circuit is that the summing node can be monitored and any voltage detected used to indicate fault or non-linear conditions.

EXTERNAL PHASE COMPENSATION

Many power op amps are internally compensated for unity gain stability. However, this trades off gain-bandwidth product for stability under all operating conditions. Since distortion reduction is proportional to the ratio of open loop to closed loop gain, it is desirable to have as high as possible open-loop gain at high frequencies. Since it is unlikely that the power op amp will be configured for unity gain, the external phase compensation allows for a reduced compensation, yielding improved distortion and slew performance.

The small signal response curve for PA04 shown in Figure 2 helps to illustrate the comparative advantage of external phase compensation. The straight line at 20dB represents a gain of 10 amplifier which if the PA04 were compensated for unity gain would provide a 200 kHz rolloff. Decompensation for a gain of 10 results in a 700 kHz rolloff. In addition, note that loop gain for the unity-gain compensation is only 22 dB at 20 kHz, while it is 30 dB for the gain of 10 compensation. This increase in loop gain results in 2.5 times less distortion at 20 kHz.

The large amount of feedback at low gains obviously reduces distortion. Problems can occur however under transient conditions. If a step function is applied to the input of the amplifier circuit, the output can only change as fast as the amplifier slew rate allows. During this slew interval the input summing node will develop a large differential voltage. This nonlinear condition and input overload can cause a host of difficulties including a slow and poorly behaved recovery from this overload.

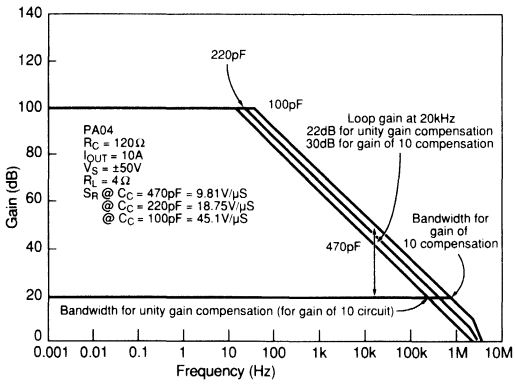


FIGURE 2. THE SMALL SIGNAL RESPONSE FOR THE PA04

Restriction of the input slew rate can avoid these transient distortion problems. The input should never be allowed to slew faster than the amplifier output can follow. If the actual slew rate of the source cannot be predicted or controlled, then simple low pass filtering at the amplifier input will prevent transient distortion.

The filter time constant is a function of amplifier slew rate. The maximum acceptable rate-of-change on the input signal is limited to a value less than the amplifier slew rate divided by the amplifier gain. With a known maximum step function input, the maximum rate-of-change at the low pass filters output occurs at t=0 and is determined by:

$$dv/dt = (V/R)/C$$

The RC time constant trc required at the amplifier input is:

$$trc = (V_{IN}A_V)/S_R$$

Where: V_{IN} = PEAK-TO-PEAK INPUT VOLTAGE
A_V = CLOSED LOOP GAIN
S_R = SPECIFIED AMPLIFIER SLEW RATE

Note that there is some reduction in bandwidth with this filter. However, with the PA04 this still permits a 40 kHz bandwidth. This limitation again favors the use of the fastest possible power amplifiers. Keep in mind that transient behavior is actually enhanced by the addition of the input filter.

STABILITY CONSIDERATIONS

When a power amplifier drives a capacitive load, the interaction between output resistance and capacitive load creates an additional pole and attendant phase shift in amplifier response (Figure 3). Inductive loads can result in stability problems due to rising impedances at high frequencies. Most follower type output stages are immune to the effects of inductive loads, but collector output, drain output and quasi-complementary output stages with local feedback loops are susceptible to parasitic oscillations driving inductive loads.

Figure 4 shows several measures are available to improve stability, each with some advantage and disadvantage: (a.) Capacitor across feedback resistor. This provides a compensating phase lead in the feedback path to counteract the effects of additional poles. This technique generally requires a unity-gain stable amplifier. (b.) Parallel inductor-resistor combination in series with amplifier output. Feedback

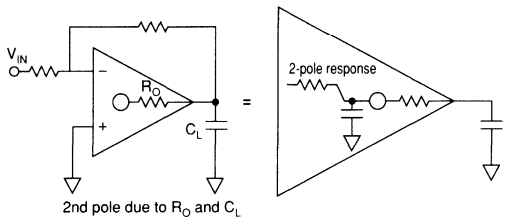


FIGURE 3. CAPACITIVE OP AMP LOADS

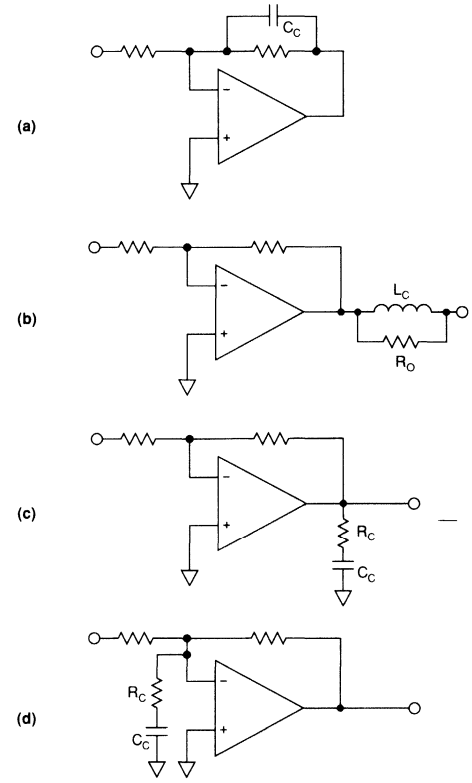


FIGURE 4. STABILITY ENHANCING TECHNIQUES

must be taken directly at output of amplifier so that inductor-resistor has the effect of isolating the amplifier and feedback network from the capacitive load. (c.) Series resistor and capacitor from amplifier output to ground, often referred to as a *snubber*. Used only in situations where amplifiers are sensitive to inductive loads. Insures a low, resistive load impedance at high frequencies. (d.) Series R-C network across op amp inputs, often referred to as *noise-gain compensation*. Simply described, this technique reduces feedback at high frequencies to the point where stability is not a problem.

Methods a and b offer the best overall bandwidth performance and transient behavior. Method a has been mentioned already as having the tradeoff of requiring a unity gain stable amplifier. However, with proper attention to design, it is possible to incorporate method a with any amplifier to help control overshoot and ringing behavior.

Method d, the noise gain compensation, will have the effect of reducing the closed loop bandwidth of the resultant circuit to the same effective closed loop bandwidth corresponding to the noise gain. To illustrate, consider a gain of 10 amplifier with a network across the inputs configured for a high frequency noise gain of 100. If the gain of 10 amplifier had an uncompensated bandwidth of 100 kHz, with the noise gain compensation, the bandwidth would be reduced to 10 kHz. In addition, the response curve peaks near the high frequency limit resulting in overshoots in the square wave response.

All amplifiers vary in their ability to tolerate capacitive loading before stability problems occur. PA04 is especially good in this regard tolerating well over 1 uF while operating at a gain of 10. In the case of PA04, no additional stability enhancement measures are required and this is the ideal case for best frequency response.

TYPICAL DESIGN EXAMPLE

A design utilizing all of the guidelines described here would be constructed around a PA04 in an inverting gain of 10 configuration as shown in Figure 5. For additional gain the PA04 is preceded by a small signal op amp also operating at an inverting gain of 10. Many choices

are available for this op amp such as the 5534 or OP37. The PA04's tolerance of reactive loads negates the need for additional stability enhancement components.

With an 8 ohm load this circuit can supply over 300W at up to 150 kHz with the input slew rate filter bypassed. With the filter in place, gain begins to rolloff at 40kHz, although full output swing is available up to 150kHz. Distortion never exceeds 0.02% THD. Power supplies will need to be capable of at least 7A to support 8 ohm loads in ac coupled applications. Regulated supplies aren't necessary but are desirable from a reliability standpoint.

When designing for low distortion with PA04, the impedance of the feedback and input networks around the op amp should be kept as low as possible. The input MOSFET's of the PA04 cause it to have a large input capacitance which is nonlinear with variations in input signal. Excessive impedances will increase distortion due to these higher order capacitance effects. The 2K ohm input resistor of Figure 5 is high enough to avoid excessive loading of the small signal op amp and low enough to avoid distortion effects with the PA04.

Several basic practices are important to implement when using PA04. Power supply bypassing consisting of good high frequency capacitors, generally ceramic, must be connected from each supply rail to ground. Unless these capacitors are physically close to the amplifier, parasitic oscillations may occur. Even an inch away from the socket pins is too far. Be sure to read and observe all ESD precautions on the PA04 data sheet, and those shipped with PA04.

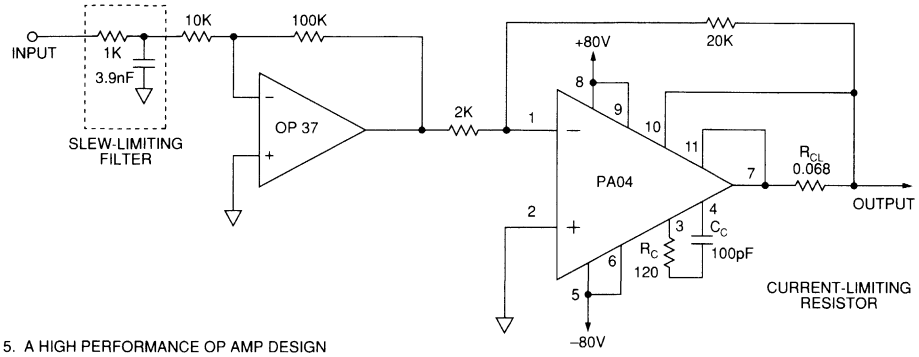


FIGURE 5. A HIGH PERFORMANCE OP AMP DESIGN

INTRODUCTION

The DB2800 series of DC/DC converters represent the state of the art in power supply performance, features and reliability. While most designers will find this series extremely simple and flexible to apply, with performance that either meets or exceeds system requirements, sometimes one or more of the converter performance specifications must be enhanced. For example, for a low noise application, the designer might wish to reduce output ripple voltage or input ripple current.

Specifying a heatsink when the converter is to be operated in an extremely hot environment is another example of a performance improvement. When the converter is to be remotely controlled, the shutdown feature might be employed. All of these examples are covered subjects in this application note.

SHUTDOWN FEATURE

One feature of the DB2800 series is the ability of the converter to be remotely shutdown. The designer may choose to use this feature for a variety of reasons, namely if a fault is detected in the load or for power savings during no load times.

The voltage on pin number three, referred to pin number twelve, is used to activate this feature. The various modes of operation attainable by driving this pin are detailed in Table 1.

When in shutdown, the DB2800 will draw approximately 50mA of input current and the output will go to a high impedance state. The dynamic performance of the converter, as it is taken in and out of shutdown, is shown in the appropriate data sheet. The shutdown pin must always be driven with at least 10k of resistance as seen from pin #3 to pin #12.

The shutdown pin will always have an additional signal present on it when the converter is running. The typical input schematic of this pin is shown in Figure 1. Typical values of the signal are shown in Table 2.

This signal is the power stage current analog voltage of the converter. A sample of this voltage is mixed with a ramp to derive a control voltage for line and load variations. Unfortunately this voltage is a potential source of emi and rfi emissions if not treated correctly.

In order to reduce this possibility, the driving voltage for shutdown should be buffered if it is a long way from the DB2800. If the shutdown feature is not used, a small value capacitor < 220pF should be used to terminate the pin to the case. The minimum value necessary for the emi/rfi problem should be used as higher values tend to limit internal current limit performance. A schematic showing a possible application using the shutdown feature is shown in Figure 2.

TABLE 1.

($V_{PIN\#3} - V_{PIN\#12}$) Vdc	Converter State
0 ⟷ 1.25	On
1.55 ⟷ 5.00	Off
High Impedance	On

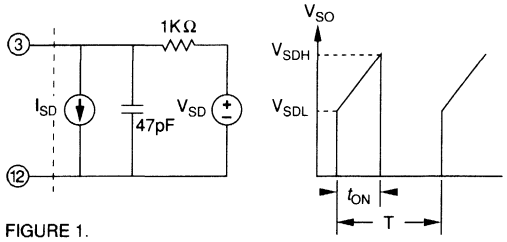


FIGURE 1.

TABLE 2.

Parameter		V_{IN} = 16	V_{IN} = 40
t_{ON}		1.96µs	0.67µs
V_{SDL}		500mV	460mV
V_{SDH}		570mV	680mV
T	—	2µs	(Typical)
I_{SD}	—	±15µA	(Max)

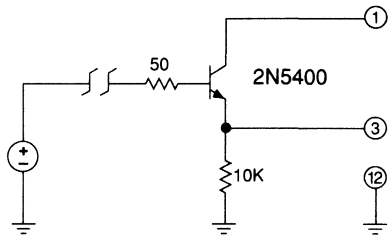


FIGURE 2.

LAYOUT CONSIDERATIONS

Careful placement of a DC/DC converter relative to its input source or bus and its load, improves both DC and transient performance. When a multiple converter system is being designed for a common load, the location of all the converters should be electrically identical to insure equal load sharing.

When the physical location of the input voltage and the load are fixed, a designer may optimize the actual location of a converter for efficiency. Figure 3 shows a typical situation where the load and the line are separated by a known fixed distance. The size of the conductors has been decided by other design considerations, i.e.current density; therefore, their resistivity in known. The input and output resistances are then functions of length. Given the input voltage/current and output voltage/current, a maximum efficiency position for the converter is approximately given by:

$$\text{Where:} \quad X_{IN} = \frac{X_T K_{IN} \cdot I_{OUT}^2}{(K_{OUT} \cdot I_{OUT}^2 - K_{IN} I_{IN}^2)}$$

X_{IN} = Distance between input voltage and converter
X_T = Total distance between input voltage and load
I_{IN} = Input current
I_{OUT} = Output current
K_{IN} = Input line resistivity
K_{OUT} = Output line resistivity
R_{IN} = Lumped input line resistance
R_{OUT} = Lumped output line resistance

Note that R_{OUT} will reduce the output voltage as seen by the load unless the output voltage is actually sensed at the load. The DB2800 series employs remote sensing so this error can be corrected.

When multiple converters are used, additional considerations are necessary. Figure 4 shows a non-ideal layout of three converters, each driving a separate load. The first problem with this design is that

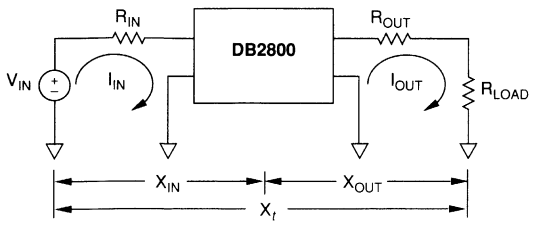


FIGURE 3.

the input voltage to any one converter is dependent on the input current to all converters. Additionally, any increase in the load current to any one converter generates a transient input voltage which is felt by all the converters which then generates an output voltage transient. Figure 5 shows a more preferred layout. With this connection, any one of the three converters can operate through a transient or DC imbalance without affecting the entire system performance.

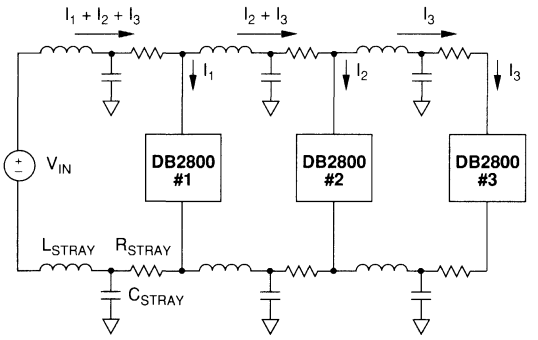


FIGURE 4.

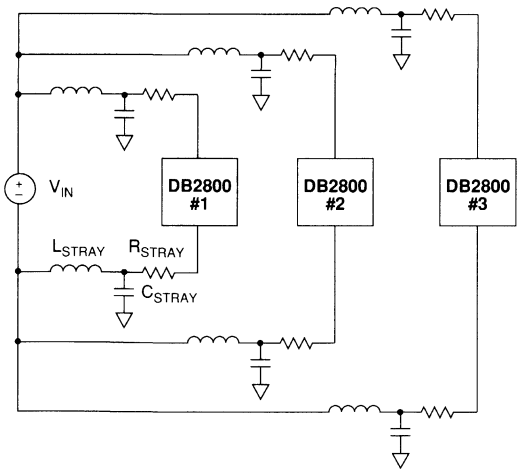


FIGURE 5.

THERMAL MANAGEMENT

Since a DC/DC converter is not a 100% efficient device, some of its input power will be converted into heat. Proper thermal design and management should be achieved to improve reliability and insure the maximum case temperature of the converter is not exceeded. Improving the thermal performance of the converter system ultimately results in lowering the thermal resistance between the converter and some cooler body.

Any power absorbed by the converter that is not delivered to the load is dissipated in the converter as heat. We can calculate this power by using the following formula:

$$\text{Where:} \quad P_{DISS} = P_{OUT}\left(\frac{1-\eta}{\eta}\right) \tag{1}$$

P_{DISS} = Power dissipated by the DB2800
P_{OUT} = Power dissipated by the load
η = Efficiency of the DB2800

The P_{OUT} used here is the worst case or highest steady power expected. The efficiency η can be determined from the appropriate data sheet given the output current and input voltage.

Once P_{DISS} is determined, the thermal design can be done as follows. An electrical equivalent of the thermal system can be constructed using the standard power to current, temperature to voltage and thermal resistance to resistance analogs. A thermal schematic of a DB2800 converter and its environment is shown in Figure 6, where:

θ_{INT}	=	Internal thermal resistance	(°C/W)
θ_{CS}	=	Case to heatsink thermal resistance	(°C/W)
θ_{CA}	=	Case to ambient thermal resistance	(°C/W)
T_{HS}	=	Heatsink temperature	(°C)
T_{AMB}	=	Ambient temperature	(°C)
T_{CASE}	=	Case temperature of the converter	(°C)
T_{INT}	=	Internal temperature of the converter	(°C)

The next figure shows both a heatsink and an ambient environment as sinks for P_{DISS}. When a heatsink is not used, θ_{CS} and T_{HS} are removed. The case temperature can be shown to be equal to:

$$T_{CASE} = \frac{P_{DISS} \cdot \theta_{CA} \cdot \theta_{CS} + T_{HS} \cdot \theta_{CA} + T_{AMB} \cdot \theta_{CS}}{\theta_{CA} + \theta_{CS}} \tag{2}$$

When no forced air for cooling is used, the θ_{CA} value is fixed, being dependent on the geometry and material of the converter package. For the DB2800 series, θ_{CA} is approximately 6°C/W.

Given an internal power dissipation, a desired case temperature rise, a case to ambient thermal resistance, and both ambient and heat sink temperatures, then a heatsink may be designed or selected. Equation 2 is reorganized for θ_{CS}:

$$\theta_{CS\,(MAX)} = \frac{(T_{CASE} - T_{HS}) \cdot \theta_{CA}}{(P_{DISS} \cdot \theta_{CA} + T_{AMB} - T_{CASE})} \tag{3}$$

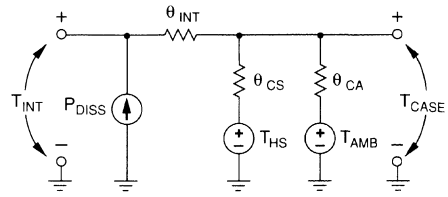


FIGURE 6.

EXTERNAL FILTER SELECTION

To improve the input ripple current, output ripple voltage, and/or the ripple voltage rejection of a DC/DC converter, additional filtering is required. Reducing the input ripple current normally requires an input L-C filter. Improving the output ripple voltage can begin with additional output capacitance. Increasing the ripple voltage rejection ratio can be accomplished with either technique. Whenever additional filtering is added to a DC/DC converter, the AC characteristics are changed. The design of the additional filter must not only produce the desired improvement, but also not produce instability within the converter.

Fortunately, the input filter/stability question has been sufficiently analyzed resulting in a set of analytical guidelines for the design. The necessary information about the converter are its input ripple and impedance characteristics. The basic design goal for an input filter is to place its output impedance pole frequency, as seen by the converter, at least one decade below the converter's input impedance pole frequency.

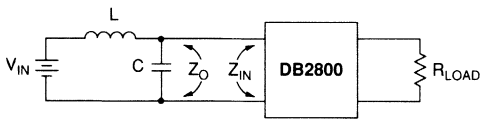


FIGURE 7.

The idea here is to make the output impedance of the filter much smaller than the input impedance of the converter at any frequency. Figure 7 shows schematically the impedances involved. The input impedance of the DB2800 series is shown in the appendix of this application note. The Magnitude of Z_{OUT} at any frequency is given by:

$$|Z_{OUT}| = \frac{2\pi fL}{1 - 4\pi^2 f^2 LC}$$

The pole frequency of Z_{OUT} is given by:

$$f_{ZOUT} = \frac{1}{2 \cdot \pi \cdot \sqrt{LC}}$$

The design begins with determining the amount of attenuation required at some frequency. From the input ripple current spectrum graphs one can determine the magnitude of the various ripple components. To convert from dBμA to amps, the following formula is used:

$$I_{pk}\,(\text{Amps}) = 1\mu A \cdot A\,\text{LOG}\left(\frac{Ipk(db\mu A)}{20}\right)$$

To determine the LC product, an asymptotic approximation can be done using logarithmic/linear paper after[1]. An example of this approach is shown in Figure 8.

1. Scale the vertical axis at -20dB per division starting at 0 dB.
2. Scale the logarithmic axis for the frequency band of interest.
3. Draw a horizontal line on the 0dB level, the low frequency attenuation of the LC filter.
4. Mark off the amount of attenuation required at the frequency of interest.
5. Draw a 40 dB/decade line up to the 0 dB attenuation level.
6. The frequency at which the line in Step 4 intersects 0 dB is the pole frequency of the filter.
7. Verify that this frequency is much lower than the input impedance break frequency point. If not, repeat steps 3 through 6 using more attenuation at the frequency of interest.

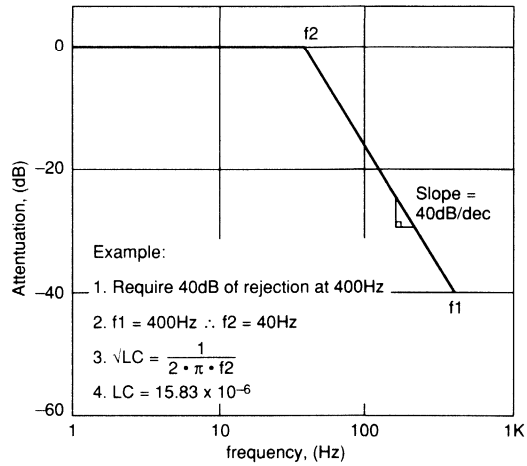


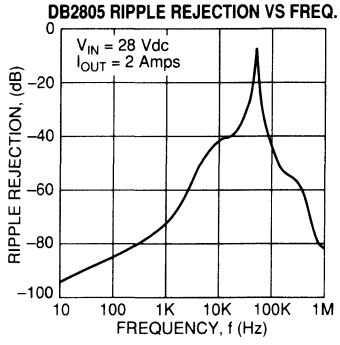
FIGURE 8.

Reducing the output voltage ripple is usually done with the addition of an external capacitor across the output of the DC/DC converter. Again the design starts with the amount of attenuation required. The ripple voltage vs. frequency graphs can be used to determine the magnitudes of the various ripple components. The output impedance of the converter, together with the ripple magnitude, can be used to form a simple RC circuit from which a capacitance value can be determined.

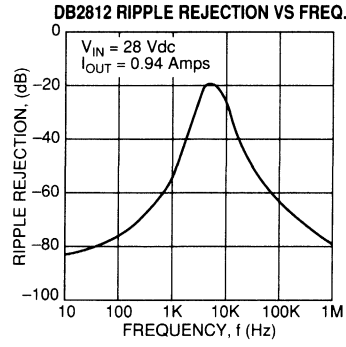
When adding additional filtering to a DB2800, the transient, startup and d.c. characteristics of the converter should be verified. The converter should be tested for all known line and load variations prior to adding any external filtering. Once the filter(s) have been added, the converter should be tested again under the same line and load variations to verify that the stability of the converter has not been compromised.

[1] *Switch Mode Power Conversion*
Author: K. Kit Sum
Marcel Dekker, Inc. Copyright 1984

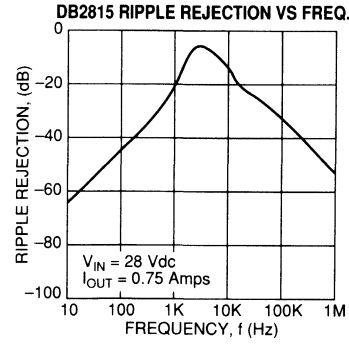
DB2805 RIPPLE REJECTION VS FREQ.



DB2812 RIPPLE REJECTION VS FREQ.

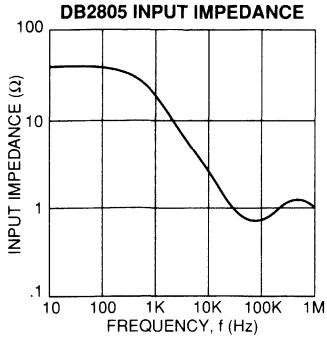


DB2815 RIPPLE REJECTION VS FREQ.

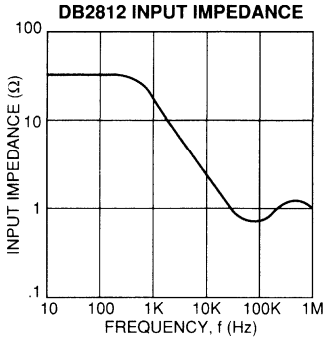


APPENDIX

DB2805 INPUT IMPEDANCE



DB2812 INPUT IMPEDANCE



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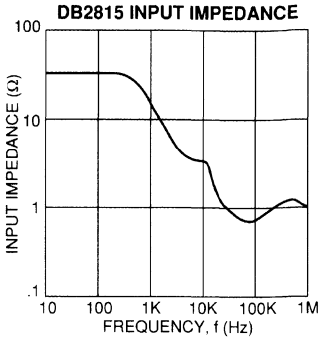

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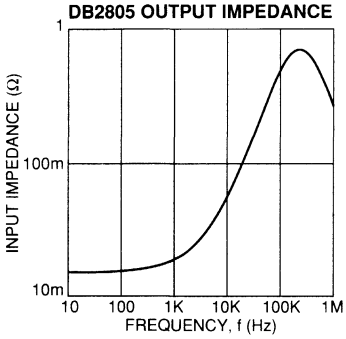

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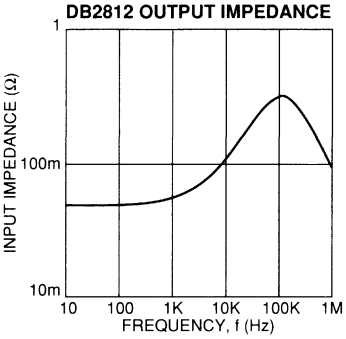

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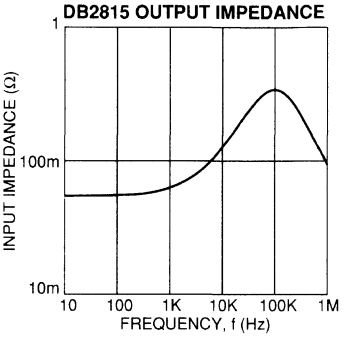
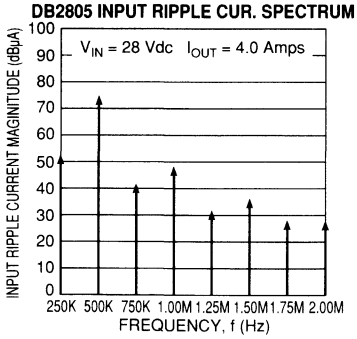


DB2805 INPUT RIPPLE CUR. SPECTRUM



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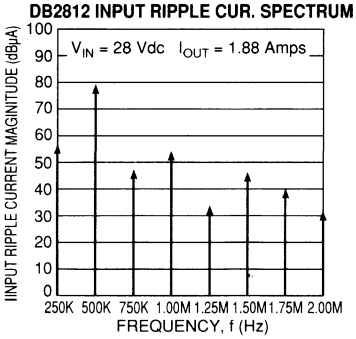

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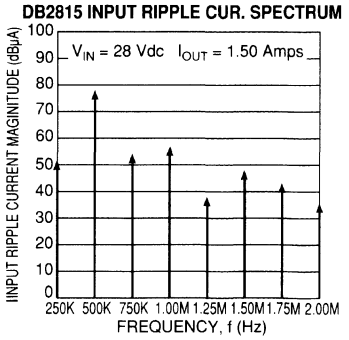
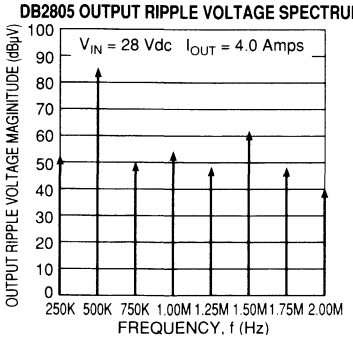
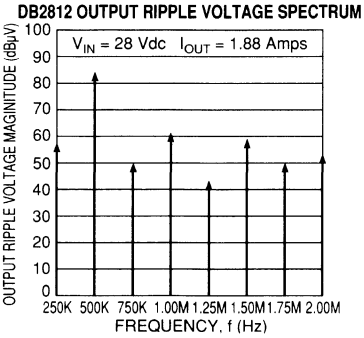


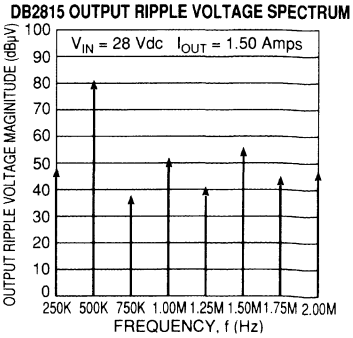
DB2805 OUTPUT RIPPLE VOLTAGE SPECTRUM



DB2812 OUTPUT RIPPLE VOLTAGE SPECTRUM



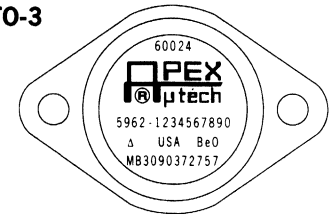
DB2815 OUTPUT RIPPLE VOLTAGE SPECTRUM



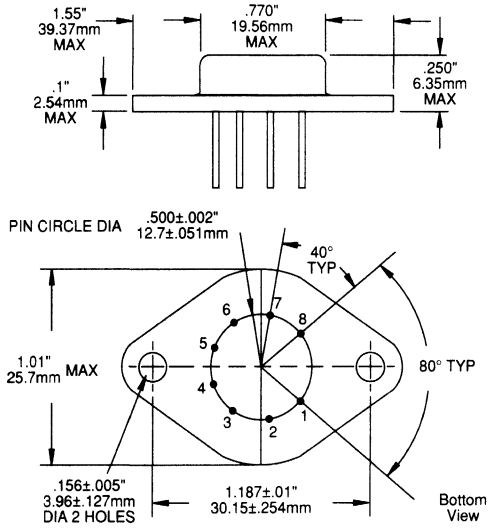
PACKAGES AND ACCESSORIES

NOTES:

8-PIN TO-3



NOTE: ESD triangle (Δ) on top of package denotes pin 1 location.

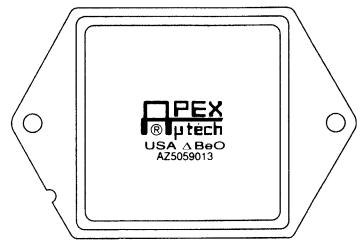


PIN DIAMETER:	.965/1.067mm or .038/.042"
PIN LENGTH:	12.19/12.70mm or .480/.500"
PIN MATERIAL, STD:	Nickel plated alloy 52, solderable
PIN MATERIAL, MIL:	Gold plated alloy 52, solderable
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	15 grams or .53 ounces
ISOLATION:	500VDC any pin to case
SOCKETS:	APEX PN: MS03
CAGE JACKS:	APEX PN: MS02 (Set of 8)
HEATSINKS:	APEX PN: HS01 thru HS05

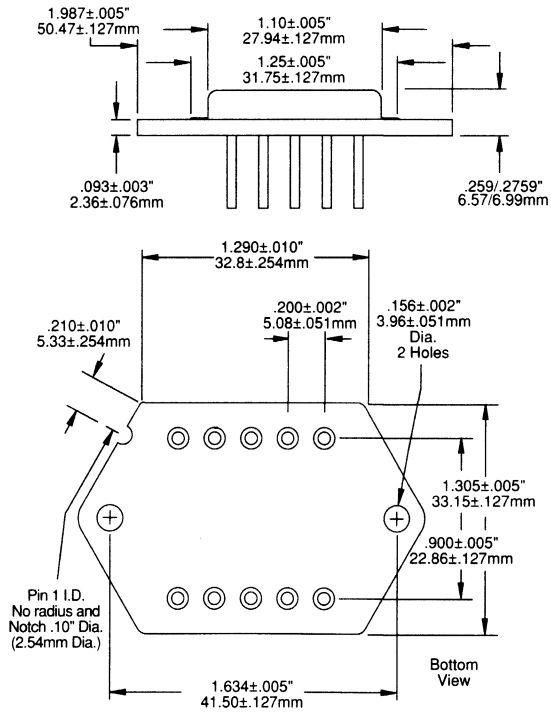
CAUTION

Recommended mounting torque is 4-7 in•lbs (.45 - .79 N•m)

PD10/60S



NOTE: Notch on package base denotes pin 1 location.



PIN DIAMETER:	1.47/1.57mm or .058/.062"
PIN LENGTH:	11.43/12.70mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	36 grams or 1.27 ounces
ISOLATION:	500VDC any pin to case
CAGE JACKS:	APEX PN: MS04 (Set of 12)

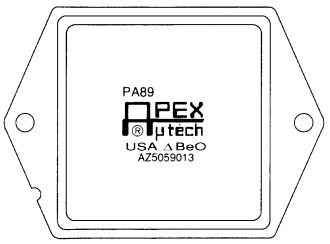
CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

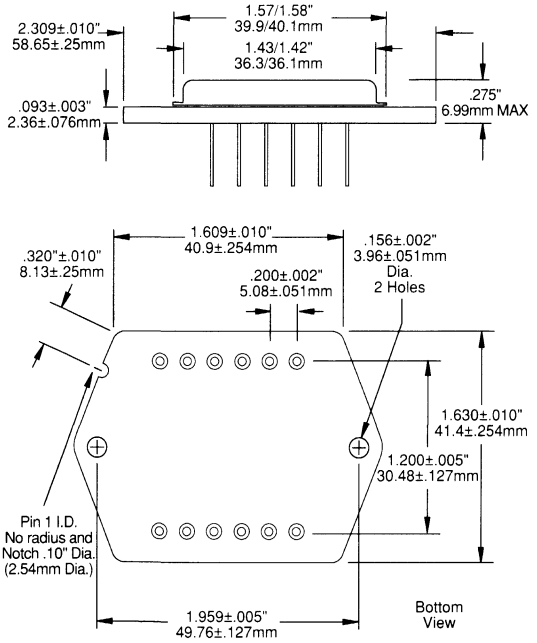
POWER DIP™ PACKAGES

OUTLINE DIMENSIONS

MO-127 HIGH VOLTAGE



NOTE: Notch on package denotes pin 1 location.



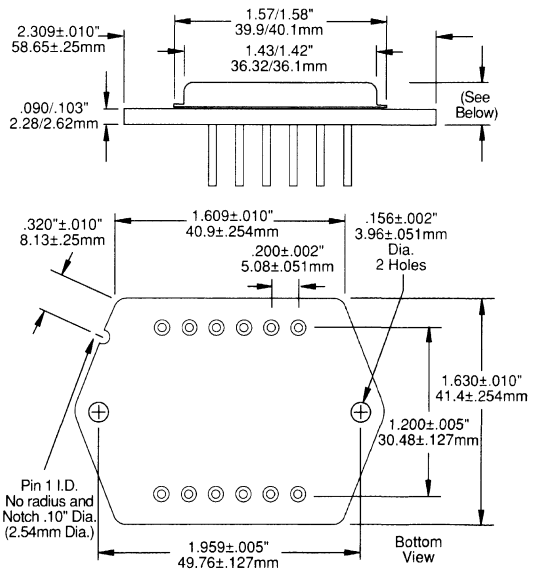
PIN DIAMETER:	.584/.686mm or .023/.027"
PIN LENGTH:	11.43/12.70mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	53 grams or 1.87 ounces
ISOLATION:	1200VDC any pin to case
CAGE JACKS:	N/A
MATING SOCKET:	MS06
HEATSINK:	HS06, HS11

CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

JEDEC MO-127 (STD) & MO-127 COPPER

NOTE: Notch on package denotes pin 1 location.



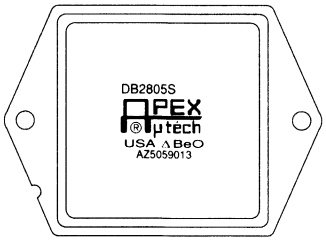
PIN DIAMETER:		1.47/1.57mm or .058/.062"
PIN LENGTH:		11.43/12.7mm or .450/.500"
PIN MATERIAL, STD:		Nickel plated steel
ISOLATION:	STANDARD:	500VDC any pin to case
	COPPER:	300VDC any pin to case
HEIGHT:	STANDARD:	7.37mm OR .275" MAX
	COPPER:	8.89mm OR .350" MAX
PACKAGE:	STANDARD:	Hermetic, nickel plated steel
	COPPER:	Base: Nickel plated copper
WEIGHT:	STANDARD:	53 grams or 1.87 ounces
	COPPER:	58 grams or 2.05 ounces
CAGE JACKS:		APEX PN: MS04 (Set of 12)
MATING SOCKET:		APEX PN: MS05
HEATSINK:		APEX PN: HS06, HS11

CAUTION

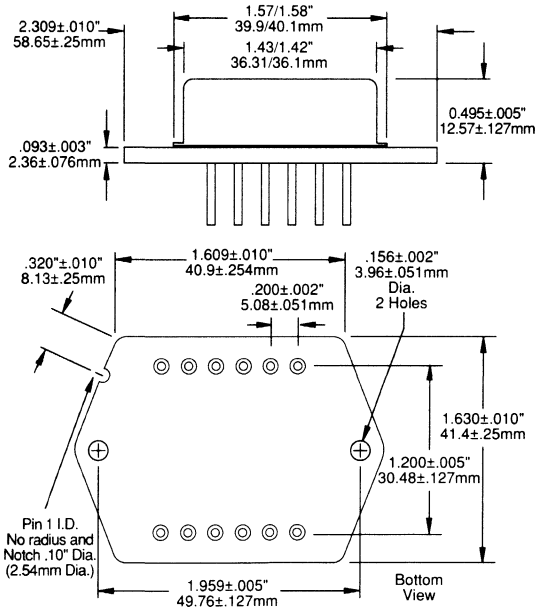
Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

POWER DIP™ PACKAGES

MO-127 HIGH PROFILE



NOTE: Notch on top of package denotes pin 1 location.



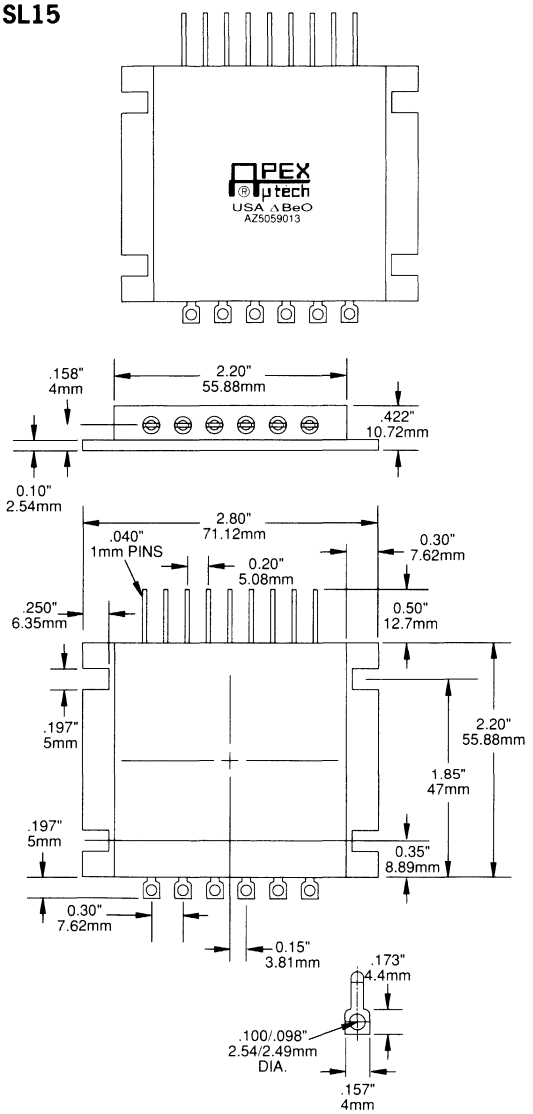
PIN DIAMETER:	1.47/1.57mm or .058/.062"
PIN LENGTH:	11.43/12.7mm or .450/.500"
PIN MATERIAL, STD:	Nickel plated steel
ISOLATION:	500VDC any pin to case
PACKAGE:	Hermetic, nickel plated steel
WEIGHT:	54 grams or 1.90 ounces
CAGE JACKS:	APEX PN: MS04 (Set of 12)
MATING SOCKET:	APEX PN: MS05
HEATSINK:	APEX PN: HS06, HS11

CAUTION

Recommended mounting torque is 8-10 in•lbs (.90 - 1.13 N•m)

SIDE LEAD PACKAGES

SL15



PIN PLATING:	Gold
PACKAGE:	Hermetic, Nickel Plated
WEIGHT:	150g or 5.3 oz.

CAUTION

Recommended mounting torque is 5-7 in•lbs (.56 - .79 N•m)

ACCESSORIES INFORMATION

HEATSINKS

A wide spectrum of applications can be satisfied with the heatsinks stocked as accessories for APEX power amplifiers. All are made of aluminum to provide high levels of conduction. HS01 clamps over the TO-3 case using virtually no additional space on a printed circuit board. HS02 is suitable for chassis or printed circuit mounting. HS03 through HS05 are designed for chassis mounting. The HS09 is a second source for 0803HS from Burr-Brown. Despite its small size, it is more effective than HS01. The HS11 provides the most protection for prototyping or for production of high power products. All chassis mountable heatsinks are pre-drilled for the 8-pin TO-3 hole pattern, except the HS06, which is pre-drilled for the 12 pin, MO-127 package. In large volume most of these heatsinks may be procured from AAVID Engineering Inc. Conservative calculations are recommended for prototype work while performance graphs are included to enable optimization for production runs. Due to calculation complexity of thermal circuits and of power dissipation levels where reactive loads are driven, it is often helpful to utilize temperature measurements after the electrical design has been completed.

APEX PN	RATING 1	RATING 2	RATING 3	AAVID PN
HS01	11.6	6.0	4.2	5427B
HS02	4.5	3.2	2.5	5680B-0150-15
HS03	1.7	1.4	1.0	6050-3B-15
HS04	.95	.57	.44	60650-3B-15
HS05	.85	.7	.53	6055-5.5B-15
HS06	.60	-	-	A-002-141-39
HS09	11.7	-	6.6	-
HS11*	.68	-	-	-

Ratings are all thermal resistances from amplifier mounting surface to ambient expressed as °C/W. Rating 1 is for an unobstructed mounting of optimum orientation. Rating 2 pertains to forced air at a velocity of 100 FPM and Rating 3 is for 200 FPM. For further details consult individual heatsink graphs.

* Efficiency improves for water cooling.

HEATSINK THRU-HOLES

Custom heatsink manufacture or mounting of the Apex power amplifier to a bulkhead for heatsinking, requires the use of heatsink thru-holes for the external connection pins. For the 8-pin TO-3 package the main path for heat flow occurs inside the circumference of 8 pins. (Refer to Figure 1)

Therefore, a single large hole, (to allow the 8 pins to pass through), will remove the critical heatsink material from where it is most needed. Instead, 8 separate holes must be drilled. Refer to Table 1 for recommended drill sizes for heatsink thru-holes for Apex power amplifier packages.

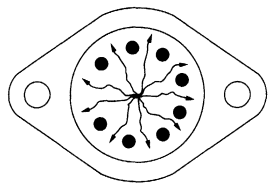


Fig. 1: Main heat flow path, 8-pin to TO-3 package.

APEX PACKAGE	RECOMMENDED DRILL SIZE	HOLE DIAMETER INCHES	mm
8-PIN TO-3	#46	.081±.002	2.057±.051
PD10/60	#37	.104±.002	2.642±.051
MO-127	#37	.104±.002	2.642±.051
MO-127 High Voltage	#50	.070±.002	1.781±.051

Table 1: Heatsink thru-hole sizes.

TEFLON TUBING

Anodized heatsinks can be easily nicked or scratched, exposing bare aluminum, which is an excellent electrical conductor. When mounting the Apex power amplifier using a socket, it is recommended to sleeve, with Teflon tubing, a minimum of two opposite pins. This centers the external connection pins in the heatsink thru-holes and prevents electrical shorts when tightening the power amplifier down on a heatsink. When soldering directly to external connection pins it is recommended to sleeve, with Teflon tubing, all pins. Table 2 lists the recommended Teflon tubing and some suggested manufacturers (for manufacturers' phone numbers, see "Vendors for Power Op Amp Accessories").

TUBING DIMENSIONS

APEX PACKAGE	Nominal I.D. Inches	Nominal I.D. mm	Nominal O.D. Inches	Nominal O.D. mm	MFG.	MFG. PART NO.
8-PIN TO-3	.042	1.067	.074	1.88	★	TSI-S18
					★★	TFT-250-18
PD10/60	.066	1.676	.098	2.489	★	TSI-S14
MO-127					★★	TFT-250-14
MO-127 High Voltage	.028	.711	.052	1.321	★	TSI-S22
					★★	TFT-250-22

Table 2: Teflon tubing. ★ SPC Technology ★★ Alpha Wire Corp.

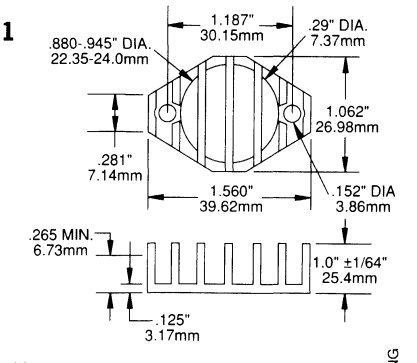
RECOMMENDATIONS FOR THERMALLY CONDUCTIVE WASHERS

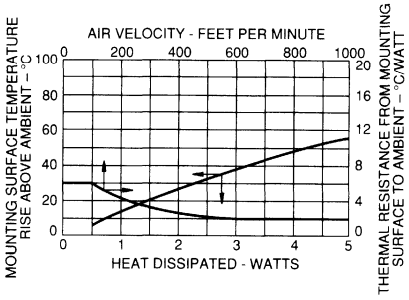
Power Devices Inc. AL-155-10C "Thermstrate" provides maximum thermal conductivity equal to thermal grease. It is electrically conductive but this will not be a problem with the isolated packages of Apex amplifiers.

In rare occasions where electrical insulation is required, the Crayotherm T0-3-8, CR2-MT provides thermal conductivity equal to a mica washer and grease.

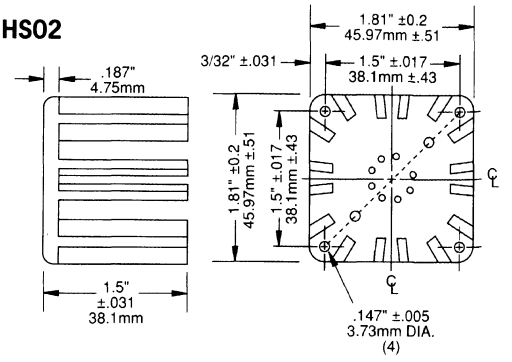
No others are considered acceptable. We will not warranty failed amplifiers used with other make/model of washers. Any thermal compound other than plain grease (such as thermally conductive adhesives) will also void the warranty.

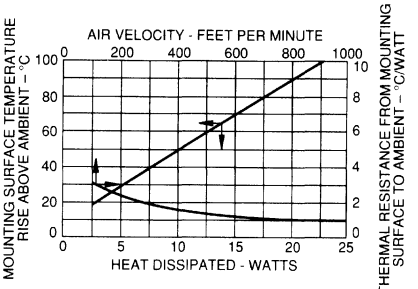
HS01



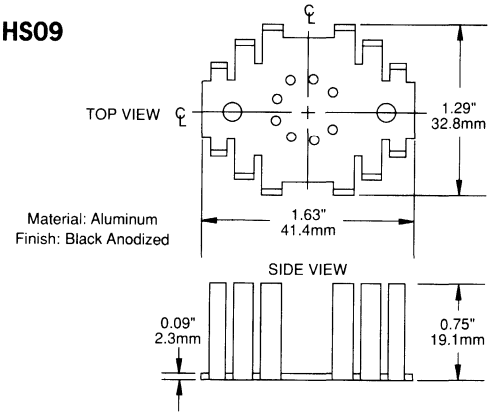


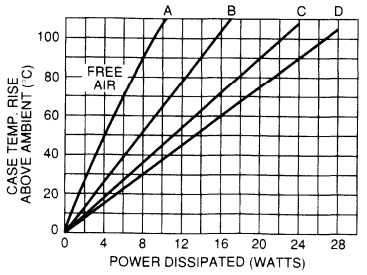
HS02





HS09

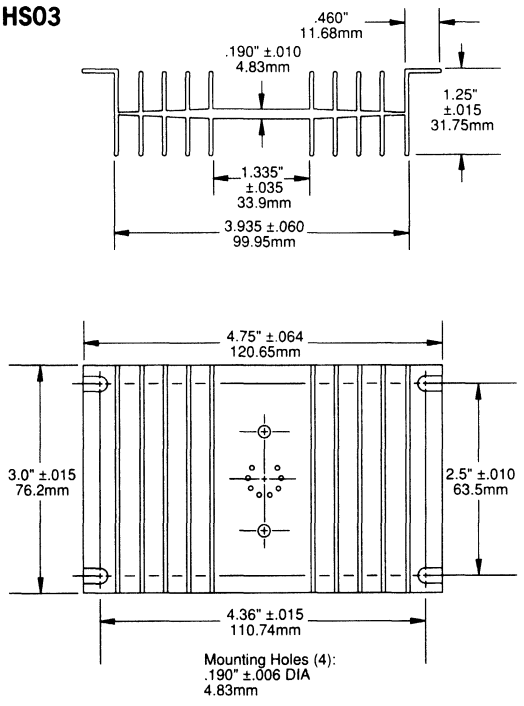


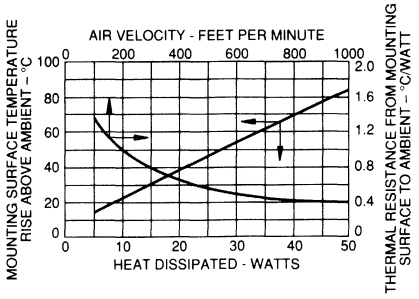


DESCRIPTION
OF CURVES
A. N.C. Horiz. & Vert with Dissipator (Free Air)
B. 200 FPM w/ Diss.
C. 500 FPM w/ Diss.
D. 1000 FPM with Dissipator

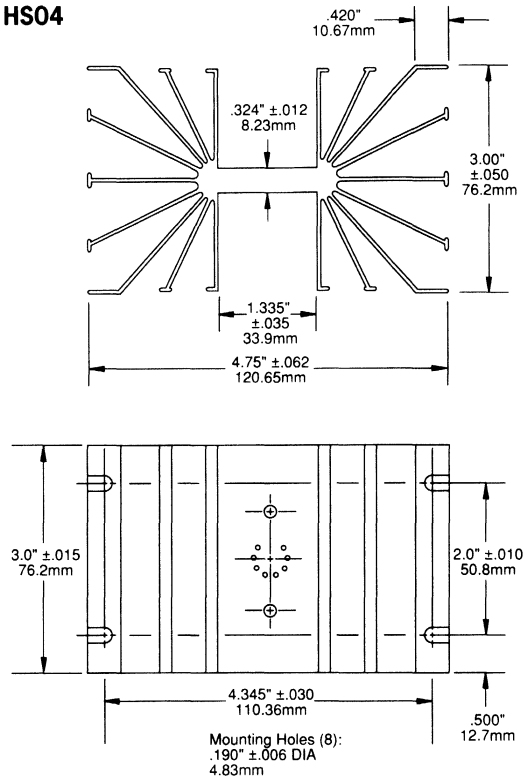
HEATSINKS

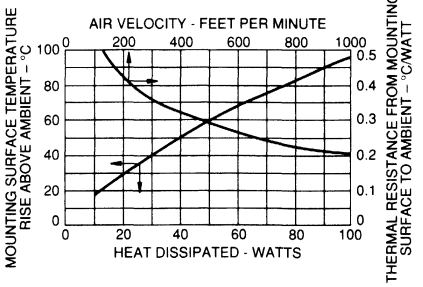
HS03





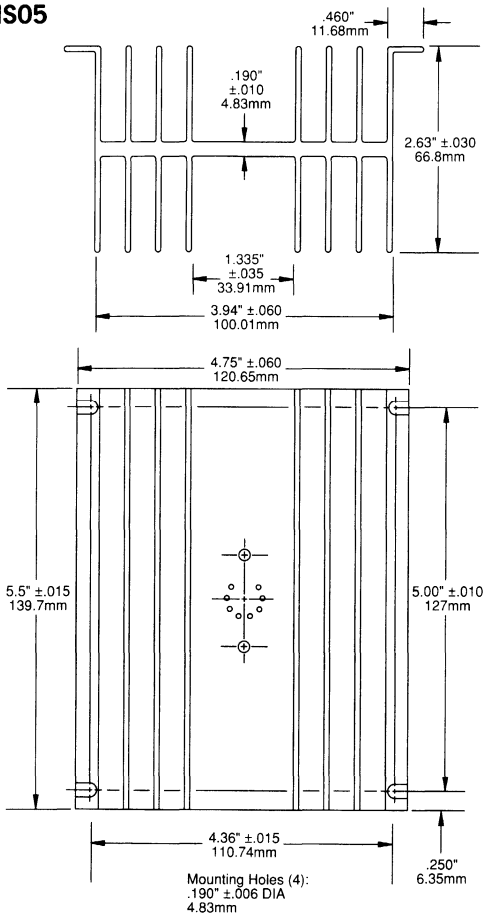
HS04

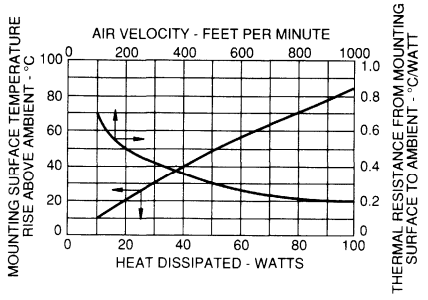




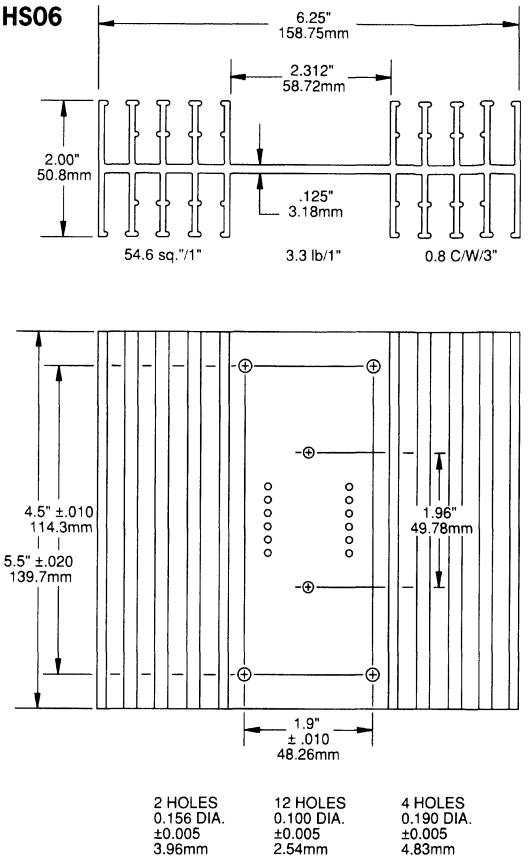
HEATSINKS

HS05





HS06



Standard Commercial
Extrusion Tolerances Apply

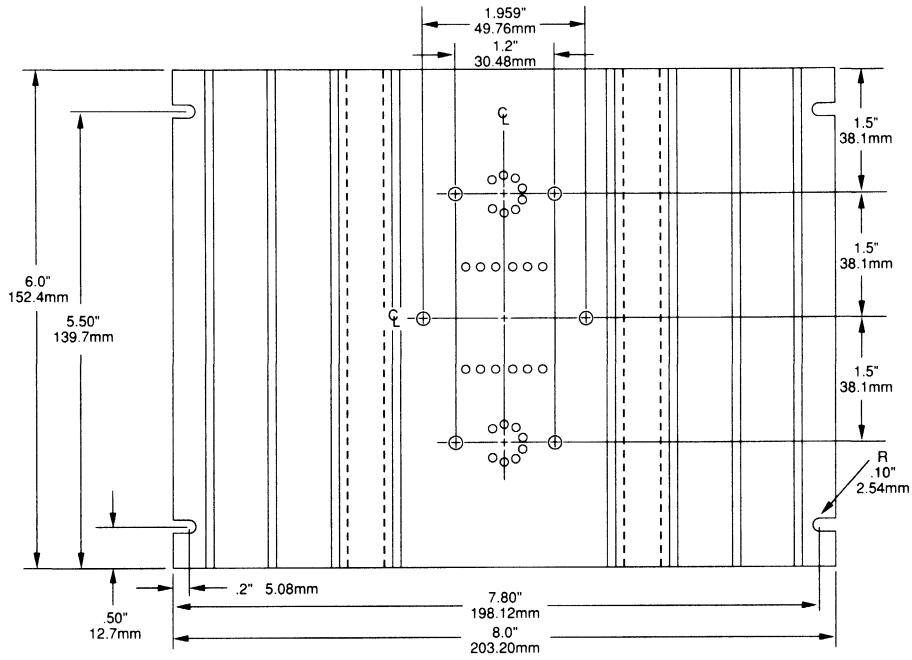
Material: Aluminum Alloy

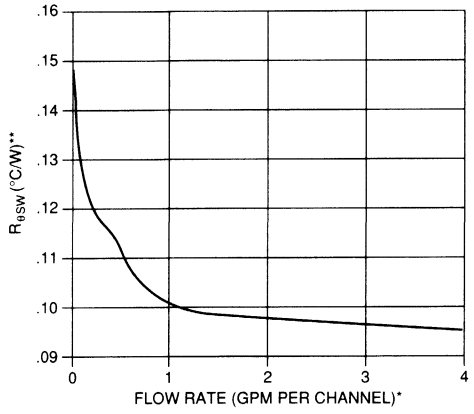
Finish: Black Anodize

Thermal Resistance: ≈ .6°C/W

AAVID P/N: A-002-141-39

HS11





$R_{\theta SA}$ = .675 °C/W (Free air vertical)

$R_{\theta SW}$ = .102 °C/W (Water cooled @ 1 GPM per channel)

Additional mounting loss (with thermal grease):
PD12: .008 - .017 °C/W
TO-3: .05 - .1 °C/W

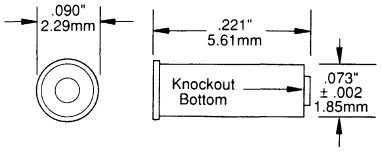
* BOTH CHANNELS FED IN PARALLEL USING CLEAN WATER
** $R_{\theta SW}$ = THERMAL RESISTANCE FROM HEATSINK TO WATER

CAGE JACKS & MATING SOCKETS

REFER TO APPLICATION NOTE 11 FOR MOUNTING TECHNIQUES USING CAGE JACKS AND MATING SOCKETS

MS02/CAGE JACK

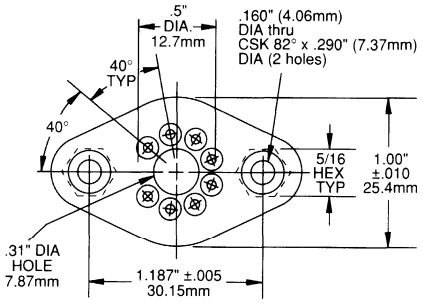
(Package of 8 for PC board insertion)
.040" DIA. PINS — 8-PIN TO-3 PACKAGE

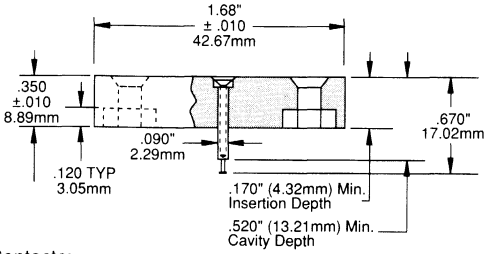


Recommended Mounting Hole: .076"±.002 DIA (#48 Drill)
Minimum Insertion Depth: .10
Knockout Tools : Tip: 435-3935-01-00-00
(for long pins) Impact Tool: 435-3101-00-00
1:1 Layout Template is Available
Cambion PN: 450-3716-01-03

MS03/MATING SOCKET

.040" DIA. PINS — 8-PIN TO-3 PACKAGE

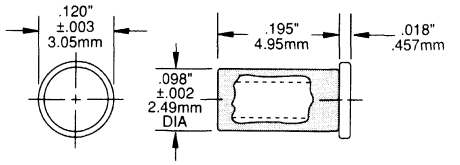




Contacts:
Resistance: .020Ω MAX
Contact Body: Brass
200/300µ in. Tin over 100/150µ in. Nickel
Inner Contact Clip: BeCu
30µ in. Gold over 50µ in. Nickel
Socket Body: Polyester, Glass Filled, 94 V_O–Rating
Color: Green
Operating Temperature Range: –55°C to +125°C

MS04/CAGE JACK

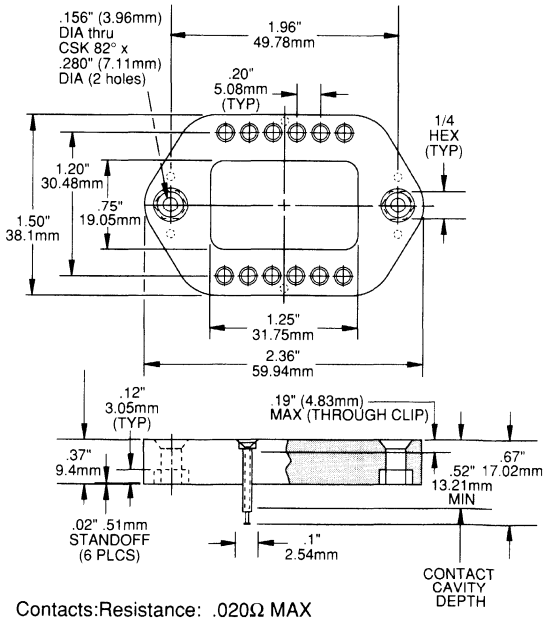
(Package of 12 for PC board insertion)
.060" DIA. PINS —POWER DIP™ PACKAGES
—PD10/60S —MO-127



Recommended Mounting Hole: .102"±.002 DIA (#38 Drill)
Hole Depth: .200 Minimum
Material: Body: Brass
Spring: Beryllium Copper
Finish: Body: 20µ in. Soft Gold over 200µ in. Copper
Spring: 500µ in. Hard Gold over 200µ in. Copper
Cambion PN: 450-3326-01-03-00

MS05/MATING SOCKET

.060" DIA. PINS —POWER DIP™ PACKAGES
—MO-127



Contacts:Resistance: .020Ω MAX
Contact Body: Brass
200/300µ in. Tin over 100/150µ in. Nickel
Inner Contact Clip: BeCu
30µ in. Gold over 50µ in. Nickel
Socket Body: Polyester, Glass Filled, 94 V_O–Rating
Color: Green
Operating Temperature Range: –55°C to +125°C

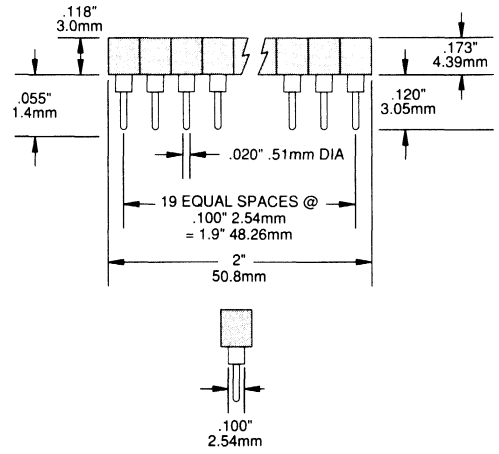
ACCESSORIES
INFORMATION

MATING SOCKETS & THERMAL WASHERS

REFER TO APPLICATION NOTE 11 FOR MOUNTING TECHNIQUES USING CAGE JACKS AND MATING SOCKETS

MS06/MATING SOCKET

.025" DIA. PINS—MO-127 HIGH VOLTAGE

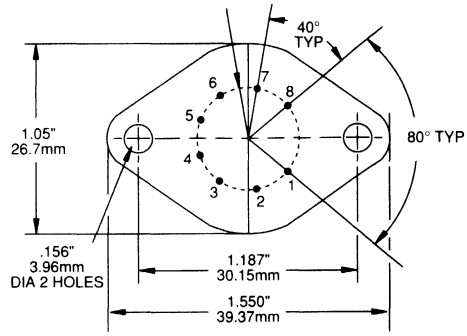


Body: Black polyester, glass filled
Contacts: Beryllium Copper
Shell: Half Hard Brass
PCB Hole: .035" ±.002", .889mm ±.051mm
Insulation Resistance: 5000 megohms minimum
Dielectric Withstanding Voltage: 500 volts AC
Flammability: UL 94V-0
Temperature Range: -65°C to +125°C

Robinson Nugent Part Number: SBE-20-S-TG
S = Solder Tail
TG = 10 µinch (.254µm) minimum
Gold on contact area
200 µinch (5.08 µm) minimum Tin on terminal area
50 µinch (1.27µm) minimum Nickel underplate

TW03/THERMAL WASHER

FOR 8-PIN T0-3 PACKAGE



PIN CIRCLE DIAMETER .500" OR 12.7mm
PIN DIAMETER .090" or 2.29mm

NOTE:

1. TW03 is electrically and thermally conductive. Thermal conductivity is superior to grease.
2. TW03 available in packages of 10 only.
3. For optimum thermal transfer, avoid abrasive handling of TW03 which can damage its .5 mil thick layer of dry thermal compound with which each side is coated.
4. Power Devices part number: Thermstrate AL-155-10C.

ACCESSORIES VENDORS

VENDORS FOR POWER OP AMP ACCESSORIES

The following list answers the most common requests received on the APEX Applications Hotline. It is by no means a complete list of sources, but can save you valuable time locating your requirements.

HEATSINKS

AAVID Engineering , Inc.
Two Kool Path, P.O. Box 4000, Laconia NH 03247
(603) 528-3400

EG&G Wakefield Engineering
60 Audubon Rd., Wakefield MA 01880 (617) 245-5900

International Electronic Research Corp.
135 W. Magnolia Blvd., Burbank, CA 91502-7704
(818) 842-7277

Thermalloy, Inc.
2021 W. Valleyview Lane, Dallas TX 75234-9990
(214) 243-4321

TEFLON TUBING

Alpha Wire Corp.
711 Lidgerwood Ave., Elizabeth, NJ 07207-0711
(908) 925-8000

SPC Technology
4801 N. Ravens Wood, Chicago IL 60640
(312) 907-5181

MATING SOCKETS

Component Technologies, Inc.
7855 E. Evans, Suite A, Scottsdale, AZ 85260
(602) 998-1484

CAGE JACKS

Concord Electronics Corp.
30 Great Jones St., New York, NY 10012
(212) 777-6571

Interconnection Products, Inc.
2601 S. Garnsey, Santa Ana CA 92707 (714) 540-9256

RESISTANCE WIRE

MWS Wire Industries
31200 Cedar Valley Dr., Westlake Village CA 91362
(818) 991-8553

THERMAL GREASE

Thermalloy, Inc.
2021 W. Valleyview Lane, Dallas TX 75234-9990
(214) 243-4321

LOW VALUE RESISTORS

RCL Electronics, Inc.
U.S. 70 East, Smithfield, NC 27577
(919) 934-5181

Riedon Division
M.W. Riedel & Co.
300 Cypress Ave., Alhambra, CA 91802-1221
Mailing address: P.O. Box 1221, Alhambra, CA 91802-1221
(213) 283-7694

Kelvin
14724 Ventura Blvd., No. 1003
P.O. Box 826, Fajardo, Puerto Rico 00738
(809) 863-0066 FAX 863-5353

THERMALLY CONDUCTIVE WASHERS

Power Devices, Inc.
26941 Cabot Road
Building 124
Laguna Hills, CA 92653
(714) 582-6712

Crayotherm Corp.
1185 N. Van Horne Way
Anaheim, CA 92806
(714) 630-2696

NOTE:

Many of the above items can be purchased in small quantities through distributors such as:

Newark Electronics
(312) 784-5100 — Call for local branch office.

CUSTOMER SERVICE

ORDERING INFORMATION

TO PLACE AN ORDER:

Call 7:00 a.m. to 5:00 p.m. (MST) ..... **(602) 742-8601**
(14:00 to 24:00 Greenwich Mean Time)
or FAX ..... **(602) 888-3329**

Same Day Shipping on orders received by noon (MST)

DOMESTIC ORDERS

APEX MICROTECHNOLOGY ships most small orders from stock. If you need immediate delivery, call us direct before noon MST and specify "EXPRESS" service. We will make every effort to ship on the same day via air express.

EXPORT ORDERS

APEX F.S.C., the export arm of APEX MICROTECHNOLOGY, is represented throughout the industrialized free world by exclusive distributors who offer technical assistance and/or data sheets as well as speedy delivery at competitive prices. Evaluation orders can be shipped without delay to most countries.

EVALUATION ORDERS

EVALUATION orders are available in the United States. Your purchase order must specify "Evaluation" and is limited to a quantity of three amplifiers and three mating sockets. If the amplifiers do not meet your needs, have not been damaged (used within specification), have not been soldered, and are returned to APEX within 30 days, credit will be issued for both amplifiers and sockets.

CUSTOMIZING APEX PRODUCTS

APEX does customize standard models to meet specific customer requirements. Available options range from custom marking through minor internal circuit changes. Custom orders usually involve a minimum quantity, a per shipment lot charge, and a per piece surcharge over the cost of the standard model. The following are examples of services performed: standard part plus burn-in, test drift over wider temperature range, gradeout for improved voltage drift, customer part numbers up to 12 digits, gold flashed pins, individual test data and non-standard quiescent current trim.

TWO-YEAR WARRANTY

All products manufactured by APEX MICROTECHNOLOGY are warranted to be free of defects under specified operating conditions for a period of two years from the original shipment date. Conformance to specifications at time of shipment is certified.

The warranty applies only to the original customer and is in lieu of all other warranties, expressed or implied. Under no condition will APEX MICROTECHNOLOGY be liable for any anticipated profits, consequential damages, loss of time or other losses incurred by the customer in connection with the purchase and/or use of the product.

TECHNICAL SUPPORT

Technical assistance is available toll free from 7:00 a.m. to 5:00 p.m. MST Monday-Thursday, 7:00 a.m. to 1:00 p.m. MST Friday. APEX application engineers are professionals with extensive design experience. They can help you select the appropriate product, debug your design, and suggest design approaches. Our toll-free number is (800) 421-1865.

SOURCE INSPECTION AND SURVEYS

APEX supports Vendor Quality verification through surveys, source inspections and audits. Source inspection must be requested at the time of order placement. Scheduling of source inspection within 5 working days is required. When product is ready for source inspection, we will notify you by fax or telephone. Standard charges apply if source inspection takes place within 5 working days after which extra charges will apply. Please see *Special Services* price list for charges.

QUALITY ASSURANCE

All APEX MICROTECHNOLOGY industrial grade products are functionally tested and visually inspected to the intent of method 2017 (excluding high power die visual) of MIL-STD-883 prior to capping. After the package is hermetically sealed, static and dynamic final electrical tests are performed. Final marking includes a lot code traceable to the flow sheets kept on record. The Quality Department reports directly to the president of the company.

Military products are built in accordance with MIL-H-38534. Quality Conformance Inspection is performed in accordance with MIL-H-38534 Option 1. Group A data is kept on file with the production records. Generic In-line Group B, C and package evaluation data is on file. Please see *Special Services* price list for non-standard data requirements charges.

FAILURE ANALYSIS

In case of failure within the two year warranty period, DO NOT RETURN the product without first calling the APEX Applications Hotline to explain the problem and receive a Return Material Authorization number.

The device will be tested, opened, and inspected visually to determine the cause of failure. A "Failure Analysis" will be supplied free of charge. This information will help you maximize reliability and avoid future failures.

COMPANY ACCESS, TERMS & CONDITIONS

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

HOURS OF OPERATION

	Mountain Standard Time	Day	Greenwich Mean Time
Order Entry	7:00 a.m. to 5:00 p.m.	Mon-Fri	14:00 to 24:00
Applications	7:00 a.m. to 5:00 p.m.	Mon-Thur	14:00 to 24:00
	7:00 a.m. to 1:00 p.m.	Fri	14:00 to 20:00
All Other Departments	7:00 a.m. to 4:00 p.m.	Mon-Thur	14:00 to 24:00
	7:00 a.m. to 1:00 p.m.	Fri	14:00 to 20:00

MAILING AND SHIPPING ADDRESS INFORMATION FOR ALL DEPARTMENTS

APEX MICROTECHNOLOGY CORP. (Domestic)
APEX F.S.C. INC. (Export)
5980 N. Shannon Road
Tucson, AZ 85741, USA

TELEPHONE INFORMATION

SWITCHBOARD
Connects to all departments
(602) 742-8600

FAX
(602) 888-3329

TELEX
170631

APPLICATIONS TOLL-FREE HOTLINE
Connects directly to Applications
US & Canada only
(800) 421-1865

PRODUCT LITERATURE TOLL-FREE HOTLINE
For product literature requests
(800) 448-1025

APPLICATIONS ENGINEERING
(602) 742-8662, (602) 742-8663

CUSTOMER SERVICE
(602) 742-8601

ORDER ENTRY
(602) 742-8601

SALES
(602) 742-8609

QUALITY ASSURANCE
(602) 742-8619

APEX F.S.C. INC. (export)
(602) 742-8606

ACCOUNTS RECEIVABLE
(602) 742-8653

CHIEF EXECUTIVE OFFICER
(602) 742-8679

TERMS AND CONDITIONS

SHIPMENTS will be fully insured and sent via air express unless otherwise specified. F.O.B. is Tucson, AZ. For shipments via the Postal Service a $6.00 surcharge will be added to the invoice. Any delivery rescheduled with less than eight weeks notice will be charged a 2% surcharge for every month of delay.

MINIMUM ORDER is U.S. $50.—plus shipping and applicable taxes.

LOST OR DAMAGED SHIPMENT. Contact the Common Carrier and APEX at once. Failure to do so within 30 days from shipment date will void the insurance claim. APEX MICROTECHNOLOGY is not responsible for loss or damage in transit, but will process the insurance claim for you. If the shipment was required to be uninsured, APEX will supply proof of shipment, thereby creating a legal obligation to pay the original invoice when due.

PRODUCT RETURNS within 30 days of shipment, will be accepted only if prior authorization has been obtained from APEX and the units have been used within the specified operating conditions. No solder residue should be on the pins. Restocking charge is 25% for standard industrial products. Custom and military products are not returnable.

PRICES are published in the latest U.S. price list. Custom processing charges are published separately. F.O.B. is Tucson, AZ, U.S.A. Applicable state and local taxes will be added.

CANCELLATION CHARGES are 15% for standard products. For customized products they are:
25% if components purchase orders have been placed.
50% if parts assembly has been started.
75% if parts have been capped.

PAYMENT TERMS for approved accounts are net 30 days from the date of shipment, C.O.D. for new accounts without D & B rating. Past due accounts will be charged a .06% per day late fee.

BILLING in duplicate is done on the day of shipment. Air freight charges will be billed by the carrier directly to the customer. On prepaid orders, the air express shipping charges are paid by APEX.

DOMESTIC SALES REPRESENTATIVES

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421-1865

ALABAMA, KENTUCKY, MISSISSIPPI, TENNESSEE
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Bill Peak, Jr.
Huntsville, Alabama
Tel: (205) 536-1506
Fax: (205) 551-0558

CALIFORNIA (Northern)
KOLM MARKETING
CONTACT: Henry Kolm
Los Altos, California
Tel: (415) 948-2635
Fax: (415) 948-6284

CALIFORNIA (Southern)
COM-STAR
CONTACT: Merlin Carlson
Rancho Cucamonga, California
Tel: (714) 944-5744
Fax: (714) 989-3367

DELAWARE, DISTRICT of COLUMBIA, MARYLAND, PENNSYLVANIA (Eastern), VIRGINIA
NELSON ELECTRONICS
CONTACT: Pat Nelson, Mike Antonucci
Ellicot City, Maryland
Tel: (301) 747-7887
Fax: (301) 465-1378

FLORIDA, Melbourne
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Steve Terlep
Melbourne, Florida
Tel: (407) 724-6795
Fax: (407) 951-9717

FLORIDA, Orlando
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Walt Currie
Orlando, Florida
Tel: (407) 855-0843
Fax: (407) 851-1464

FLORIDA, Tampa
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Jack Clark
Tampa, Florida
Tel: (813) 963-1076
Fax: (813) 968-2480

GEORGIA
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Darrell Pahl
Duluth, Georgia
Tel: (404) 497-9404
Fax: (404) 497-9412

ILLINOIS, IOWA
INDUSTRIAL REPRESENTATIVES, INC.
CONTACT: Mark Mitchell
Skokie, Illinois
Tel: (708) 967-8430
Fax: (708) 967-5903

MAINE, MASSACHUSETTS, NEW HAMPSHIRE, RHODE ISLAND, VERMONT
SIGNAL SALES
CONTACT: Dick Means
Woburn, Massachusetts
Tel: (617) 938-7872
Fax: (617) 938-8199

MINNESOTA, NORTH DAKOTA, SOUTH DAKOTA
INDUSTRIAL REPRESENTATIVES, INC.
CONTACT: Steve Bierma
Bloomington, Minnesota
Tel: (612) 854-8027
Fax: (612) 854-8312

NEW JERSEY, NEW YORK (Southern)
K & R ENGINEERING SALES
CONTACT: Bob Resker
Flanders, New Jersey
Tel: (201) 584-5235 (800) 631-9362
Fax: (201) 584-4375

NORTH CAROLINA, SOUTH CAROLINA
CURRIE, PEAK & FRAZIER, INC.
CONTACT: Mac Wylie
Greensboro, North Carolina
Tel: (919) 373-0380
Fax: (919) 273-6308

TEXAS (Texas Instruments only)
REPMASTERS
CONTACT: Wayne Ooten
Sherman, Texas
Tel: (214) 247-6236
Fax: (214) 892-0148

WISCONSIN
INDUSTRIAL REPRESENTATIVES, INC.
CONTACT: Kevin Heuvelmans
Brookfield, Wisconsin
Tel: (414) 789-9393
Fax: (414) 789-9272

For states or regions not listed above, please call Apex directly for assistance at (602) 742-8602, or Fax (602) 888-3329.

APEX INTERNATIONAL SALES REPRESENTATIVES

APEX MICROTECHNOLOGY CORPORATION • TUCSON, ARIZONA • APPLICATIONS HOTLINE (800) 421 1865

AUSTRALIA, NEW ZEALAND
K.D. FISHER AND
COMPANY PTY. LTD.
Adelaide, South Australia
Tel: (61) 8-277-3288
Fax: (61) 8-276-4024

AUSTRIA
NANO-80 GmbH.
Wien
Tel: [43] (222) 5051522-0
Fax: [43] (222) 5051522-21

BELGIUM, LUXEMBOURG
ALCOM ELECTRONICS B.V.B.A.
Kontich
Tel: (30) 3/458.30.33
Fax: (30) 3/458.31.26

CANADA, Ontario
bbd ELECTRONICS, INC.
Toronto
Tel: (416) 821-7800
Fax: (416) 821-4541
Telex: 06-218523

bbd ELECTRONICS, INC.
Ottawa
Tel: (613) 564-0014
Fax: (416) 821-4092

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bbd ELECTRONICS, INC.
Montreal
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Fax: (514) 697-0277

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bbd ELECTRONICS, INC.
Edmonton
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Fax: (416) 821-4092

CANADA, Manitoba
bbd ELECTRONICS, INC.
Winnipeg
Tel: (204) 942-2977
Fax: (416) 821-4092

CANADA, British Columbia
bbd ELECTRONICS, INC.
Vancouver
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Fax: (416) 821-4092

DENMARK
C-88 AS
Kokkedal
Tel: +45 42 24 48 88
Fax: +45 42 24 48 89

FINLAND
SW INSTRUMENTS OY
Espoo
Tel: (358) 0-8041041
Fax: (358) 0-881911

FRANCE
MICROEL
Les Ulis Cedex
Tel: [33] (1) 69.07.08.24
Fax: [33] (1) 69.07.17.23
Telex: 692493 F MICRO

GERMANY
EMTRON ELECTRONIC GmbH.
Nauheim
Tel: [49] (6152) 61081
Fax: [49] (6152) 69347

HONG KONG/PEOPLE'S REPUBLIC OF CHINA
EXCELPOINT COMPANY LIMITED
Honk Kong
Tel: (852) 8339013
Fax: (852) 8345508

INDIA
IRYS ENGINEERING SERVICES
Pune
Tel: 91 (212) 339836
Fax: 91 (212) 436798
Telex: (953) 145679

ISRAEL
BORAN TECHNOLOGIES LTD.
Petah Tikva
Tel: 972-3-9345171
Fax: 972-3-9344235
Telex: 381512

ITALY
CONSYSTEM s.r.l.
Milano
Tel: [39] 2-99041977
Fax: [39] 2-99041981

JAPAN
KYOKUTO BOEKI KAISHA LTD.
Tokyo
Tel: [81] (3) 3244-3787
Fax: [81] (3) 3246-1846
Telex: J22440 KYOKUBO J

KOREA
MAINSAIL MERCANTILE LTD.
Seoul
Tel: 82 (2) 745-2761
Fax: 82 (2) 745-2766
Telex: K33143

THE NETHERLANDS
ALCOM ELECTRONICS B.V.
A.J. Capelle a/d Ijssel
Tel: 31-10 451-9533
Fax: 31-10 458-6482

NORWAY
ELTRON A/S
Oslo
Tel: [47] (2) 500650
Fax: [47] (2) 502777

SINGAPORE, MALAYSIA, THAILAND, INDONESIA
EXCELPOINT SYSTEMS (PTE) LTD.
Singapore
Tel: (65) 284 8537
Fax: (65) 284 8547
Telex: RS25343 EPSPL

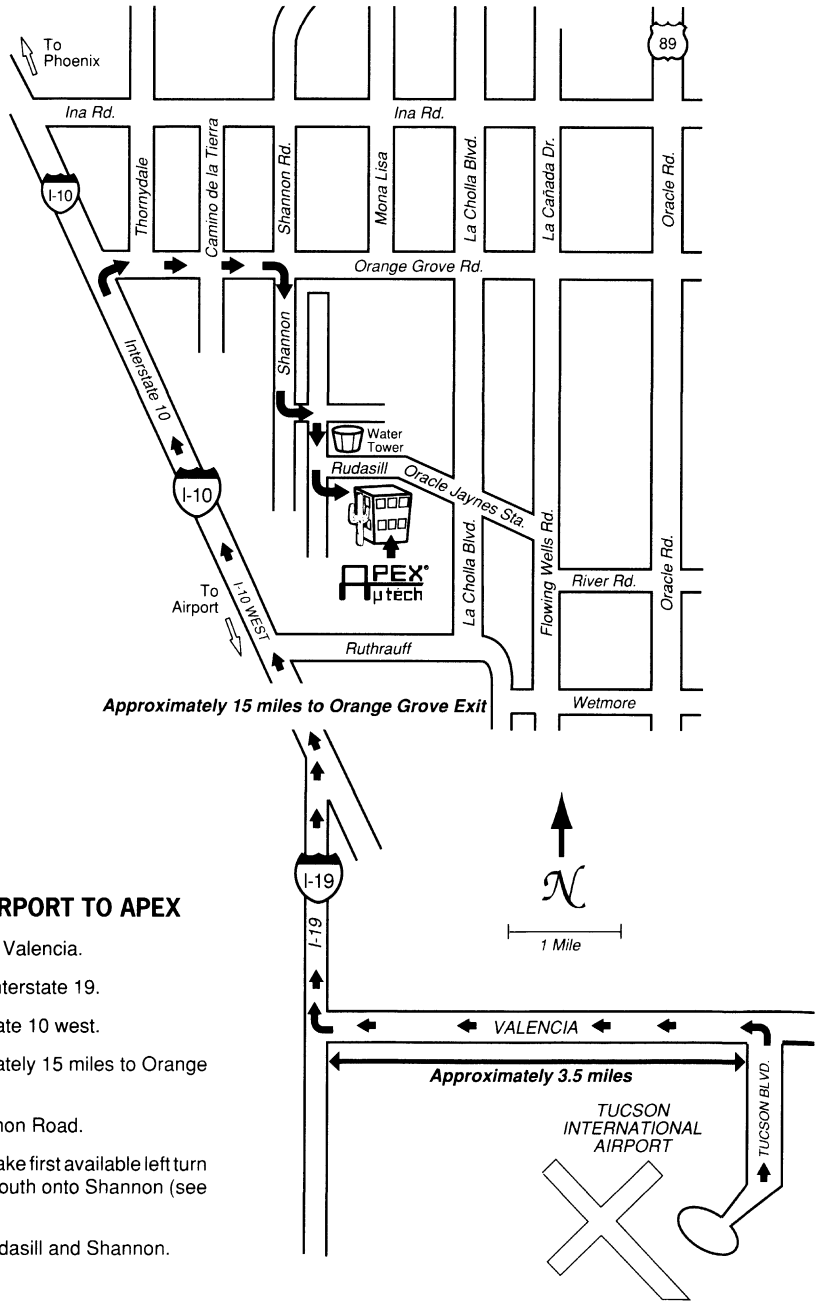
SPAIN
ADM ELECTRONICA, S.A.
Madrid
Tel: 34 (1) 409 47 25
Fax: 34 (1) 409 69 03

SWEDEN
EGEVO ELEKTRONIK AB
Spanga
Tel: [46] 8-7959650
Fax: [46] 8-7957883

SWITZERLAND
HEMAR AG
Baden
Tel: [41] 56-26 54 86
Fax: [41] 56-26 17 73
Telex: 826398

TAIWAN, REPUBLIC OF CHINA (R.O.C.)
PROSPECT TECHNOLOGY CORP.
Taipei
Tel: 886-2-721-9533
Fax: 886-2-773-3756

UNITED KINGDOM
MICROELECTRONICS
TECHNOLOGY LTD.
Oxford
Tel: 44 (844) 278781
Fax: 44 (844) 278746



DIRECTIONS FROM AIRPORT TO APEX

Tucson Blvd. north 1 mile to Valencia.

Valencia west 3.5 miles to Interstate 19.

Interstate 19 north to Interstate 10 west.

Interstate 10 west approximately 15 miles to Orange Grove exit.

Orange Grove east to Shannon Road.

Shannon south to Rudasill. Take first available left turn then right turn after turning south onto Shannon (see map).

APEX is on the corner of Rudasill and Shannon.

PRODUCT MARKING

PA12M/883 — LINE 1

APEX μtech — LINE 2

5962-XXXXXXXXXX — LINE 3

MB309 Q 9117 — LINE 4

Δ USA BeO — LINE 5

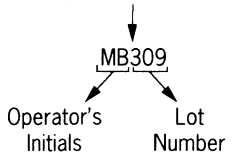
60024 — LINE 6

LINE 1
SMD* Parts: Apex Model Number
Standard Parts: Apex Model Number
Custom Parts: Blank

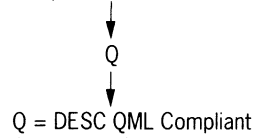
LINE 2
All Parts: APEX logo

LINE 3
SMD Parts: DESC SMD Part Number
Standard Parts: Blank
Custom Parts: APEX Model Number

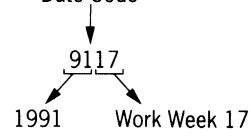
LINE 4
All Parts: Lot Code



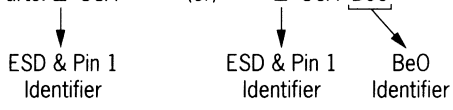
Compliance Indicator



Date Code



LINE 5
All Parts: Δ USA (or) Δ USA BeO

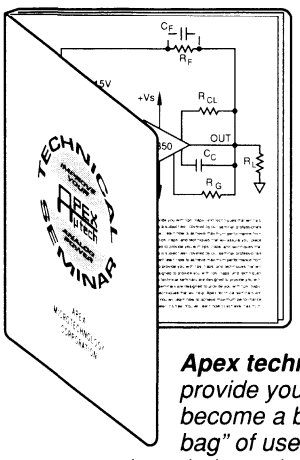


LINE 6
All Parts: 60024 = APEX CAGE Code

* SMD = Standardized Military Drawing

SUBJECT INDEX

SUBJECT INDEX (CONTINUED)



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IMPROVE YOUR ANALOG POWER, IT'S FREE!

Apex technical applications seminars *are designed to provide you with tips, traps and techniques that will help you become a better Analog Designer. We will give you a "grab bag" of useful circuits, explain their pros and cons, and show their use in real-world applications. You will learn how to achieve maximum performance from your designs as well as avoid common pitfalls.*

MAJOR TOPICS

- ***INSIDE POWER OP AMPS***
- ***AMPLIFIER LIMITATIONS AND THEIR EFFECTS***
  Slew Rate • Output Saturation • Current Limit • Common Mode Voltage • Safe Operating Area
- ***STABILITY AND COMPENSATION***
  Sources of Instability • Tricks and Fixes • Precautions and Practices
- ***PROTECTION***
  Input and Output • Thermal and SOA
- ***HIGH SPEED TECHNIQUES***
  Slew Rate Enhancement • Settling Time
- ***GENERAL APPLICATIONS***
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To find out more about upcoming seminars in your area, call the Apex Applications Hotline (800) 421-1865, or contact your local Apex sales representative.